Development of Readout Electronics for the ATLAS Tile Calorimeter at the HL-LHC

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for the degree of Doctor of Philosophy.

Declaration

This dissertation is the result of my own work, except where explicit reference is make to the work of others. It has not been submitted for another qualification to this or any other university.

Fernando Carrió Argos

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Preface

The Large Hadron Collider (LHC) is one of largest particle accelerators in the world. It has been used to explore energy frontier physics since 2010, with a collaboration composed of more than 7,000 scientists from 60 different countries. After a major upgrade that will occur in the 2020s, the LHC will become the High Luminosity LHC (HL-LHC). The HL-LHC will increase the instantaneous luminosity by a factor 5 compared to the LHC. The integrated luminosity of the HL-LHC program will be 10 times the integrated luminosity of LHC.

The R&D HL-LHC efforts involve a large community in Europe, but also in the US and Japan. The design of the HL-LHC and the consequent upgrade of the experiments at the HL-LHC represents an exceptional technological challenge. New accelerator technologies are under development such as superconducting magnets and cavities and high-throughput electronics to receive and process the extraordinary amount of data generated by the experiments. In addition, the new readout and trigger architecture planned for the ATLAS in the HL-LHC requires a complete redesign of the front-end and back-end electronics systems to cope with the new requirements in radiation levels, data bandwidth and clocking distribution.

This thesis is focused on the development of readout electronics for the ATLAS experiment at the HL-LHC, particularly in the design of the Tile Preprocessor (TilePPr) prototype envisaged for the readout of the Tile Calorimeter and communication with the ATLAS trigger system.

Chapters 1 and 2 present an introduction to the LHC and HL-LHC experiments, followed by an extensive review of the Tile Calorimeter and the plans for the ATLAS Phase II Upgrade for the HL-LHC.

The TilePPr prototype hardware design is fully described in Chapter 3, followed by the result of signal integrity simulations that confirmed the correct design of the PCB. At the end of the chapter some experimental results obtained during the initial tests with the first prototypes are presented.

Chapter 4 describes all the firmware developments implemented for the operation of the Demonstrator module in the TilePPr prototype and in the DaughterBoard. This chapter includes a detailed description of all the firmware blocks designed for the front-end and back-end electronics, focusing in the development of high-speed data links with fixed and deterministic latency.

Chapter 5 presents the development of FPGA-based circuits for the precise measurement of phase differences between clocks. A phase measurement circuit, called OSUS, based on oversampling techniques is discussed. The experimental results with the OSUS circuit obtained from its implementation in the TilePPr prototype are presented here. The OSUS circuit permits the synchronization of the Demonstrator module and the LHC clock, as well as the monitoring of the phase stability of clocks with a precision of about 30 $\mathrm{ps}_{\mathrm{RMS}}$.

Chapter 6 includes a description of the testbeam setup and some experimental physics results obtained. During these testbeam campaigns the TilePPr prototype was the main readout system in the back-end electronics operating the Demonstrator module.

Finally, the conclusions and future plans for this work are given at the end of this document.

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Chapter 1

The Large Hadron Collider

1.1 Introduction

The Large Hadron Collider (LHC) [1] is the world's largest and most powerful particle accelerator. It is installed and operated at the European Organization of Nuclear Research (CERN) in a circular tunnel of 27 km and 100 m underground, crossing the border of France and Switzerland, close to Geneva. The LHC is composed of super-conducting magnets designed to collide proton beams at a center-of-mass energy of $\sqrt{s} = 14$ TeV, delivering an instantaneous luminosity of $\mathcal{L} = 1 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$.

The LHC is the last stage of a series of accelerators increasing the energy of the proton beams. Figure 1.1 shows a diagram of the CERN's accelerator complex and how they are interconnected. Linac2 and PS Booster compose the first stages of the accelerator complex where the proton beam reaches an energy of 1.4 GeV. Then, the beam is injected into the Proton Synchrotron (PS) which accelerates the beam up to 25 GeV. The Super Proton Synchrotron (SPS) receives the protons from the PS and accelerates them to 450 GeV before injecting them into the LHC. Finally, in the LHC proton beams are accelerated to their maximum energy in two separated beam pipes where beams travel in opposite directions before colliding.

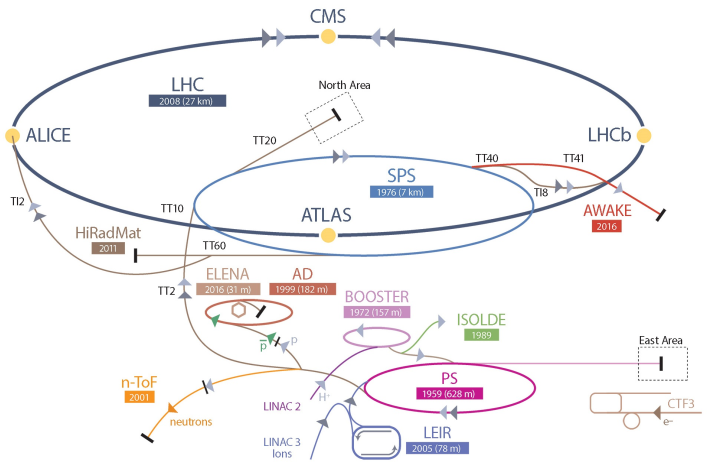


Figure 1.1: The CERN's accelerator complex.

1.1.1 LHC experiments

Seven experiments installed around the LHC analyze the particles produced in the collisions. The LHC collides the proton beams at four interaction points around the accelerator ring corresponding to the location of the main experiments: ATLAS (A Toroidal LHC ApparatuS) [2], CMS (Compact Muon Solenoid) [3], ALICE (A Large Ion Collider Experiment) [4] and LHCb (Large Hadron Collider beauty) [5].

The two largest experiments, ATLAS and CMS, are multi-purpose experiments located in opposite sides of the LHC ring. ATLAS and CMS were designed and optimized to measure the properties of the strong and electroweak forces with high precision at the TeV scale, and studying new physics beyond the Standard Model. In 2012, both experiments announced the discovery of the Higgs boson [6] with a mass around 125 GeV. The LHCb studies B-physics and the CP violation whereas ALICE experiment investigates the quark-gluon plasma through heavy ion collisions.

The other three experiments in the LHC are much smaller in size. The TOTEM (TOTal Elastic and diffractive cross-section Measurement) [7] experiment is near the CMS detector and performs high-precision measurements of the proton size and the LHC luminosity. The LHCf (LHC forward) [8] is located near the ATLAS detector and studies the particle generation in the forward region of collision as a simulation of cosmic rays in laboratory conditions. The last experiment approved by the LHC is the MoEDAL (Monopole and Exotics Detector at the LHC) [9]. The MoEDAL is installed in the walls of the LHCb cavern and searches directly for the magnet monopole.

1.2 The ATLAS experiment

The ATLAS experiment [2] is a general-purpose detector designed to study the products of p-p collisions at the LHC. The ATLAS detector is the largest detector in the LHC and is about 45 meters long, more than 25 meters high, and has an overall weight of approximately 7,000 tons.

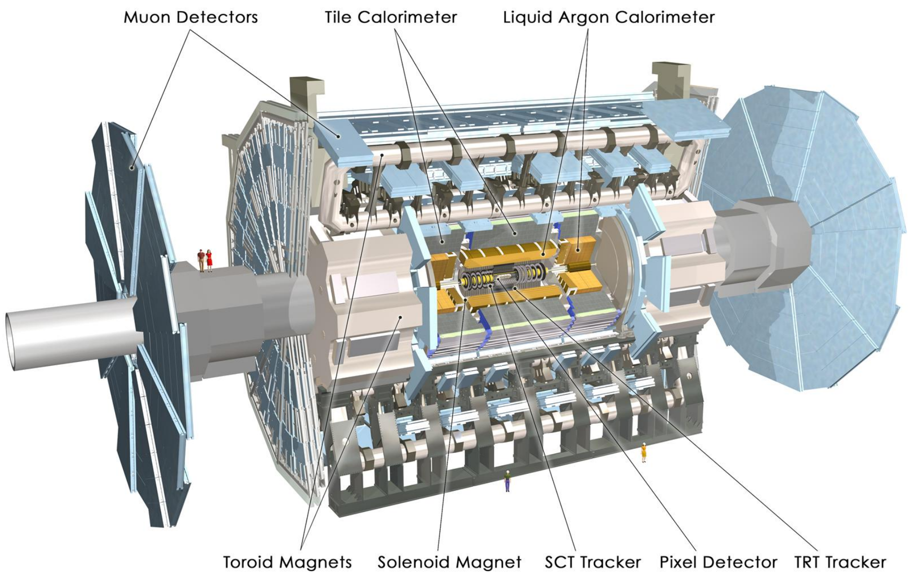


Figure 1.2: The ATLAS experiment.

The two proton beams collide at the center of the ATLAS detector producing particles in all directions. The ATLAS experiment is composed of different subdetectors to measure the different type of particles emerged from the collisions: the Inner Detector (ID), electromagnetic and hadronic calorimeter systems and the Muon Spectrometer (MS).

Built around the beam pipe, the ID is located at the inner part of ATLAS. It was designed for tracking and vertexing by the measurement of the trajectories of the charged particles generated in the collisions. A solenoidal magnet surrounds the ID generating a magnetic field of 2 Tesla which bends the trajectories of the charged particles. The curvature of the trajectories is used for the calculation of the particle momentum. Surrounding the ID, the Liquid Argon (LAr) and the Tile (TileCal) calorimeters measure the deposited energy and reconstruct the direction of different types of particles. The outermost layer of the ATLAS is composed of the MS and a toroid magnet, where a muon tracking system measures the trajectories of the muons beyond the calorimeters. Three superconducting air-core toroid magnets surrounding the ATLAS detector generate a field of 0.5 Tesla in average to bend the trajectory of charged particles.

The ATLAS detector provides high precision measurements of different types of particles and processes.

The design requirements of the ATLAS detector include the following aspects:

- Very good electromagnetic calorimetry for electron and photon separation and measurement, complemented by a full coverage hadronic calorimetry for accurate jet and missing transverse energy (E_T^{miss}) measurements.
- High-precision muon measurements, with the capability to guarantee accurate measurements at the highest luminosity using the external muon spectrometer alone.
- Efficient tracking at high luminosity for high-p_T lepton-momentum measurements, electron and photon identification, τ -lepton and heavy-flavour identification, and full event reconstruction capability at low luminosity.
- Triggering and measurement of particles at low-p_T, providing high efficiencies for most physics processes of interest at LHC.
- Large acceptance in pseudorapidity (η) with almost full azimuthal angle (ϕ) coverage. The azimuthal angle is measured around the beam axis, while the pseudorapidity is measured with respect to the plane perpendicular to the beam line and derived from the polar angle (θ):

$$\eta = -\ln\left(\tan\left(\frac{\theta}{2}\right)\right) \tag{1.1}$$

1.2.1 Trigger and Data AcQuisition system

The current ATLAS trigger system [10] is composed of 3 levels of event selection. While the Level 1 (L1) trigger system is completely based on custom hardware designed for the ATLAS detector, the Level 2 (L2) and the Event Filter (EF) levels are largely based on Commercial Off-The-Shelf (COTS) components. Each trigger level refines the event selection that the previous level provided, thus reducing the trigger rate. A schema of the ATLAS Trigger and Data AcQuisition (TDAQ) system is shown in Figure 1.3.

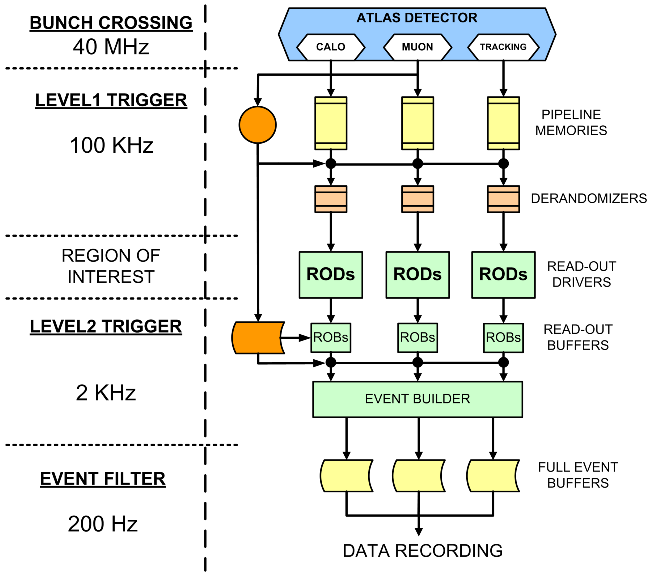


Figure 1.3: ATLAS trigger and data acquisition system.

The L1 decision is based on reduced-granularity information provided by the Resistive Plate Chambers (RPC) and Thin-Gap Chambers (TGC) for high p_T muons, and by the calorimeters for electromagnetic clusters, jets, τ-leptons, E_T^{miss} and large E_T. The L1 trigger reduces the event rate from 40 MHz to a maximum of 100 kHz on average. The L1 decision must arrive to the readout electronics in less than 2.5 μs, meanwhile the front-end electronics keeps the events in pipeline memories.

The L2 trigger decision is based on Regions of Interest (RoI). The RoIs are regions of the detector where the L1 has identified possible trigger objects within the event with full-granularity and full-precision. The RoI are stored in the Read Out Buffers (ROBs) until the L2 trigger system process them. The L2 trigger system uses the ROIs information on coordinates, energy and type of signature to reduce the amount of data and reduces the event rate below 3.5 kHz, with an average event processing time of approximately 40 ms.

In the final trigger decision level the Event Filter (EF) process the complete events built in the Event Builder (EB) system and the events selected are permanent stored in the CERN computer center for further physics analysis. Although the EF was initially designed to reduce the output to about 200 Hz, during the Run 1 (2010-2012) the trigger event output was 800 Hz.

In addition, the Data AcQuisition (DAQ) system provides infrastructure for the configuration, control and monitoring of the ATLAS detector, while the Detector Control System (DCS) supervises the detector services, such as power supplies or gas systems.

1.3 The Tile Calorimeter

The Tile Calorimeter detector [2] [11] is a sampling calorimeter which uses steel as absorber and scintillator tiles as active medium. It covers the region, $|\eta|<1.7$, behind the liquid argon electromagnetic calorimeter. TileCal is divided into a central Long Barrel, 5.6 meters in length, and two Extended Barrels, 2.6 meters in length. The radial depth of TileCal is approximately 7.4 λ (interaction lengths). Each barrel is azimuthally divided into 64 wedges of size $\Delta\phi \sim 0.1$, made of steel plates and scintillator tiles, with a total weight of 2,600 metric tons for the complete detector.

The combination of the orientation of the scintillator tiles radially and normal to the beam axis with wavelength-shifting (WLS) fiber readout on the tile edges, allows for almost seamless azimuthal calorimeter coverage. The WLS fibers are grouped into bundles defining 5,182 calorimetric cells. The fiber bundles are read out by 9,852 PhotoMultiplier Tubes (PMTs) providing an approximate projective geometry in pseudorapidity. There is a gap region between the long and the extended barrel which is instrumented with special cells. The front-end electronics and readout optics are highly integrated within the mechanical structure of TileCal. The PMTs and all the readout electronics are housed on aluminum units, called super-drawers, located at the outermost part of TileCal. The front-end electronics also provide analogue sums of channels from cells with the same η coordinate, forming trigger towers which are the basis for the L1 trigger processing. The low-voltage power supplies of the front-end electronics are mounted in an external steel box at one of the sides of the super-drawer which contains the connections for power and other services. For the calibration systems, the calorimeter is equipped with a laser system, a Charge Injection System (CIS) and a ^{137}Cs radioactive source which are employed to calibrate the detector response to the electromagnetic scale with a high precision. The structure of the TileCal modules is depicted in Figure 1.4.

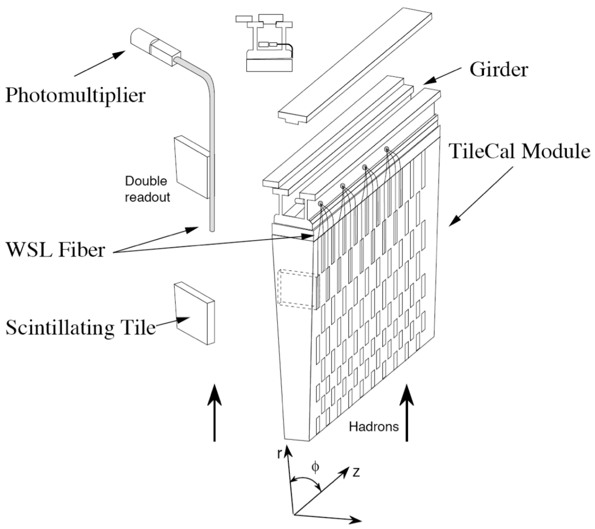


Figure 1.4: Structure of a TileCal module and main components.

1.3.1 Optics

The TileCal active medium is composed of scintillating tiles of eleven different sizes [12] of 3 mm thickness and with radial lengths ranging from 97 mm to 187 mm and azimuthal lengths ranging from 200 mm to 400 mm, where different size of the tiles corresponds to different depth in radius. Ionizing particles crossing the tiles induce the production of ultraviolet scintillation light in the polystyrene base material of the tiles and this light is subsequently converted to visible light by wavelength shifting.

The tiles are surrounded by a plastic sleeve to protect the tile and improve the scintillation light yield due to its high reflectivity of 95%. In addition, the plastic sleeve contains a mask pattern to reduce the optical non-uniformity of the tiles to a level below 5% for the sum of signals of both sides of the tile. The WLS fibers are attached to the tile edges to collect the light produced in the scintillators and shift its wavelength to a longer one. Each WLS fiber collects light from tiles and routes it to the PMTs inserted into the super-drawers.

The WLS fibers are grouped together in bundles and coupled to the PMTs. The fiber grouping defines a three-dimensional cell structure to form three radial sampling depths, approximately 1.5, 4.1 and 1.8 λ thick at $\eta = 0$. These cells have dimensions $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ in the first two layers and 0.2×0.1 in the last layer. The depth and η-segmentation of the barrel and extended barrel modules are shown in Figure 1.5. Each tile is read out by two different PMTs providing redundancy and sufficient information to partially equalize signals produced by particles crossing the calorimeter at different positions.

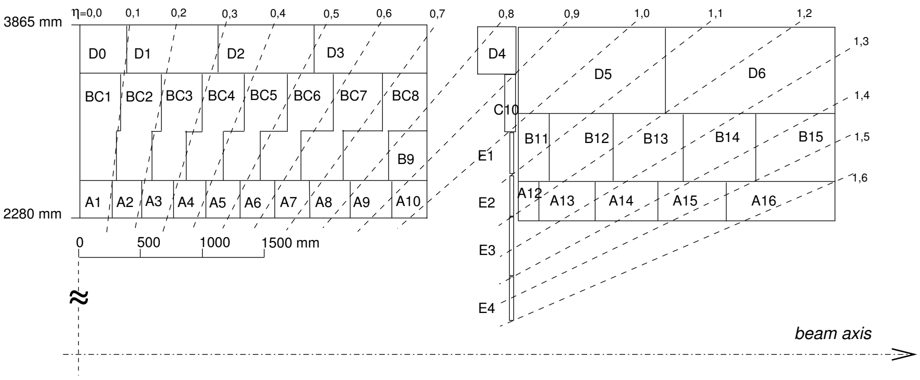


Figure 1.5: Segmentation in depth and η of the TileCal modules for half of a long barrel (left) and for an extended (right) barrel. TileCal cell distribution is symmetric respect to the interaction point at the origin.

1.3.2 Front-end electronics

The Long Barrel and Extended Barrels are subdivided in four partitions (EBA, LBA, LBC and EBC) as depicted in Figure 1.6. Each partition is contains 64 super-drawers for a total of 256 super-drawers. The front-end electronics [13] and readout components are housed inside the super-drawers, while the rest of the trigger and readout electronics are located off detector in the ATLAS counting rooms (USA15). Figure 1.7 depicts a block diagram of the TileCal electronics.

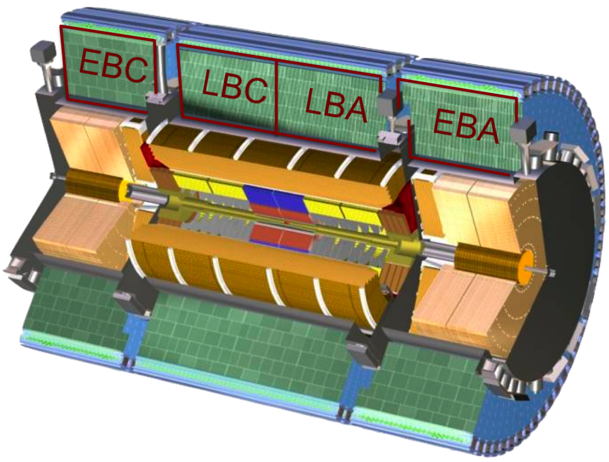


Figure 1.6: Tile Calorimeter partitions. EBA and EBC partitions correspond to the Extended Barrels and LBA and LBC partitions to the central Long Barrel.

Photomultiplier block

The PMT block is the key element in the readout chain as they measure the light produced by the scintillating tiles. It is composed of a mechanical structure made of steel cylinder and mu-metal shield for magnetic shielding and contains a light mixer, a PMT, a high voltage divider and the 3-in-1 card (Figure 1.8). The light mixer mixes the light from the readout fibers to ensure uniform illumination of the photo-cathode. The PMT blocks are inserted into the aluminum structure of the super-drawers, ensuring an accurate placement of the light mixer and WLS fiber bundle for each tile. The main components of a PMT block are the following:

- Photomultipliers: the PMT converts the light signal from the fiber bundles into an electric charge. The Hamamatsu R5900 PMT was selected to read out the tiles. This PMT has a compact size with of $28 \times 28 \times 28$ mm^3 and has a dynode structure with 8 amplification stages.

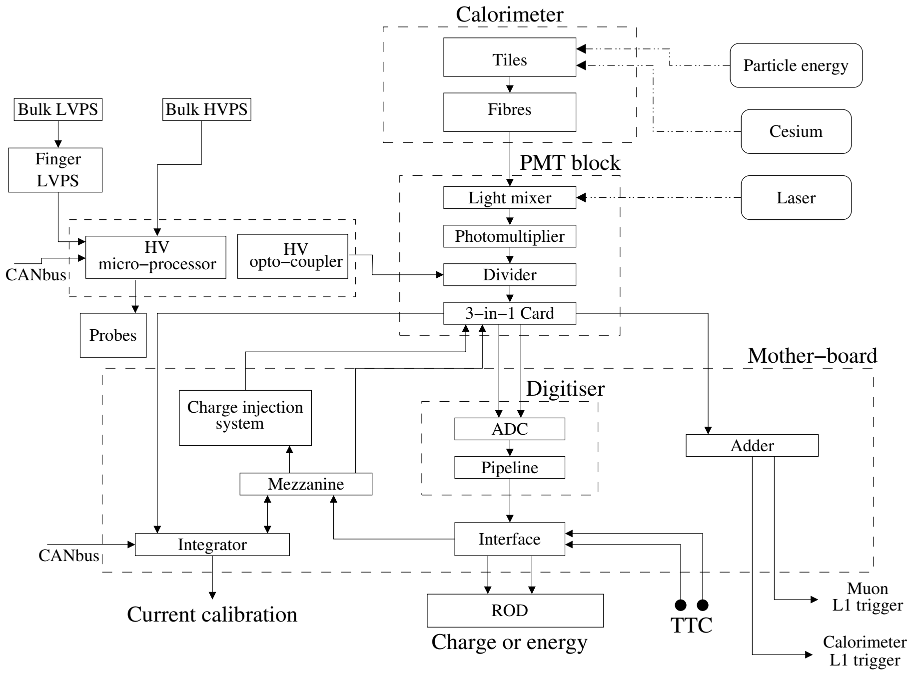


Figure 1.7: Block diagram of the TileCal electronics.

- Light mixers: since the PMT response depends over the photocathode surface position illuminated, a light mixer is used for mixing the light coming from all the fibers in the bundle, so that there is no correlation between the position of the fiber and the area of the photocathode receiving the light.

- Magnetic shielding: The mu-metal and iron magnetic shielding in the PMT must prevent residual fields from the ATLAS solenoid and toroids that could cause gain variations. It should provide a protection up to 500 Gauss magnetic fields in any direction.

- HV dividers: the primary purpose of the divider is to partition the high voltage between the dynodes of the PMT. The High Voltage (HV) divider also serves as a socket to allow the connection of the PMT to the front-end electronics without any interconnecting wires. This design minimizes the capacitance between the PMT and the electronics, which is important to reduce noise and unreliable connections.

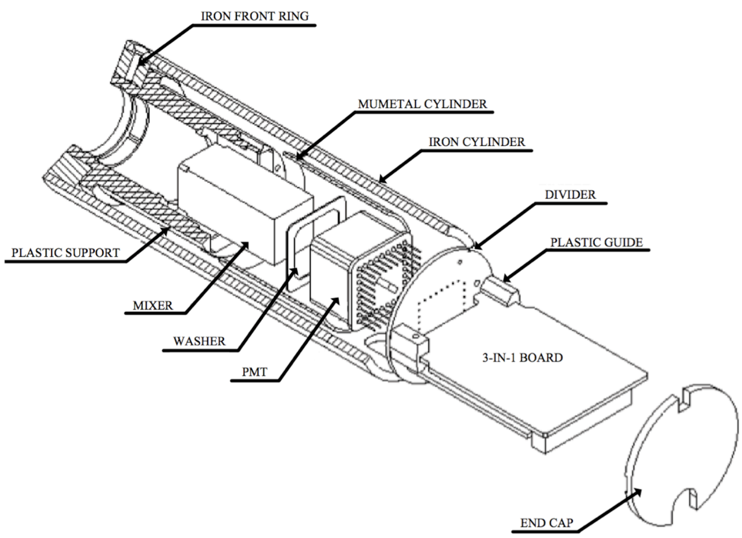


Figure 1.8: Scheme of the PMT block.

- 3-in-1 cards: these boards provide a high and a low gain shaped pulse for the digitizer boards, the charge injection calibration system and slow integration of the PMT signals for monitoring and calibration.

Digitizer system

The 3-in-1 cards amplify and shape the PMT signals generating two output signals, high and low gain with a gain ratio of 64. High and low gain signals are transmitted to the Digitizer boards, where they are digitized every 25 ns by 10-bit Analog-to-Digital Converters (ADC). The Digitizer board is equipped with two depth-configurable pipeline memories in the TileDMU ASIC [14] which store the digitized data until the reception of a L1 accept signal (L1A). Each TileDMU ASIC receives the digitized data from three channels, this is six channels per Digitizer board. Upon the reception of a L1A signal, a data frame containing up to 16 samples is copied into the derandomizer buffers in the Interface board for its transmission to the ROD system in the back-end electronics. In order to reduce the total data bandwidth during the normal operation only one of the two gains, and only 7 samples are read out. The sampling clock is provided by the TTCrx ASIC [15] and can be adjusted collectively for all ADC in a Digitizer board in steps of 106 ps. The phase adjustment of the clock is necessary to ensure that the central sample is near the pulse peak. The motherboard also contains an analog part to provide a voltage reference to the ADCs and two 8-bit Digital-to-Analog Converters (DAC) that provide a pedestal for the AC-coupled inputs. Each super-drawer of the LB contains up to 8 digitizer boards whereas the EB modules contains 6 digitizer boards.

Interface board

The Interface board [16] is the digital link with the back-end electronics system. Each module hosts one Interface board which receives and distributes the TTC signals to the electronics, collects and formats data from the digitizer boards, and transmits the digitized data via an optical link to the ROD system. The Interface board implements a redundant readout system with two output fibers to reduce possible errors due to single event upset, though, at a given time, only one of the two fibers is connected to the ROD system. Figure 1.9 shows a block diagram of the Interface board.

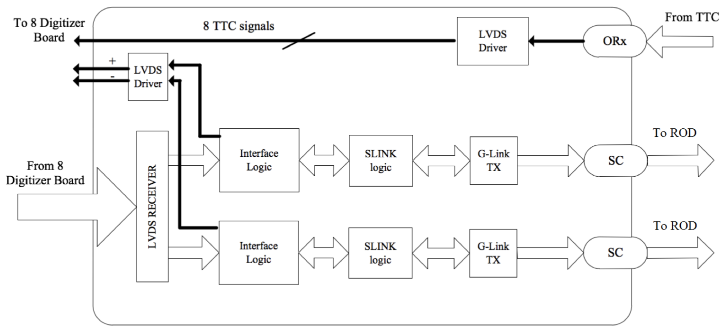


Figure 1.9: Block diagram of the functional blocks and data flow of the Interface board.

Adder board

The adder boards receive the analog signals from up to six 3-in-1 cards composing a trigger tower and perform an analog sum. Two analog sum results are sent to the L1 trigger system. The first analog sum comprises the sum of all the cells, while the second one only contains the last layer cell.

1.3.3 Back-end electronics

The back-end electronics system is installed in the counting rooms of the cavern (USA15), located 70 meters away from the detector and contains two different sub-systems: the Read Out driver (ROD) system and the Trigger, Timing and Control (TTC) system [17]. The back-end electronics is organized in four partitions, each one dedicated to the readout of the Long and Extended Barrels. These units are physically split into different crates: a 6U Versa Module Eurocard (VME) TTC crate and a 9U VME ROD crate.

Read Out Driver

The Read Out Driver [18] is the core element of the back-end electronics receiving data from 8 super-drawers through optical links. A total of 32 RODs, divided in four VME crates, one per barrel, are needed to read out the Tile Calorimeter, this is eight RODs per rack. The ROD module is composed of a ROD motherboard and four Processing Units (PU), each populated with two commercial Digital Signal Processor (DSP) chips that process the data before its transmission to the ATLAS DAQ system.

In addition, one Trigger and Busy Module (TBM) is installed per ROD crate. This 9U VME module receives and distributes the TTC signals from the local TTC system to the RODs, and also gathers the busy signals from eight RODs to provide a combined busy signal to the ROD Busy module.

Trigger, Timing and Control

The back-end TTC system is installed in four VME crates. Each TTC partition contains a series of VME boards to handle the TTC information in the different subsystems.

- Local Trigger Processor (LTP): the LTP receives the TTC signals from the Central Trigger Processor (CTP) and distributes them to the TTCvi module.

- LTP Interface (LTPI): the LTPI communicates multiple LTP modules with the CTP.

- TTC VME Bus Interface (TTCvi): the TTCvi provides the A and B channel signals to the TTCex for its encoding and distribution to the front-end electronics.
- TTC Emitter (TTCex): the TTCex converts the commands received from the TTCvi to optical signals.
- TTC Optical Coupler (TTCoc): the TTCoc fans out the optical signals up top 320 different destinations.
- ROD Busy module: this module monitors the busy signal, and produces the OR operation of the 16 busy input lines.

Other TileCal-specific modules are also present in the TTC crate, which are primary used for calibration purposes but also receive or handle TTC information.

- Shaft module: it controls the calibration trigger requests. It is primary used to share the calibration request during physics runs.
- TTC Receiver in PCIe Mezzanine Card (TTCpr) module: the TTCpr provides TTC information to the TDAQ software for the calibration runs. This board is attached into the Single Board Computer (SBC) of the TTC crate.
- Laser Read Out Driver: this module provides information from the Laser calibration system to the TDAQ software and distributes TTC signals to the Laser system.

The TTC rack location was chosen to minimize the length of the TTC fibers to the front-end crates and the associated contribution to the trigger latency, understood as the time difference between the bunch crossing identification (BCID) and the arrival time of the L1A signal to the front-end electronics system. In addition, the programmable delay lines of the calibration boards are configured to reproduce the timing of signals generated by particles originated from the interaction point.

1.4 Data flow of the TileCal readout chain

The complete readout process is shown in Figure 1.10. It starts collecting the light generated by particles crossing the TileCal scintillating tiles, and then routing it to the PMTs through WLS fibers. The PMTs convert the light into an electrical analog pulse which is shaped and amplified by the 3-in-1 cards, distributing two copies of the analog signal with a ratio of 1:64. The analog PMT signals are transmitted to the digitizers boards where the signals are digitized at the LHC frequency and stored in the configurable-depth pipeline memories of the TileDMU. In parallel to this operation, the low gain analog signals are summed in groups of five and the result is sent to the L1 trigger system.

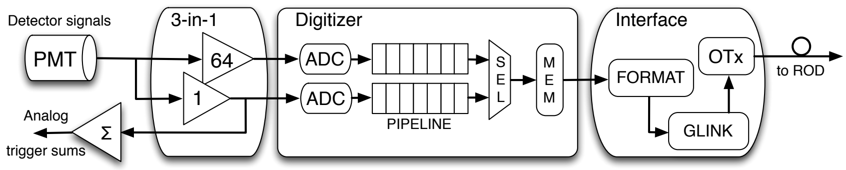


Figure 1.10: Block diagram of TileCal readout chain.

In the L1 trigger system, the CTP transmits the L1A signal through the TTC network via the LTP to the front-end electronics requesting the selected events at a mean rate of 100 kHz. When the front-end electronics receives the L1A signal, the TileDMU transmits the samples corresponding to the requested BCID to the Interface board. Then, the Interface board builds up a data fragment containing the samples from all channels in the super-drawer and transmit it to ROD system in the back-end electronics system. The data flow rate is controlled using a busy feedback signal from the back-end electronics to the CTP. The busy signal is generated by the RODs modules when the input buffers are full. This signal is transmitted to the TBM and ROD busy module which distributes it to the CTP, informing that it is not possible to accept new events.

Chapter 2

ATLAS Upgrades for HL-LHC

The High Luminosity upgrade of the Large Hadron Collider (HL-LHC) [19] is planned for the Long Shutdown 3 (LS3) period from 2024 to 2026. The HL-LHC will provide a nominal instantaneous luminosity of $\mathcal{L}$ =7.5 $\times$ 10^{34} cm^{-2}s^{-1}, 7.5 times the initial design luminosity, with an average of 200 inelastic collisions per bunch crossing. The HL-LHC will deliver an integrated luminosity of 300−350 fb^{-1} per year with the goal of 4000 fb^{-1} by 2035, about 10 times the integrated luminosity reached with the LHC. The central activity at the HL-LHC will be the measurement of the properties of the recently discovered Higgs boson and, in particular, the studies of the Higgs coupling to the different fermions and bosons, as well as the precise measurement of the trilinear Higgs self-coupling through the observation of di-Higgs production. The HL-LHC will produce high statistics data that will permit the study in detail of the Standard Model and physics Beyond the Standard Model. A temporal overview of the plans for the LHC evolution towards the HL-LHC is given in Figure 2.1.

The complete upgrade of the ATLAS detector [20] is planned in three different phases corresponding to the three long shutdown periods. After LS3, the ATLAS Phase II Upgrade will prepare the different sub-detectors for the HL-LHC luminosity conditions. The pile-up of events per beam crossing in ATLAS will increase from 20 to 200, requiring a finer granularity for the detectors and

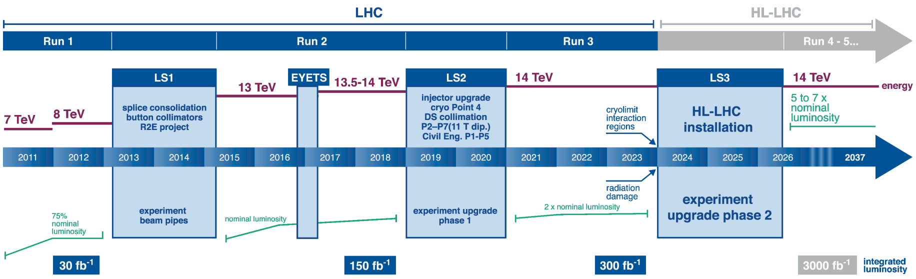


Figure 2.1: LHC plan for the next ten years, with a series of shutdowns with dedicated upgrades and increase of energy and luminosity.

a new TDAQ architecture able to handle the trigger rates and the amount of generated data. Moreover, the increment of the luminosity will require a new front-end electronics system more tolerant to radiation.

Some detectors, such as the Inner Detector, the LAr Forward Calorimeter and the Forward Muon Wheels will be more affected by the radiation and will require the complete replacement of the current detector and electronics. This is not the case for the calorimeters and muon chambers, where there is no necessity of replacing their structures and active materials. Only an upgrade of the front-end and back-end electronics systems is required in order to cope with the new radiation levels and data bandwidth.

2.1 TDAQ architecture

The TDAQ system will be completely redesigned for the HL-LHC to address the performance requirements in combination with the increased trigger rates and data volumes. The proposed TDAQ for the HL-LHC [21] consists of a single-level hardware trigger stage, called Level-0 (L0) trigger system, and a software system called Event Filter (EF). Figure 2.2 presents a block diagram of the single-level TDAQ architecture for the HL-LHC.

The L0 trigger system receives the information from the LAr and TileCal detectors, and the muon system reducing the trigger rate from 40 MHz to 1 MHz by the application of hardware-based algorithms.

The calorimeters provide coarse granularity data to the L0Calo system to identify electron, tau and jet candidates, and to calculate E_T^{miss}. In parallel,

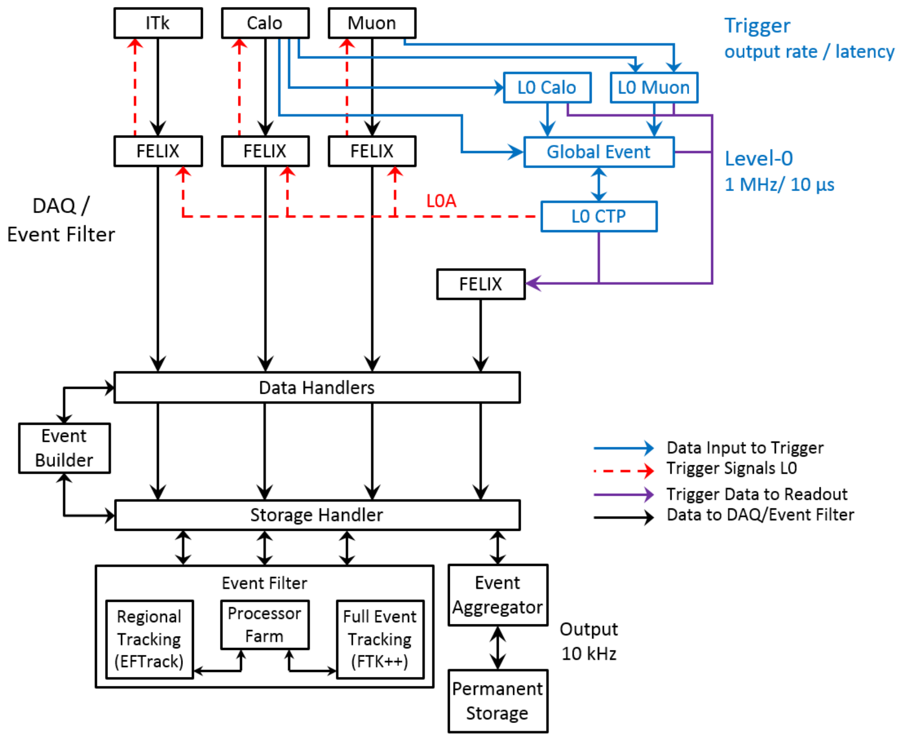


Figure 2.2: Block diagram of the single-level architecture envisaged for the TDAQ at the HL-LHC [21].

the L0Muon system receives data from all muon subsystems and from the most external cells of TileCal to identify muons. It also receives information from the Monitoring Drift Tubes (MDT) and RPCs to improve the muon trigger coverage.

The L0Calo and L0Muon systems provide trigger objects with reconstructed energies and spatial locations to the Global Event which combines them into higher level signatures. These signatures are then passed to the Level-0 Central Trigger Processor (L0CTP) which makes the Level-0 decision (LA0) based on several parameters.

Related to the readout path, all detectors transmit the data to a common readout system called Front-End LInk eXchange (FELIX) [22]. This system is used to transmit selected detector data to Level-0 trigger system using low latency point-to-point connections and also to interface the detector electronics with the DCS and TTC systems. The FELIX system sends the event data to the Data Handlers where data is reformatted and then buffered into the

Storage Handler before being transmitted to the EF for the application of the last trigger algorithms. The Storage Handler buffers the event data while the EF is processing the events between fills. In the last stage of the trigger architecture, the EF makes the final trigger decision using software algorithms at a rate of 10 kHz.

The TDAQ collaboration is also considering a second option: an architecture with two hardware levels (Level-0 and Level-1), where the L0 trigger rate reaches 4 MHz and the Level-1 (L1) trigger system implements more complex algorithms reducing the event rate to 800 kHz.

In order to fulfill the latency requirements imposed by the new TDAQ system and adding a margin for future developments, the detectors will implement large pipeline memories to store 10 μs of data for Level-0 and 35 μs for Level-1 (in the case of a L0/L1 trigger architecture). The latency, trigger and data rates between the detector readout and the trigger systems for both architecture options are summarized in Table 2.1.

	L0 schema	**L0/L1 schema**
L0/L1 trigger rate	4 MHz	4 MHz / 800 kHz
L0/L1 latency	10 μs	10 μs / 35 μs
Data rate to L0Calo and L0Muon	40.08 MHz	40.08 MHz
Latency data to L0Calo and L0Muon	1.7 μs	1.7 μs
Data rate to FELIX	1 MHz	800 kHz
Latency data to FELIX	10 μs	35 μs

Table 2.1: Trigger parameters and readout data rates for the two proposed TDAQ architectures.

2.2 Tile Calorimeter Upgrade

The motivation for the upgrade of the Tile Calorimeter is to fulfill the new requirements set by the HL-LHC. The complete replacement of the readout electronics is foreseen for the Phase II Upgrade [20] in order to meet the increased radiation tolerance requirements and to be compatible with the TDAQ architecture, providing more precise and higher granularity information to the trigger systems.

In the proposed TDAQ architecture the back-end electronics system will readout the detector and transmit pre-processed data from cells to the trigger system at the LHC frequency. In parallel to the data processing for the trigger system, the data samples will be stored in pipeline memories until the reception of a Level-0/Level-1 acceptance signal. A block diagram of the upgraded readout architecture is shown in Figure 2.3.

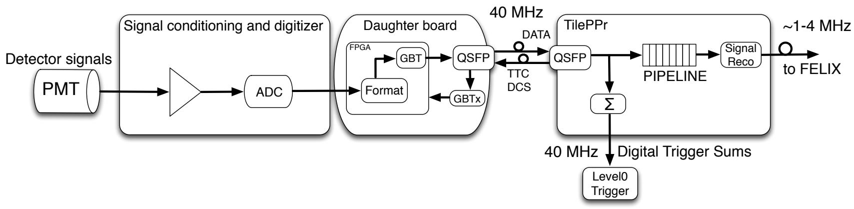


Figure 2.3: Block diagram of the TileCal readout architecture for the Phase II Upgrade.

The new TDAQ architecture requires a considerable increase in bandwidth and number of links between the front-end and back-end electronics systems, in addition to the use of high-speed links between the back-end electronics and trigger systems. While with the current system the detector is read out through 256 optical links with a bandwidth of 800 Mbps for each link, the new readout architecture requires 4096 optical links (including redundancy) transmitting at 9.6 Gbps per link.

Table 2.2 summarizes the main features of the current and the Phase II Upgrade readout systems.

Downlinks	**Current**	**Phase II**
Nbr. of links	256	2048
Link bandwidth	80 Mbps (TTC)	4.8 Gbps
Uplinks	**Current**	**Phase II**
Nbr. of links	256	4096
Link bandwidth	800 Mbps	9.6 Gbps
Nbr. of readout boards	32 (ROD)	32 (TilePPr)
Nbr. of crates	4 (VME)	4 (ATCA)
BW to DAQ per module	3.2 Gbps (ROS)	40 Gbps (FELIX)
BW to Trigger per module	Analog	~500 Gbps

Table 2.2: Comparison between the current and Phase II readout systems.

The Demonstrator module

In parallel with the developments of the readout electronics for the HL-LHC, the Demonstrator project aims to evaluate and qualify the upgraded trigger and readout electronics before the complete replacement of the electronics after the Phase II Upgrade.

A Demonstrator module containing the upgraded front-end electronics was developed in the framework of the project. It combines the Phase II readout electronics with the legacy analog interface for the L1 trigger system since the full digital trigger system will not be installed before the Phase II Upgrade. In the back-end electronics, a Tile Preprocessor (TilePPr) prototype will read out and operate the Demonstrator module. The TilePPr will store the samples in pipeline memories and transmit L1 selected data to the ROD modules keeping backward compatibility with the current DAQ system. The Demonstrator module will replace one of the super-drawers into the ATLAS experiment. The installation of the Demonstrator module into the ATLAS experiment is foreseen during one of the short LHC shutdowns planned for the Run 2.

2.2.1 Front-end electronics

The front-end electronics comprise the set of electronic equipment, boards and devices dedicated to the data readout and operation of the PMTs which are hosted in the TileCal modules. The electronics will be housed inside four aluminum structures per module, called minidrawers, placed in the outermost part of the detector. The mechanical design of the super-drawers has been modified to organize the front-end electronics in four independent modules improving the access and serviceability, and reducing the impact of the single point failures. Figure 2.4 shows the mechanical structure of the TileCal detector and how the super-drawers have been organized in minidrawers.

As is shown in Figure 2.5, each minidrawer houses up to 12 PMTs together with its corresponding Front-End Boards (FEB), one High Voltage board to distribute power to the PMTs, one MainBoard (MB) which receives the PMT signals and one DaughterBoard (DB) which interfaces with the back-end electronics.

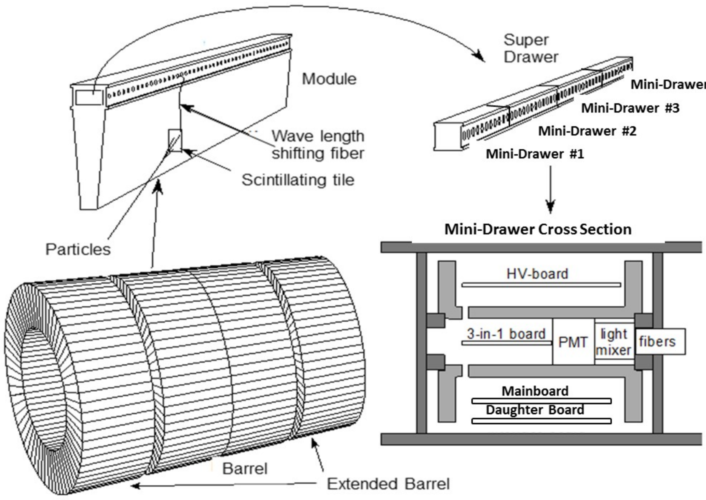


Figure 2.4: Picture of the TileCal modules and the minidrawers.

DaughterBoard

The DaughterBoard [23] provides a high-speed communication path between the front-end electronics and the TilePPr modules in the counting rooms (USA15). In the upgrade electronics, the DBs will be responsible for the reception and execution of configuration commands for the front-end electronics, as well as for collecting and transmitting the digitized signal from the PMTs to the TilePPr. In addition, the DBs will distribute the recovered LHC clock to the FEBs for the digitization of the PMT signals. Figure 2.6 depicts a block diagram with the main components of the DaughterBoard.

The DaughterBoard version 4 (Figure 2.7) was used during the 2015-2017 testbeam periods and will be integrated into the Demonstrator module. The DB version 4 fulfills all the requirements of the HL-LHC and is compatible with the three FEB options that will be presented in next sections. The DB was designed in two independent halves, corresponding to A and B sides, where each half serves 6 PMTs on one side of the minidrawer. The DB is populated with two Xilinx Kintex 7 Field Programmable Gate Arrays (FPGA) connected to two Quad Small Form-factor Pluggable (QSFP) modules. These connections provide a redundant high-speed communication with the back-end electronics.

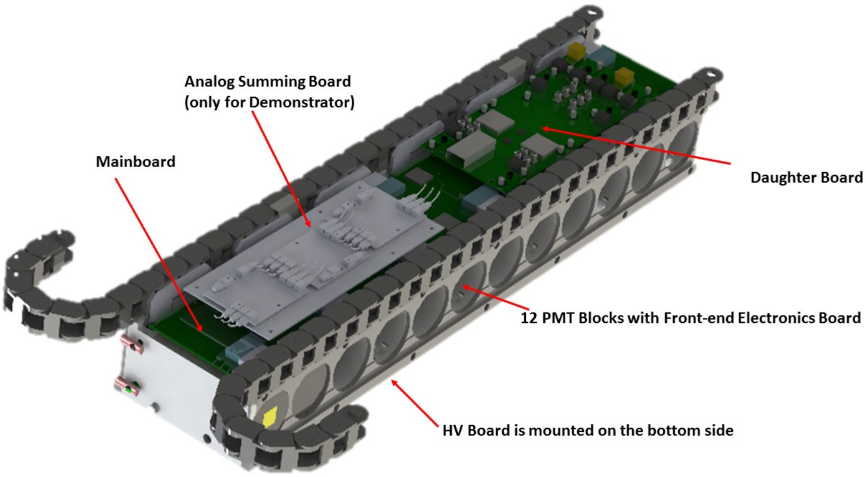


Figure 2.5: Detailed drawing of the minidrawer indicating the position of the different parts of the front-end electronics.

Each side of the DB includes one GBTx [24] chip per side which recovers the LHC clock and distributes it to the FPGA for the operation of the front-end electronics and communication with the back-end electronics. In addition, the GBTx also provides remote reset and configuration capabilities. Both FPGAs are connected to the GBTx through LVDS buffers forming two independent JTAG chains. The JTAG chain is closed transmitting the TDO signal to the back-end electronics using the FPGA not being programmed, and therefore only one FPGA can be programmed at a time. Although during the normal operation of the module the FPGAs will be configured from the on-board flash memories, the remote programming enables the possibility of programming the FPGAs if the flash memory is damaged or updating the firmware version in the flash memories.

A DB is connected to a MainBoard through a 400-pin FMC connector. This connector provides a high-speed path to receive the PMT digitized data and to configure and operate the FEBs. Related to the power distribution, each side of the DB is individually powered with 10 V from the MainBoard.

Different techniques will be implemented in the FPGA to prevent errors due to Single Event Upsets (SEU) or Multi Event Upsets (MEU). One of these techniques is the memory scrubbing where the FPGA configuration memory

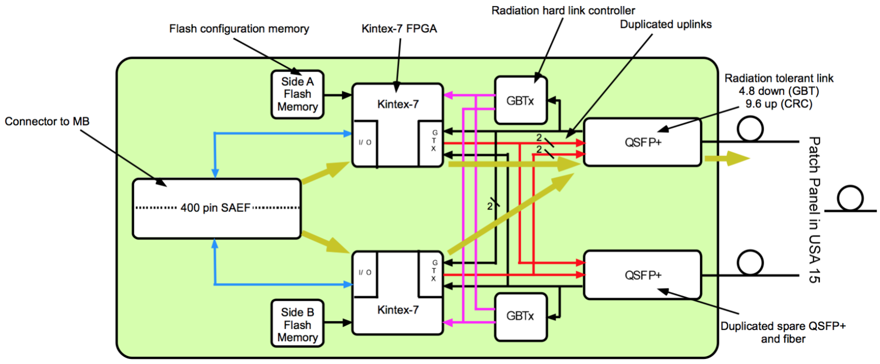


Figure 2.6: Block diagram of the DaughterBoard.

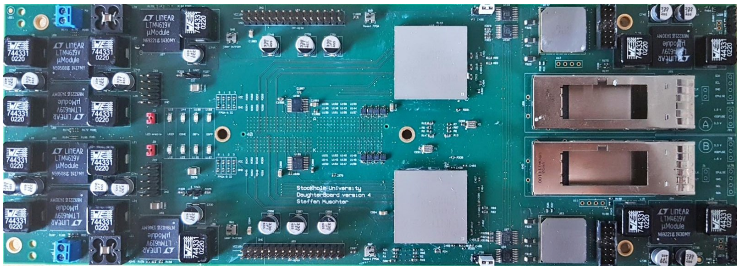


Figure 2.7: Picture of the DaughterBoard version 4.

is continuously checked and corrected if possible. For those cases where the memory integrity cannot be recovered the DB will be remotely reset or reprogrammed. Moreover, the Triple Modular Redundancy (TMR) will be implemented in firmware to reduce the likelihood of data errors due to SEU or MEU.

MainBoard

The MainBoard [25] controls the FEBs and also provides a high-speed path to transmit digitized PMT signals to the DaughterBoard. Depending on the FEB option the MainBoard could also include circuitry to digitize the signals coming from the FEBs. In this thesis, the MainBoard for the 3-in-1 option is covered in detail since it is used in the Demonstrator module.

3-in-1 front-end boards

The upgraded 3-in-1 FEB [26] is a revised version of the current FEB installed in ATLAS. This new FEB is composed of COTS components. It features dynamic range of 17 bits, better linearity and lower noise than the previous version. Functionality of the FEB includes: the fast signal processing chain, the slow signal processing chain and the calibration circuitry. Figure 2.8 shows a picture of the upgraded 3-in-1 card.

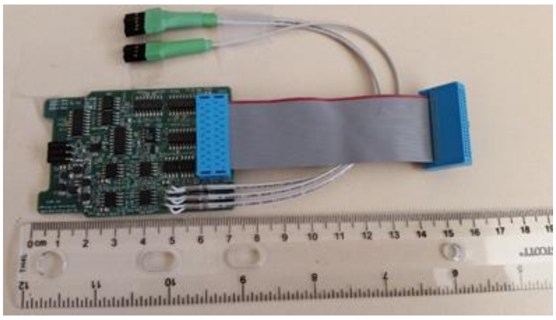


Figure 2.8: A 3-in-1 card designed for the HL-LHC.

Figure 2.9 presents a block diagram of the functional blocks of the 3-in-1 card. The fast signal processing chain includes a 7-pole passive LC shaper to transform a PMT pulse into a wider pulse. The wide pulse is amplified with two clamping amplifiers with a gain ratios of 1 and 32, providing the so-called high and low gain signals. The amplified signals are routed to MainBoard where they are digitized with on-board dual-channel 12-bit ADCs. The slow signal processing chain includes a 6-gain programmable slow integrator. It is used to monitor the average PMT currents for Cesium detector calibration, and monitoring of instantaneous luminosity. The precise charge injection circuit is connected to the shaper. Charge injection procedure is used to calibrate each readout channel and response of the amplifiers and ADCs, as well as the integrator circuit.

The 3-in-1 card was selected for the Demonstrator module since it is backward-compatible with the present analog trigger. A 3-in-1 card can provide analog signal to the L1 calorimeter trigger system (L1Calo). If inserted into the ATLAS detector before the HL-LHC upgrade, the Demonstrator will provide analog trigger sums to the L1Calo system.

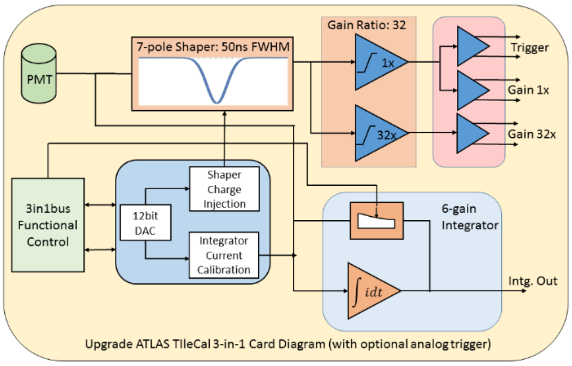


Figure 2.9: Functionality of 3-in-1 card for the upgrade of the TileCal detector.

The 3-in-1 MainBoard circuit (Figure 2.10) is divided in four sections each controlled by an Altera Cyclone IV FPGA. A section contains the required circuitry to control and read out three PMTs for a total of twelve PMTs per MainBoard. Each FPGA controls three dual-channel ADCs for digitizing the PMT signals at 40 Msps, six DACs for control the bias voltage levels applied to the ADC inputs and three ADCs for sampling the integrators at 50 kSps. All the control and data lines are routed to the DaughterBoard via the FMC connector. The Cyclone FPGAs are accessed from the DaughterBoard via an SPI interface, while digitized PMT signals are sent directly from the ADCs to the DaughterBoard using LVDS lines at 560 Mbps. Also two I^2C buses (one per side) are dedicated for the read out of the integrator ADCs.

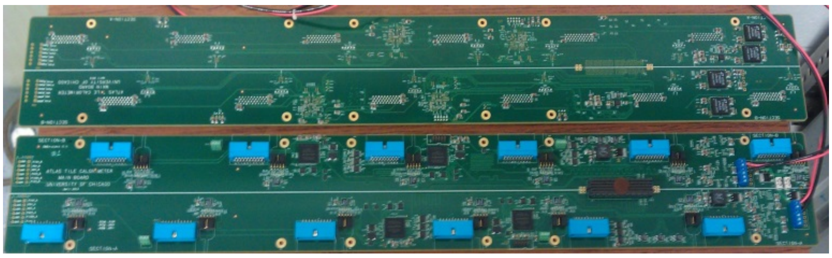


Figure 2.10: Picture of both sides of the MainBoard for the 3-in-1 FEB option.

In the same way as the DaughterBoard, this MainBoard is divided in two halves called A and B sides. Each side has its own power distribution, where the Schottky diodes connecting both sides prevent power failures in case of malfunctioning of one of the fLVPS bricks. Even if one side of a minidrawer fails completely, all PMTs on the opposite side can still be read out. The steel structure of the TileCal modules acts as a good radiation shield, where the end of the module close to the patch panel is exposed to a higher rate of radiation. A simulated map of the radiation dose for the ATLAS is shown in Figure 2.11. Based on this map, the voltage regulators and FPGAs were placed where the radiation is lower.

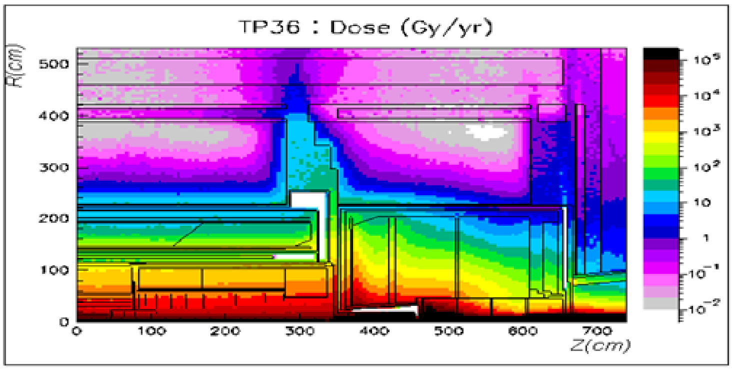


Figure 2.11: Simulated radiation dose in ATLAS after 100 fb^{-1}, being 1/40$^{\text{th}}$ of the total integrated luminosity expected for the HL-LHC [27].

QIE FEB

The core of the second FEB design is a Charge (Q) Integrator and Encoder (QIE) chip [28]. This custom ASIC digitizes the analog PMT signals with a constant resolution and no dead-time, covering a dynamic range of about 18 bits. In opposition to the other two FEB designs, the QIE does not perform any pulse shaping, but integrates the PMT current for every tick of the LHC clock so pileup-related noise is reduced.

Figure 2.12 depicts a block diagram of the main blocks of the QIE. The first stage of the QIE consists of a current splitter dividing the PMT current into fixed fractions. Then the output of the splitter is time-multiplexed between four gated integrators at 40 MHz and digitized with a flash ADC. The total acquisition time of the QIE corresponds to a latency of four clock cycles due to its pipelined operation. In addition, the QIE includes a fixed-threshold Time to Digital Converter (TDC) which is used to measure the time position of rising edge of the PMT pulses. The QIE FEB includes a calibration circuitry to calibrate the system with a Cesium source and current injection. The QIE outputs data through 8 LVDS outputs at 80 Mbps which constitutes of a 9-bit floating point word for the digitized charge, 2 bits to identify the gated integrator, and 5 bits for the TDC data.

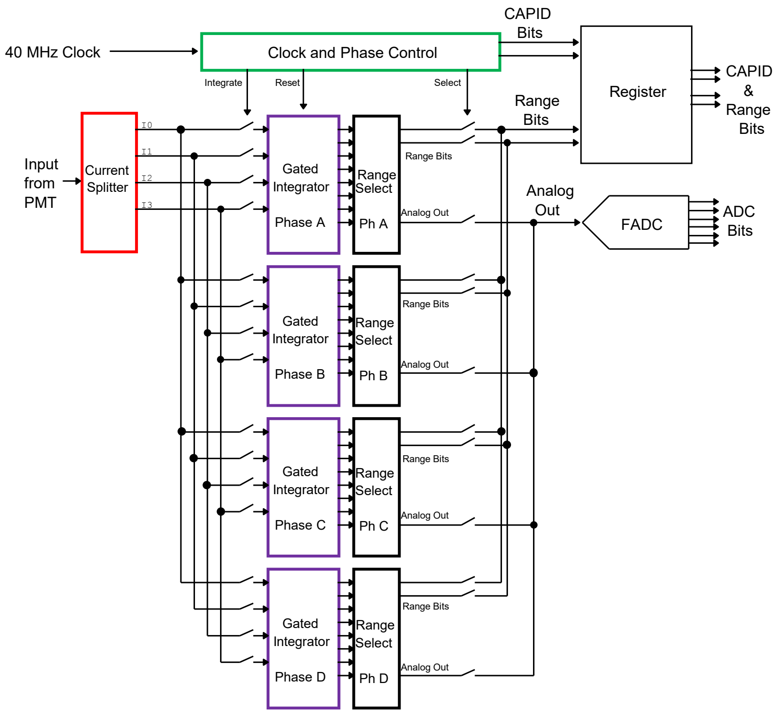


Figure 2.12: Block diagram describing the operation of the main modules of the QIE chip [27].

The QIE MainBoard is the least complex of the three types of MainBoards. It handles point-to-point LVDS signals for controlling purposes and to read out the QIE FEBs. Due to the limited number of pins in the FMC connector of the DaughterBoard v4, the MainBoard includes CPLDs to multiplex the SPI bus between the DB and the FEBs required for the control of the FEBs.

FATALIC FEB

The third FEB design relies on an ASIC called the Front end for ATLAS TileCal Integrated Circuit (FATALIC) [29]. FATALIC includes a multi-gain current conveyor which splits the input signal into three ranges with different gains (1, 8, 64) covering the full dynamic range of the PMT signal. Each current conveyor output is followed by a shaper and the readout chain is completed with a 12-bit ADC operating at 40 Msps. The FATALIC chips transmit two gains: the internal logic performs the auto-selection between high and low gain while the medium gain is always transmitted. In addition, FATALIC also includes a slow integrator circuit to measure the minimum bias current of the PMT during the operation and to calibrate the detector with a Cesium source. The circuitry for the CIS calibration is located in the FEBs.

The FATALIC MainBoard is based on the 3-in-1 MainBoard including four Altera Cyclone IV. Each FPGA is associated to three channels and serializes the parallel data provided by the FATALIC FEBs, transmitting the result to the DaughterBoard through the FMC connector. In addition, the MainBoard also provides the clock to the FEBs, and interfaces with the DaughterBoard to receive the configuration commands.

2.2.2 Power supplies

Low Voltage Power Distribution

The low voltage power is distributed to the front-end electronics using a three-stage power distribution system. The upgraded low voltage schema is largely based on the current version, due to the reliable operations of the current power supplies.

The 200 V power supplies installed in USA15 racks distribute power to the finger Low Voltage Power Supplies (fLVPS) [30] [31] located in the extreme end of each module. Each fLVPS includes 8 buck converters designed with COTS components, called bricks, to deliver 10 V to the MainBoards and DaughterBoards. Each minidrawer is powered with two bricks for double-redundancy, using the OR-diode circuit in the MainBoard. Extra effort has been made to make the fLVPS bricks radiation-tolerant with special focus on SEU. The fLVPS bricks are controlled and monitor through the DCS system.

The Point Of Load (POL) regulators of the front-end electronics comprise the third stage of the LV power distribution system. The POL regulators convert 10 V to the required voltage for the different electronic components. The POL regulators were selected to provide low-noise and were qualified for the operation with the TileCal radiation levels.

High Voltage Power Distribution System

The High Voltage Power distribution System (HVPS) controls and monitors the voltages applied to the almost 10,000 PMTs via the DCS system. The TileCal community is developing two different approaches for the high voltage distribution: the HV remote [32] and the HV internal [27]. Both approaches have in common that the high voltage power supplies are placed away from the detector in USA15. The difference is the location of the high voltage regulation and control circuits.

HV remote

In this approach, the control and monitoring electronics will be located away from the detector, in USA15, and each PMT will receive high voltage independently via two long wires. Individual wires will be combined into cables. This implementation is shown in Figure 2.13.

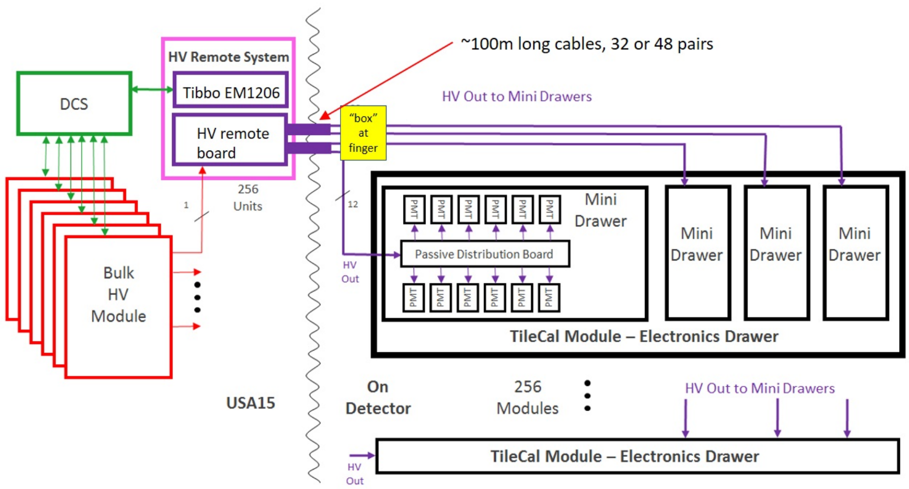


Figure 2.13: Block diagram of the remote HV power distribution system [27].

The high voltage control circuit of the remote HVPS is an improved version of the currently used HVPS during Runs 1 and 2. The first version is capable of delivering HV to groups of 12 channels corresponding to an entire minidrawer where each channel could be controlled individually.

Continuing with the developments of the HV remote system, the local electronics boards used to control and monitor voltages will be replaced with commercial computers that interface with the HV remote system through Ethernet. The second version of the HV remote system will be able to provide high voltage to 24 channels per high HV board, for a total of 512 boards for the complete detector.

One of the advantages of the HV remote system is that no radiation tolerant electronics is needed and the access to the HV boards for maintenance will be easy since the electronics will be located in USA15. The disadvantage is that the system needs almost 10,000 long wires.

HV internal

The HV internal system implements a different schema where the high voltage is sent directly to each module through a common high voltage cable. In the front-end electronics, each DaughterBoard is connected to one HVOpto board that regulates and monitors the voltage applied to 12 PMTs. Figure 2.14 shows a block diagram of the HV internal system.

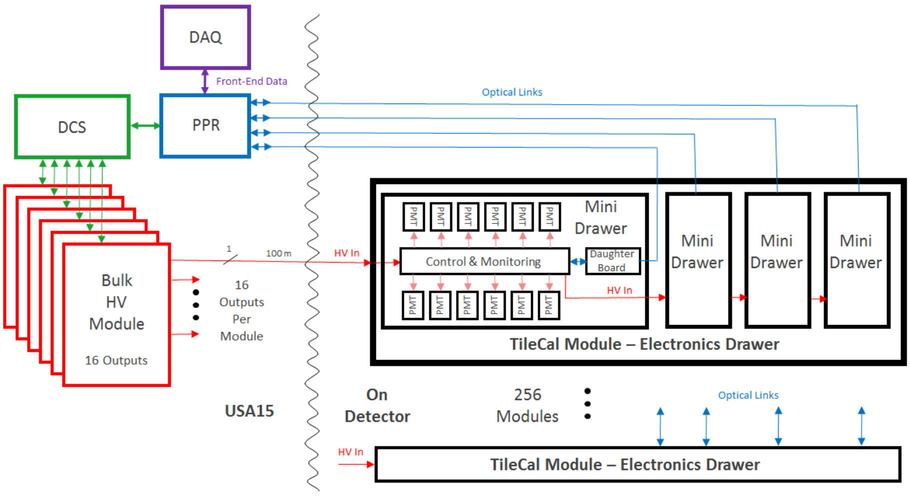


Figure 2.14: Block diagram of the internal HV power distribution system [27].

The HV bulk power supply in the counting rooms provides high voltage to four minidrawers in parallel through a single coaxial cable. The core of the HV Opto board is a Maxim Integrated MAX1329 chip which features 16 multiplexed analog inputs connected to an ADC, 2 DACs and GPIOs. The DCS system sets the high voltage individually for each PMT by transmitting commands to the DaughterBoards through the TilePPrs. The DaughterBoards receive and store the applied voltages digitized by the ADC of the MAX1329 chip. The MAX1329 chips are read out through an SPI interface. The DaughterBoards collect the monitoring data and transfers it to the DCS system through the TilePPr.

The advantage of the HV internal option is the reduction in the number of high voltage cables (where only one per four minidrawers is needed), at the expense of a more difficult maintenance of the HV system due to the limited access to the detector.

Active dividers

The passive HV dividers employed to distribute the high voltage to the PMT dynodes were redesigned to fulfill the HL-LHC requirements. The legacy HV dividers are implemented with a resistive network that provides non-linearities below the 1% with the small anode currents generated with the current luminosity. The new HV dividers [33] were designed with active components (transistors) to provide a constant gain independently of the anode current at the HL-LHC where the anode currents will be larger for some cells due to the higher pulse rates.

2.2.3 Back-end electronics

The upgraded back-end electronics system will be, as the current version, located in USA15 racks, 70 meters away from the detector. The Phase II Tile back-end electronics consist of two different systems: the Tile PreProcessor modules and the Trigger and DAQ interface (TDAQi) boards. The Tile back-end electronics system is based on the Advanced Telecommunications Computing Architecture (ATCA) specifications [34]. The ATCA framework provides a commercially and standardized platform for high-speed serial interconnects on the backplane supporting different I/O interfaces.

Tile PreProcessor module

The Tile PreProcessors [35] will be first and main element in the back-end electronics. It will be responsible for the reception and processing of the digital data coming from the TileCal modules. They will also distribute the DCS and TTC information for synchronization with the LHC clock to the front-end electronics.

The TilePPr modules will transmit selected data, integrator data and DCS information to the FELIX system. It will also provide reconstructed energy and time per cell to the TDAQi boards. On the other hand, the FELIX system will transmit the LHC clock, TTC commands and DCS configuration to the TilePPr modules to distribute it to the on-detector electronics.

The TilePPr module will be designed as a full size ATCA blade following the ATCA specifications, where the interfaces with the other ATCA boards in the same shelves will be achieved through three backplane connectors in locations called Zone 1 to 3.

- Zone 1 connector provides slow control paths for the shelf management and the power connection.
- Zone 2 connector routes the different data paths between the TilePPr module and the different ATCA blades connected in the same shelf.
- Zone 3 connector provides high-speed point-to-point connections to QSFP connectors in the TDAQi to communicate with the FELIX system and to the PreProcessing Trigger (PPT) FPGA.

The TilePPr module will be composed of an ATCA carrier board with four Advanced Mezzanine Card (AMC) [36] slots to host the Compact Processing Modules (CPM). The ATCA carrier will provide power to the CPMs, as well as, the basic interfaces for the communication with other systems through the backplane.

The CPMs will be designed with a single AMC form factor and will be populated with one FPGA and high-speed optical modules to implement all the required functionalities. The FPGA and optical modules will be selected to provide the CPM with the capability to read out and operate up to 8 minidrawers (two of the current TileCal modules). Therefore 32 TilePPr modules will be required for the complete readout of the TileCal detector.

During the operation, the TilePPr modules will distribute LHC clock, TTC commands and DCS configuration to the front-end electronics. Furthermore, the CPM FPGAs in the TilePPr module will compute the reconstructed energy and time per cell and bunch crossing, transmitting them to the TDAQi board. At the same time, the CPM FPGAs will store the received samples in pipelined memories until the reception of a L0/L1 acceptance signal. When this happens, the selected data will be extracted from the memories, formatted and transmitted to the FELIX system. Figure 2.15 presents a block diagram of the TilePPr and TDAQi boards for the Phase II Upgrade.

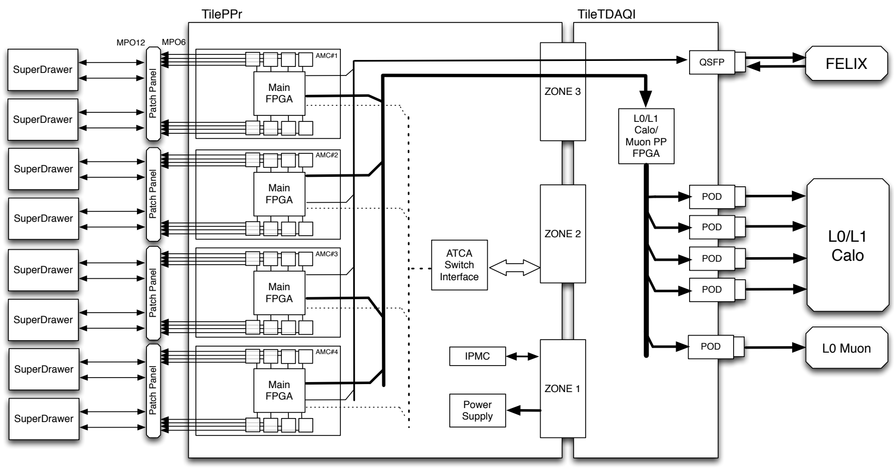


Figure 2.15: Block diagram of the final TilePPr and TDAQi designs.

Tile PreProcessor prototype

The TilePPr prototype is the first iteration of the final TilePPr module. It is the main element of the back-end electronics system in the Demonstrator project, providing compatibility with the upgraded front-end electronics system and the current DAQ system. It is capable of operating up to four minidrawers (one complete TileCal module), and therefore represents one eighth of the final design.

The first prototype includes all the components required to receive and process data from the Demonstrator module, as well as to decode and distribute

TTC signals to the front-end electronics for configuration and synchronization with the LHC clock. It also interfaces with the DCS system to control and monitor the high voltage distribution to the PMTs.

Furthermore, this prototype serves as a testbench for the development of trigger pre-processing algorithms that will be implemented in the TDAQi board after its installation in the HL-LHC.

The core processing of the TilePPr prototype relies on two high-performance FPGAs connected to four QSFP optical modules. The TilePPr prototype was designed as a double mid-size AMC board that can be operated in an ATCA carrier or in a μTCA shelf. Chapter 3 is devoted to the TilePPr prototype design, describing it in detail, and Chapters 4 and 5 cover the integration and operation of the TilePPr within the Demonstrator module.

Trigger and DAQ interface

The Trigger and DAQ interface [37] board will be the interface between the TilePPr module and the ATLAS TDAQ system. The TDAQi will be designed as an ATCA Rear Transition Module (RTM) [38] and will be powered and operated from the TilePPr module through the Zone 3 connectors.

The PPT FPGA in the TDAQi will compute trigger objects with different granularity and energy resolution with the data provided by the TilePPr modules. The trigger data will be transmitted to the trigger systems through the optical links using a protocol with low, fixed and deterministic latency. In addition, the TDAQi will provide a point-to-point path between the TilePPr module and the FELIX system through a QSFP module placed in the TDAQi board.

Chapter 3

Design of the TilePPr prototype

The TilePPr will be the first element and the main readout component of the back-end electronics in the Tile Calorimeter after the Phase II Upgrade. It will also provide the sampling clock and the configuration to the front-end electronics. This chapter gives a detailed description of the design of the TilePPr prototype for the Demonstrator project. The system requirements, component selection, PCB layout design and hardware test verifications are covered in this chapter.

3.1 Specifications of the TilePPr prototype

The core of this thesis is the design of the first prototype of the TilePPr for the HL-LHC. The designed prototype is a key element in the Demonstrator project that aims to validate the proposed readout architecture for the Phase II Upgrade, as has already been discussed in Chapter 2.

The TilePPr prototype represents a slice of the final TilePPr system, reading out one complete Demonstrator module. The TilePPr prototype was used for the readout and operation of the three different front-end board options (3-in-1 cards, QIE and FATALIC) during three testbeam campaigns. More details about the performance and functionalities of the TilePPr prototype during the testbeam campaigns will be presented in Chapter 6. In addition, this prototype is envisaged to be included in the current DAQ architecture to read out and operate the Demonstrator module that will be inserted into the ATLAS experiment before the Phase II Upgrade. When integrated within the DAQ architecture, the TilePPr prototype will store the PMT digital samples in pipelines at the LHC frequency. After reception of a L1A signal, selected data will be transferred to the RODs with the appropriate format. Therefore, the Demonstrator module will be transparent to the ATLAS DAQ system emulating the current front-end electronics functionalities.

The tasks in charge and specifications that the TilePPr prototype has to fulfill as part of the Demonstrator project are listed below.

- Readout and operation of one TileCal module with the Phase II front-end electronics.
- Storage of the digital samples in pipeline buffers.
- Data formatting and transmission to the current RODs.
- Synchronization of the front-end and back-end electronics with the LHC clock provided by the legacy TTC system through data links with fixed and deterministic latency.
- Communication through Ethernet for slow control functionalities.
- Implementation of signal processing algorithms for energy and time reconstruction.
- Communication with the upgraded trigger systems sending pre-processed data for the trigger decision.
- Communication with the FELIX system.

3.2 Components and functionality

The TilePPr prototype was designed to fulfill all the functional requirements described above. Its components were selected according to the hardware specifications for the front-end electronics and the overall ATLAS Trigger and DAQ systems for the HL-LHC.

Figure 3.1 shows a block diagram the main components and communications paths of the TilePPr prototype.

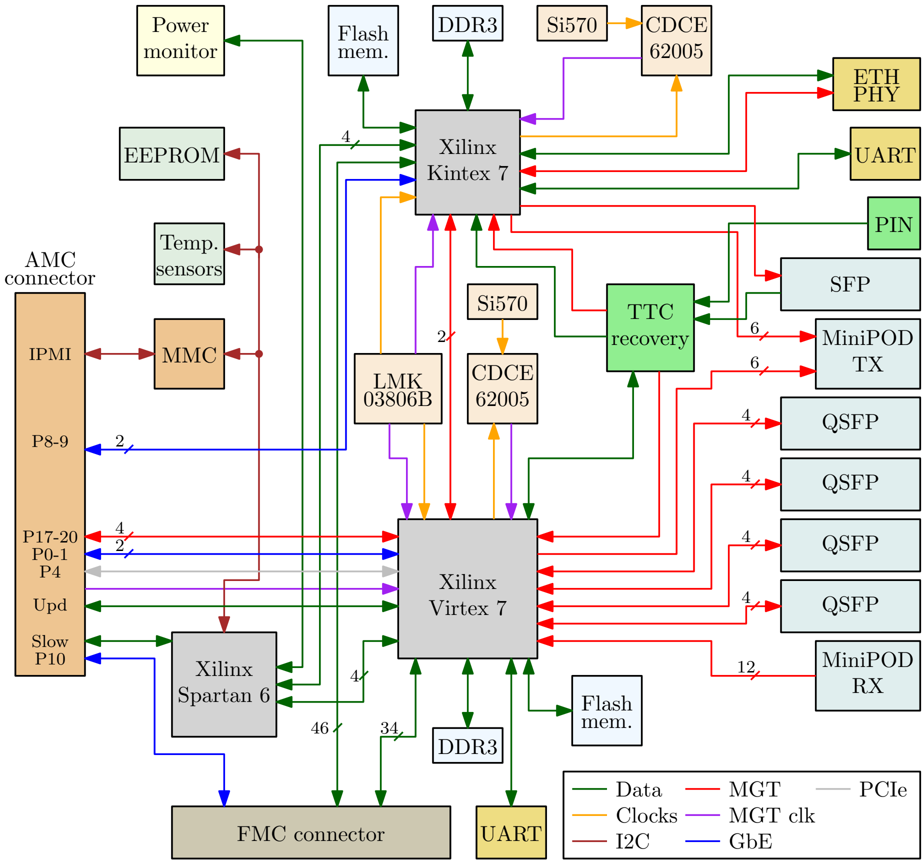


Figure 3.1: General block diagram of the TilePPr prototype.

The following subsections provide a detailed description of the selected components and functionalities.

3.2.1 Field Programmable Gate Arrays

The first components selected were the FPGA devices. At least two FPGAs were needed in the TilePPr prototype: one for the readout of the Demonstrator module and one for the communication with the trigger systems. The requirement of having a high-speed readout data path with deterministic and low latency made the use of high-performance FPGAs with embedded transceivers mandatory. Xilinx series 7 FPGAs [39] complied with all the requirements and were chosen for this reason.

The selection of the FPGAs was based on the number of transceivers and logic capabilities, resulting in the selection of a Xilinx Virtex 7 for the operation with the front-end electronics and a Xilinx Kintex 7 for the communication with the trigger systems. Since many of the auxiliary components such as clock distribution circuitry and power modules are shared between the two FPGAs, a Xilinx Spartan 6 FPGA was included in the design for configuration and monitoring.

Readout FPGA

The Readout FPGA is the core processing element of the TilePPr prototype. The Readout FPGA is in charge of the readout and operation of the Demonstrator module, interface with the FELIX system, synchronization of the front-end electronics with the LHC clock and interface with the Trigger FPGA. The selected FPGA device for the implementation of the Readout FPGA task is a Xilinx Virtex 7 XC7VX485T. It contains a large number of logic and DSP resources and 48 high-speed transceivers capable of operating at 10.3125 Gbps. The TilePPr prototype was also designed to be pin-to-pin compatible with other FPGA model: the Xilinx Virtex 7 XC7VX415T. Both FPGA models contain similar resources, with the main difference being in the type of high-speed transceivers. Table 3.1 summarizes the resources of the pin-to-pin compatible Virtex 7 FPGAs for the TilePPr prototype.

		XC7VX415T	**XC7VX485T**
Logic Cells		412,160	485,760
CLBs	**Slices**	64,400	75,900
	Distributed RAM (Kb)	6,525	8,175
DSP Slices		2,160	2,800
Max RAM (Kb)		31,680	37,080
CMTs		12	14
PCIe Gen2 blocks		0	4
PCIe Gen3 blocks		2	0
GTX transceivers		0	48
GTH transceivers		48	0
Available User I/O		350	350

Table 3.1: Summary of resources of the selected Virtex 7 FPGAs.

The XC7VX415T includes GTH transceivers supporting rates of 9.6 Gbps while the XC7VX485T contains GTX transceivers which are not designed to operate at 9.6 Gbps in a gap from 8 Gbps to 9.8 Gbps. This limitation in the data rate of the GTX transceivers is driven by the frequency range of the dedicated Phase Locked Loops (PLL) in the transceivers. However, as will be discussed in Chapter 4, the GTX transceivers can be operated out of the manufacturer specifications achieving a stable and reliable communication at 9.6 Gbps.

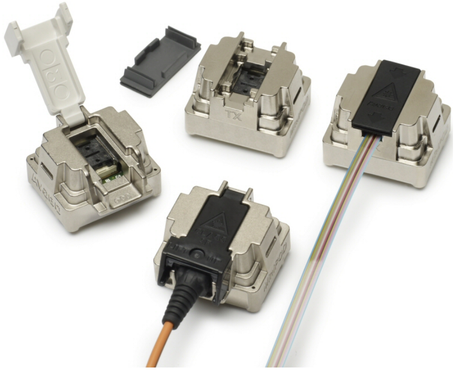
As already mentioned in Chapter 2, the DaughterBoard includes two QSFP modules for the transmission of digital data to the TilePPr prototype. Only one QSFP module is connected to the TilePPr prototype, while the second redundant QSFP is reserved in case of malfunctioning of the first QSFP. Therefore, 16 transceivers of the Readout FPGA are routed to four QSFP modules (Figure 3.2 (a)) providing a maximum bidirectional bandwidth of 160 Gbps with the front-end electronics. Moreover, another set of 12 transceivers are routed to an Avago MiniPOD receiver (Figure 3.2 (b)) [40] for the evaluation of other technologies and testing purposes.

In order to implement the interface with the FELIX system, four transceivers were routed directly to the AMC backplane connector providing point-to-point communication with the TDAQi board through the Zone 3 connector of the ATCA carrier. The FELIX interface path provides an aggregate bandwidth of 40 Gbps between the Readout FPGA and the FELIX system.

Another four-transceiver set is used for the data path between the Readout and Trigger FPGAs. The Readout FPGA will use this interface path to send the reconstructed cell energies and time to the Trigger FPGA. The Readout FPGA is also connected to 6 transmitters of an Avago MiniPOD transmitter to evaluate a different approach where the Readout FPGA can transmit directly the pre-processed data to the trigger system reducing the overall latency.

Finally, two GbE ports and one PCIe port are routed to the AMC backplane connector for the remote operation of the Readout FPGA. These ports will be used to control and configure the Readout FPGA through the IPBus ports and will provide remote programming capabilities.

(a) Luxtera QSFP module.



(b) Avago MiniPOD RX.

Figure 3.2: Optical modules employed for the high-speed communication paths in the TilePPr prototype.

Trigger FPGA

The main purpose of the Trigger FPGA is the evaluation of trigger algorithms and study of the latency for data transmissions between the Readout and the Trigger FPGAs. As introduced in the Chapter 2, in the final version of the readout electronics for the HL-LHC, the Trigger FPGA will be located in the TDAQi that will also provide communication path with the FELIX and trigger systems.

In the TilePPr prototype the selected Trigger FPGA is a Xilinx Kintex 7 XC7K420T. This FPGA model contains high-density logic and DSP resources to implement the algorithms, and 28 transceivers for the high-speed communication with the FELIX and trigger systems. Table 3.2 summarizes the logic resources and transceivers contained in the selected Kintex 7 FPGA.

Half of the channels of the Avago MiniPOD transmitter are connected to six transceivers of the Trigger FPGA for the evaluation of the communication with the trigger systems. The Trigger FPGA can transmit at a maximum aggregated bandwidth of 60 Gbps through the Avago MiniPOD module (10 Gbps per lane).

In addition, four transceivers are used for the transmission of the cell energy and time from the Readout FPGA to the Trigger FPGAs. This communication path will also be employed to evaluate different data protocols which minimize the latency between the two FPGAs in the final design.

		XC7K420T
Logic Cells		416,960
CLBs	**Slices**	65,150
	Distributed RAM (Kb)	5,938
DSP Slices		1,680
Max RAM (Kb)		30,060
CMTs		8
PCIe Gen2 blocks		1
GTX transceivers		28
Available User I/O		380

Table 3.2: Summary of resources of the selected Kintex 7 FPGA.

Finally, two additional transceivers provide remote operation and programming capabilities through the AMC backplane connector using the GbE protocol. A RJ45 connector placed in the front-panel provides Ethernet connection for local operation. The Ethernet interface is implemented using a Marvel 88E1111E PHY controller that allows the selection between 10BASE-T, 100BASE-TX or 1000BASE-T protocols.

Slow Control FPGA

The Slow Control (SC) FPGA is used for the monitoring and configuration of all the components in the TilePPr prototype. The selected FPGA is a Xilinx Spartan 6 XC6SLX16 [41] which interfaces with the Trigger and Readout FPGAs, clocking circuitry, power monitoring circuit, all optical modules, on-board sensors and with the ATCA system through the Module Management Controller (MMC) [42]. Table 3.3 summaries the logic and block resources of this FPGA.

		XC6SLX16
Logic Cells		14,579
CLBs	**Slices**	2,278
	Distributed RAM (Kb)	136
DSP Slices		32
Max RAM (Kb)		576
CMTs		2
Available User I/O		160

Table 3.3: Summary of resources of the selected Spartan 6 FPGA.

The protocol employed for communication with the majority of the on-board components is I^{2}C. Exceptions are the power monitoring circuit which uses PMBus protocol, the jitter cleaners which use Serial to Parallel Interface (SPI) protocol and the communication between the SC FPGA and the Trigger and Readout which is implemented with a custom serial protocol.

In the TilePPr prototype there are two separated I^{2}C chains as shown in Figure 3.3. The first I^{2}C chain contains the MMC, temperature sensors (MCP9808), an I^{2}C GPIO expander chip (PCA6416A), an EEPROM memory (24AA32A) and the SC FPGA. In this I^{2}C chain, the MMC works as I^{2}C master reading the data from the temperature sensors and monitoring data contained in registers in the SC FPGA. Upon a user request, the MMC can also extract the TilePPr ID number from the EEPROM memory or remote reset the FPGAs through the I^{2}C GPIO expander chip.

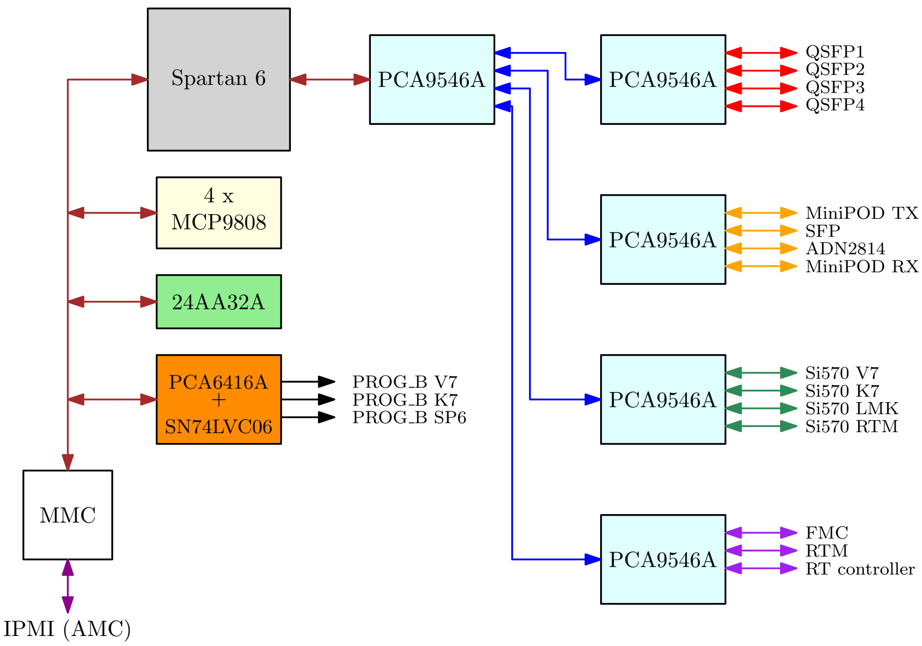


Figure 3.3: Block diagram of the I^{2}C chains in the TilePPr prototype.

The second I^{2}C chain connects the SC FPGA with the rest of the components in the board. In this I^{2}C chain the SC FPGA is the master device reading the status and configuring the following components:

- Clock distribution and generation circuitry: clock generators (LMK03806B), and programmable oscillators (Si570).
- Optical modules: QSFPs, SFP and Avago MiniPOD modules.
- TTC recovery circuitry (ADN2814).
- External boards: Rear Transition Modules and FMC boards.
- Real time controller chip.

I^2C switches (PCA9548A) were included to reduce the complexity of the routing between the SC FPGA and the I^2C slaves. In addition, I^2C switches handle any communication conflict when two or more I^2C slaves have the same address.

The SC FPGA permits complete monitoring and basic operation of the TilePPr prototype from the ATCA framework through the MMC board. The MMC is a small mezzanine card included in the TilePPr prototype which implements the Intelligent Platform Management Interface (IPMI) to manage the power connection to the ATCA system and remote operation of the AMCs. Figure 3.4 shows a picture of the MMC card v3.5 used in the TilePPr prototype.

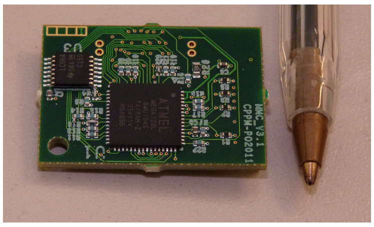


Figure 3.4: Picture of the MMC card.

3.2.2 TTC receiver block

The TTC receiver block is needed for synchronization of the TilePPr prototype and front-end electronics with the legacy TTC system. This block is composed of two Analog Devices ADN2814 chips which extract the clock and data from the TTC stream and distribute them to the Readout and Trigger FPGAs.

The TTC signal can be received through two different paths: a standard SFP connector or an ST-connectorized photo-diode. Both connectors should not be operated at the same time, and the selection between the SFP and the photo-diode is done with on-board resistors and capacitors. The output of the selected optical connector is then routed to an ON Semiconductor NB6B14S chip. The latter is a differential buffer which repeats the data to two different ADN2814 chips for the clock and data extraction.

In addition, the NB6B14S chip also buffers the TTC signals to two transceivers (one in the Trigger FPGA and one in the Readout FPGA). This latter option permits the implementation of clock and data extraction in the FPGAs using the transceiver resources.

Figure 3.5 shows a block diagram of the circuitry used for the extraction of the TTC clock and data.

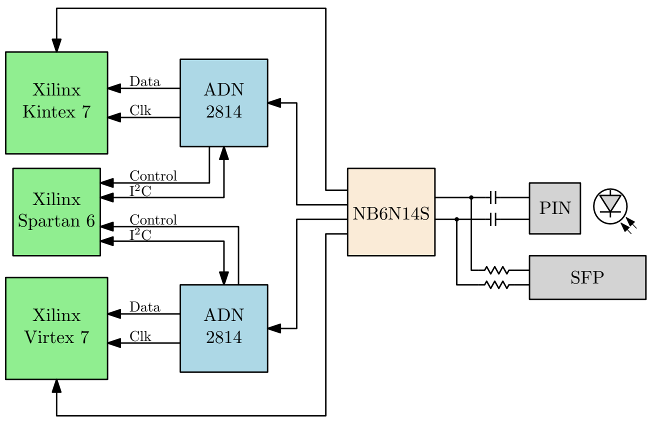


Figure 3.5: Block diagram of the TTC receiver block and its connections with the Readout, Trigger and SC FPGAs.

3.2.3 Clocking unit

The selection of the clock distribution components is one of the most important design choices because the reference clock for the transceivers requires high quality and very low jitter. The selected clocking unit provides all the clocks needed for the operation of the TilePPr prototype.

The use of high-speed transceivers synchronized with the LHC clock requires high-performance jitter cleaners, such as the CDCE62005 chip from Texas Instruments, to meet the transceiver specifications in terms of jitter. The jitter cleaners are used to clean the recovered LHC clock from the TTC receiver block and to route it to the transceivers.

The TilePPr is equipped with two CDCE62005 chips connected to the Trigger and Readout FPGAs. Each CDCE62005 chip has two selectable clock inputs and 5 clock outputs. One clock input is connected to a programmable local oscillator (SI570) and the second one is connected to the recovered LHC clock. All the clock outputs were routed to the FPGA banks in such a way that all the interfaces can be configured synchronous with the LHC clock.

The CDCE62005 chips can be programmed and controlled via the SC FPGA or through the Trigger and Readout FPGAs using level shifter chips to adapt the voltage levels between the FPGAs and the CDCE62005. The operation of the CDCE62005 chips to synchronize the TilePPr with the LHC clock will be discussed in detail in Chapter 5.

Also, a clock generator, a Texas Instruments LMK03806B chip was included in the design to provide low noise clocks for the PCIE and GbE communication channels with the ATCA carrier. The LMK03806B chip has 14 programmable clock outputs, half of them connected to the Trigger FPGA and the other half to the Readout FPGA.

3.2.4 Configuration

All FPGAs in the TilePPr prototype can be configured using either with a JTAG chain or by loading a configuration file directly from non-volatile memories. The Trigger and Readout FPGAs are connected to Byte Peripheral Interface (BPI) flash memories (Micron PC28F00AG18F). BPI memories provide initial configuration of the FPGAs during the power-up sequence. The selected BPI memories have enough space to be segmented into pages to contain different configuration files which can be updated remotely [43]. In addition, one of the advantages of the BPI memories is the reduced access time, thus reducing the time to re-write the memory and load the configuration into the FPGAs. However, the SC FPGA is connected to a 128 Mb SPI flash memory (Micron N25Q128) since the size of the configuration files is much smaller and a parallel interface is not required.

An on-board Digilent JTAG SMT2 programming module configures all the FPGAs through the JTAG chain. This programmer can connect via the front-panel through a microUSB connector. A second standard through-hole connector is provided for an external JTAG programmer. The configuration mode of all the FPGAs can be selected using on-board switches so that the configuration files are loaded from the local memories or through the JTAG chain.

Figure 3.6 shows all the programmable devices connected to the JTAG chain. The three FPGAs and the FMC connector are connected to the same JTAG chain through level shifter chips to adapt the voltage levels between the FPGA and the Digilent programmer. In case an FPGA is not present or cannot be accessed through the JTAG port, it has to be bypassed to allow the communication with the rest of the devices. This is achieved by connecting the corresponding TDI and TDO ports with the 0 Ω resistors for the FPGAs, or with the switch for the FMC module.

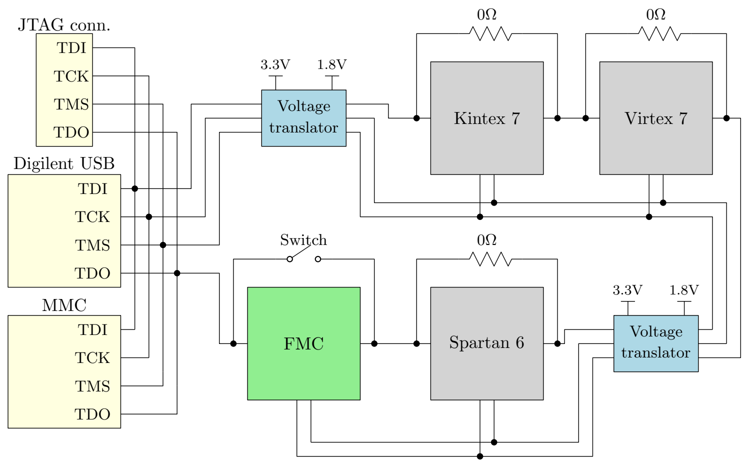


Figure 3.6: Block diagram of the TilePPr JTAG chain with the FMC connector and FPGAs.

3.2.5 Power distribution

One of the critical points during the design of the TilePPr prototype was the power distribution. The reduced area available on the board, the number of power consuming components, and the required voltages voltages made the design of the power distribution circuit challenging. In addition, voltage regulators powering the FPGA transceivers are required to have low noise to avoid any jitter contribution affecting to the quality of the high-speed signals.

Regulator Model	**Voltage (V)**	**Imax (A)**	**Power rail**	**Device**
2 x LTM4627	1.0	30	VCCINT	Virtex7, Kintex7
LTM4627	1.0	15	MGTAVCC	Virtex7, Kintex7
LTM4601A	1.2	12	MGTAVTT	Virtex7, Kintex7
LTM4618	1.8	6	MGTVCCAUX	Virtex7, Kintex7
LTM4628	3.3	8	P3V3	Clocking, sensors, I^2C
	2.5	8	P2V5	Ethernet, Kintex7
LTM4628	1.8	8	P1V8	Virtex7, Kintex7, flash memories
	1.5	8	P1V5	Virtex7, Kintex7, DDR3
LTM8029	5.0	0.6	P5V0_SP6	MIC2230
MIC2230	3.3	0.8	P3V3_SP6	Spartan6 IO Banks
	1.2	0.8	P1V2_SP6	Spartan6 core
ADP7102	5.0	0.3	P5V0	FICER photo-diode

Table 3.4: Summary of the power modules used in the TilePPr prototype indicating the operating voltage and the maximum current.

The input voltage of 12 V received directly via the AMC backplane connector when inserted into the ATCA shelf, or from an ATX power connector using a commercial ATX power supply. The power stage of the TilePPr is composed of a total of 10 voltage regulators: 8 switching regulators power the different power rails for the Trigger and Readout FPGAs, 1 switching regulator feeds the SC FPGA IO banks and core, and 1 linear regulator provides 5 V to the photo-diode of the TTC receiver block. Table 3.4 shows a complete list of the regulators constituting the power stage.

Following the manufacturer recommendations, ferrite beads were introduced in the transceivers power rails to keep the voltage ripple below 10 mV_{pp}. The output voltage ripple for all the regulators was simulated using the Linear Technology software LTSpice IV [44] confirming that the voltage ripple is kept within 10 mV_{pp}.

The power stage includes a protection circuit for monitoring the 12 V power input to prevent damage when powering the TilePPr prototype through the ATX power connector. Figure 3.7 shows a block diagram of the protection circuit, where a Linear Technologies LT4363 chip senses the input voltage and current consumption through the R_{Sense} resistor. Resistors R_1, R_2 and R_3 are used to configure the undervoltage and overvoltage levels. In case of any power deviations are detected, the LTM4363 chip opens the switch Q1 to protect the board.

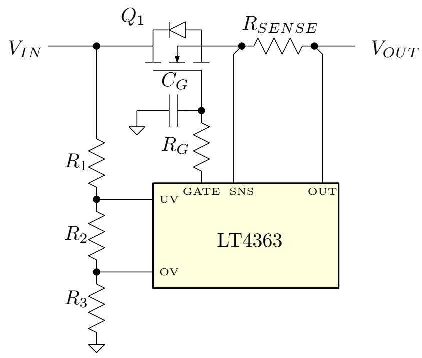


Figure 3.7: Block diagram of the protection circuit designed for the 12 V input.

Power monitoring circuit

A power monitoring circuit monitors all the voltages and currents of the power stage to identify hardware problems. Moreover, this circuit provides a better understanding of the power consumption requirements of the FPGAs in different scenarios, helping in the design of the final TilePPr.

The power monitoring circuit is implemented using two Linear Technologies LTC2974 chips, where each of them can measure the currents and voltages of up to four power rails. The first six power modules listed in Table 3.4 are connected to the power monitoring circuit.

The current delivered by the power regulators is measured through 500 $\mu\Omega$ sensing resistors connected in series between the power regulators and the power rails feeding the FPGAs. For an accurate measurement of the voltage applied to the FPGAs, sense lines connect the LTC2974 directly to power vias underneath the FPGAs. For both measurements, the input signals are conditioned with anti-aliasing filters to remove frequencies above 31.25 kHz. The SC FPGA reads out the measured values via the PMBus protocol.

3.2.6 Other components

FMC connector

The FMC connector interfaces the TilePPr prototype with other FMC cards expanding its functionalities or providing access to the FPGA IO banks for testing and debugging purposes. The FMC connector selected for the TilePPr prototype is a High Pin Count (HPC) connector from Samtec with 400 pins.

Only the Trigger and Readout FPGAs are connected to the FMC connector, where the Readout FPGA was routed to 34 differential pairs and the Trigger FPGA to 46 differential pairs. In addition, two high-speed links were routed to transceivers in the Trigger and Readout FPGAs and one high-speed link was directly connected to the AMC backplane connector.

The TilePPr prototype will also be employed as the core of the PROMETEO [45] system designed for the certification of the front-end electronics during maintenance campaigns. For this reason, the FMC pinout was designed to be pin-to-pin compatible with the PROMETEO ADC FMC board (Figure 3.8).

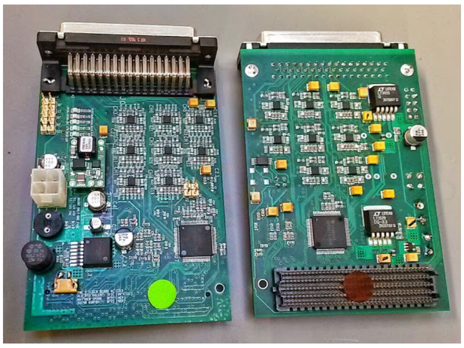


Figure 3.8: Picture of the ADC FMC board version 2 for the PROMETEO project.

DDR3 memories

DDR3 memories from Micron Technologies are connected to the Trigger and Readout FPGAs, where each FPGA will access up to 512 Mb. The DDR3 memories were added for evaluation purposes and to study the performance of the TilePPr using external memories to absorb the large quantity of data generated under high trigger rate situations.

USB-UART interfaces

The USB-to-UART bridges (Silicon Labs CP2103GM) are connected to the Trigger and Readout FPGAs for the implementation of local debug ports to check the status of the TilePPr in situ. Both debug ports can be accessed from the front-end panel through microUSB connectors and provide a maximum data rate of 1 Mbps using the Universal Asynchronous Receiver/Transmitter (UART) protocol.

3.3 Physical design and PCB layout

The TilePPr Printed Circuit Board (PCB) was designed as a double AMC form factor that can be operated either in a μTCA shelf or in an ATCA carrier. The PCB was designed following the AMC specifications [36] which defines the physical and mechanical dimensions, maximum allowable component height and the pinout of the connector. The total size of the PCB is 149 mm $\times$ 183.5 mm and it is divided in separate sections for the FPGAs, clocking circuitry, communication modules and power regulators. Figure 3.9 shows a picture of the TilePPr prototype.

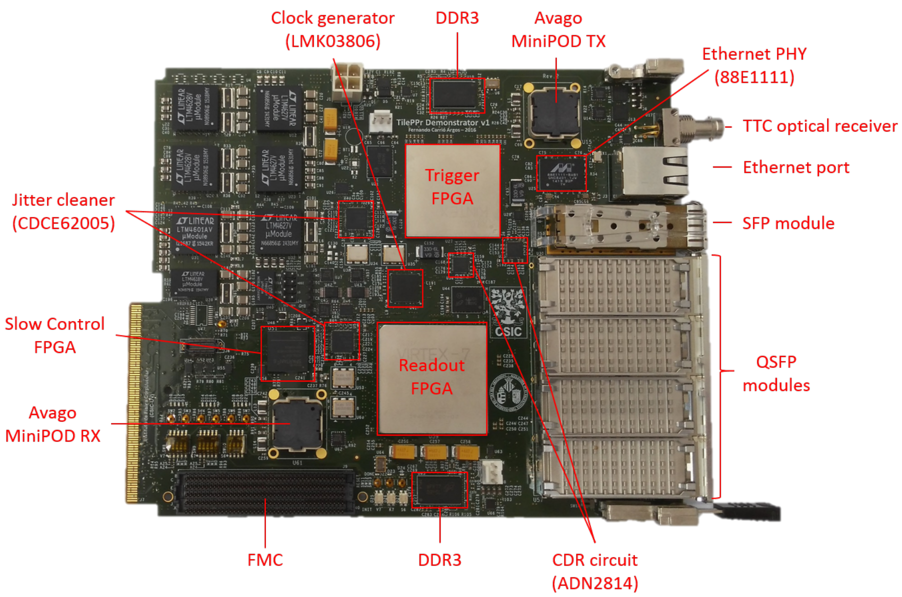


Figure 3.9: Picture of the TilePPr prototype indicating the main components.

3.3.1 Stack-up

The stack-up materials and layer thicknesses were selected to fulfill the high-speed design requirements. The selected stack-up counts a total of 16 layers used to implement the power rails and signal routing. Figure 3.10 depicts a sketch of the stack-up indicating the layer thickness and materials used.

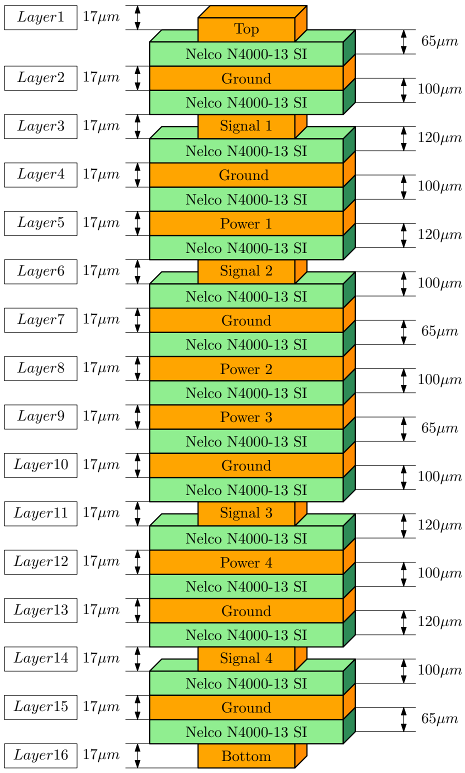


Figure 3.10: Sketch of the TilePPr stack-up.

Nelco N4000-13 SI was chosen as the dielectric material due to its low dielectric constant (ϵ_r) of 3.2 and a dissipation factor ($tan(\delta)$) of 0.008, both measured at 10 GHz for striplines. This material is widely used for high-speed designs since it offers very low dielectric losses at high frequencies.

The placement of the components required several iterations due to the large number of components and the limited number of layers. In addition, the signal routing congestion was minimized by an appropriate selection of the pins interfacing the FPGAs with the rest of the components.

The final layer distribution employed for the PCB design of the TilePPr is described below.

- Layers 2, 4, 7, 10, 13 and 15: continuous ground planes.
- Layers 5 and 12: continuous power planes.
- Layers 8 and 9: split power planes.
- Layers 3 and 14: high-speed lines for the QSFPs, Avago MiniPODs, FPGA high-speed connections and AMC backplane connections.
- Layers 1, 6, 11 and 16: clock lines, DDR3 lines and rest of slow control signals.

3.3.2 Signal integrity studies

Signal integrity simulations constitute a fundamental step during the design of high-speed communication devices. Simulations in a wide range of frequencies help to prevent interconnection problems prior to manufacturing.

Since the FPGA transceivers transmit at high data rates, the length of the high-speed interconnects are comparable to the wavelength of the traveling signals which behaves as transmission lines. The geometry and properties of the dielectric materials of the interconnects define the parameters of the transmission lines such as the characteristic impedance, propagation delay and dielectric and conductor losses.

High-speed interconnects have to be carefully designed since the noise budget can be compromised by impedance mismatches along the interconnect, interference from neighbor interconnects (crosstalk) or high losses degrading the signal amplitude.

Another important parameter in the design of high-speed interconnects is the bandwidth of the traveling signal. A high-speed interconnect has to provide a low attenuation path for all the frequencies within the bandwidth of the transmitted signal. Since digital signals have a large number of harmonics, the effective bandwidth of a digital signal is defined as the highest significant frequency component [46]. The effective bandwidth is related to the rise time of the digital signal. The mathematical expression, considering a rise time based on 20%-80% thresholds, is shown in Equation 3.1.

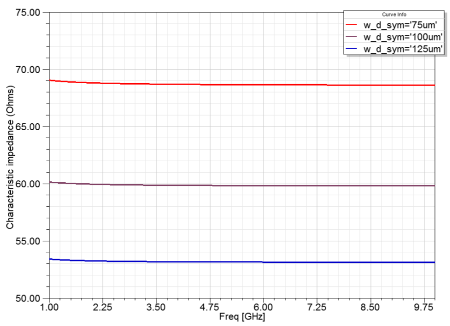
$$BW = \frac{0.23}{t_r} \tag{3.1}$$

where t_r corresponds to the rise time (20%-80%) of the signal and BW is the effective bandwidth.

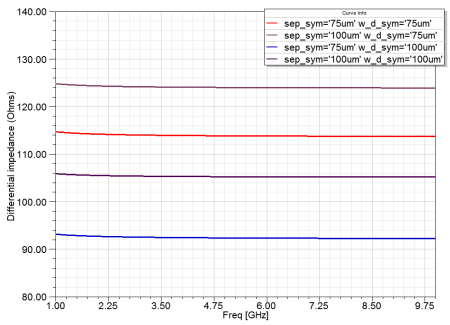
In the case of the TilePPr prototype, the high-speed transceivers contained in the Readout and Trigger FPGAs have a typical rise time of 40 ps, so according to Equation 3.1 the effective bandwidth is close to 6 GHz.

Pre-layout simulations

Prior to the routing of the PCB, pre-layout simulations were performed to define the geometry of the single-ended and differential traces. Single-ended traces were designed to provide a characteristic impedance (Z_o) of 50 Ω and differential lines to provide a differential impedance (Z_{diff}) of 100 Ω. A 2D field solver software, called ANSYS Q3D Extractor [47], was used to simulate multiple geometries with different trace width and separations between the differential traces in order to find the most suitable values. Figure 3.11 shows the results of the characteristic and differential impedance of the simulated microstrips for different combinations of trace widths and trace separation.



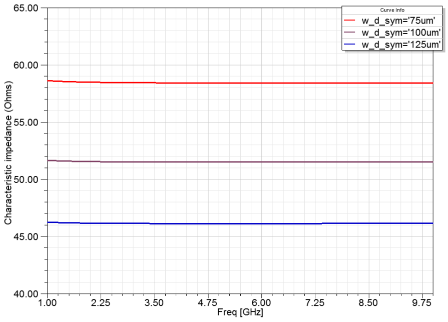
(a) Simulation of the Z_o for a single microstrip varying the trace width from 75 μm to 125 μm.



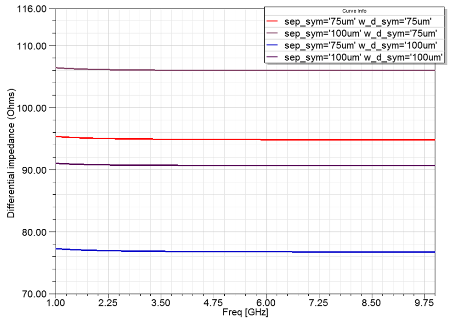
(b) Simulation of the Z_{diff} for a differential microstrip varying the trace width from 75 μm to 100 μm and the trace separation between the pairs from 75 μm to 100 μm.

Figure 3.11: Simulation of the impedance of microstrip structures.

A similar simulation was done to determine the geometry of the striplines. Figure 3.12 presents the characteristic and differential impedance of the simulated striplines.



(a) Simulation of the Z_o for a single stripline varying the trace width from 75 μm to 125 μm.



(b) Simulation of the Z_{diff} for a differential stripline varying the trace width from 75 μm to 100 μm and the trace separation between the pairs from 75 μm to 100 μm.

Figure 3.12: Simulation of the impedance of stripline structures.

Table 3.5 shows the selected values of width and trace separation for the microstrips and striplines. The geometry parameters of the microstrips and striplines were selected based on the simulation results, where the selected geometries provide impedance values within a 10% of the design constraint value.

	Microstrip		**Stripline**	
	Single	**Differential**	**Single**	**Differential**
Width	125 μm	100 μm	100 μm	75 μm
Separation	-	100 μm	-	75 μm

Table 3.5: Summary of the selected geometry values for the high-speed interconnects.

Impedance discontinuities

One of the most common source of problems which compromises the signal integrity are the impedance discontinuities along the high-speed interconnects [48]. Geometry variations along the traces produce reflections that degrade the signal quality at the receiver. Differential signal vias traversing layers, or the pads of the DC-coupling capacitors, are common sources of impedance mismatch in high-speed designs.

The proportion of the signal reflected back to the transmitter is proportional to the impedance mismatch and can be estimated by Equation 3.2.

$$\rho_d = \frac{Z_d - Z_o}{Z_d + Z_o} \tag{3.2}$$

where Z_d is the impedance of the discontinuity, Z_o the characteristic impedance of the line and ρ_d is the reflection coefficient.

The S-parameters

In this thesis, Scattering parameters (S-parameters) [49] were used to characterize and validate the designed high-speed interconnects. S-parameters describe, in the frequency domain, how the interconnections interact with incident sine waves. When an incident sine wave interacts with an interconnect, some part of the energy can scatter back from the interconnect and the other continues its propagation through the interconnect. Then, S-parameters offers a versatile way to extract the characteristics of the channel, as insertion loss, return loss or the amount of crosstalk between lines.

Figure 3.13 shows a representation of a 2-port network with the normalized wave definitions for S-parameters, where a represents the incident waves and b the scattered waves.

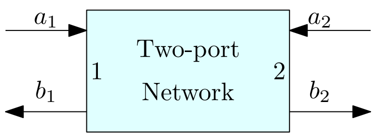


Figure 3.13: Recommended port labeling for an interconnection.

The value of the S-parameters represent the ratio of the amplitude between the incident and scattered waves. Equation 3.3 shows the definition of the S-parameters for the particular case of a 2-port network.

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \qquad S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \qquad S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \qquad S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{3.3}$$

For example, S_{11} quantifies the return loss (called before ρ_d in Equation 3.2) which corresponds to the portion of energy that is reflected back to the source, and S_{21} quantifies the insertion loss or, in other words, the portion of energy that is transferred to the receiver. The S-parameters are represented in decibels:

$$S_{ij}(dB) = 20 \cdot log_{10} \left(\frac{A_i}{A_j} \right) \tag{3.4}$$

where A_i and A_j correspond to the amplitude of the wave at ports i and j respectively, and S_{ij} is the value of the S-parameter between ports i and j.

The S-parameters can be extended to a n-port network to represent more complicated models with different high-speed lines. Equation 3.5 shows the matrix form of the S-parameters for a n-port network.

$$\begin{bmatrix} b_1 \\ b_2 \\ \vdots \\ b_n \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \dots & S_{1n} \\ S_{21} & S_{22} & \dots & S_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ S_{n1} & S_{n2} & \dots & S_{nn} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \\ \vdots \\ a_n \end{bmatrix} \tag{3.5}$$

where b_i, S_{ij} and a_j represent a generalization of the notation followed in Figure 3.13 and Equations 3.3 and 3.4.

The mixed mode S-parameters

The mixed-mode S-parameters are obtained from the S-parameters and describe the same concept as the S-parameters but considering differential- and common-mode signals. This form is more convenient for signal integrity analysis. Figure 3.14 shows a sketch of the port definitions for a 4-port network and its equivalent 2-port differential network.

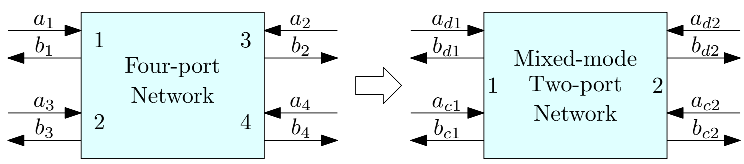


Figure 3.14: Representation of the S-parameters of a 4-port network (left) and the equivalent S-parameters of 2-port mixed-mode network (right).

As well as the S-parameters, the mixed-mode S-parameters can be represented in matrix form. Equation 3.6 shows the mixed-mode S-parameters corresponding to a 2-port differential network.

$$\begin{bmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{bmatrix} = \begin{bmatrix} \begin{bmatrix} S_{DD11} & S_{DD12} \\ S_{DD21} & S_{DD22} \end{bmatrix} & \begin{bmatrix} S_{DC11} & S_{DC12} \\ S_{DC21} & S_{DC22} \end{bmatrix} \\ \\ \begin{bmatrix} S_{CD11} & S_{CD12} \\ S_{CD21} & S_{CD22} \end{bmatrix} & \begin{bmatrix} S_{CC11} & S_{CC12} \\ S_{CC21} & S_{CC22} \end{bmatrix} \end{bmatrix} \cdot \begin{bmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{bmatrix} \tag{3.6}$$

where a_{di}, b_{di} are the differential-mode signal and a_{ci}, b_{ci} are the common-mode signals.

Each of the submatrixes composing the mixed-mode matrix presented in Equation 3.6 describes a different energy response of the characterized line:

- S_{DD} submatrix: differential- to differential-mode signal response.
- S_{DC} submatrix: mode conversion of common- to differential-mode signals.
- S_{CD} submatrix: mode conversion of differential- to common-mode signals.
- S_{CC} submatrix: common- to common-mode signal response.

The most useful mixed-mode S parameters to characterize the high-speed interconnect are the S_{DD11} or differential return loss parameter and the S_{DD21} or differential insertion loss parameter.

However, the mixed-mode S-parameters are also used for quantifying the amount of near- and far-end crosstalk induced in a victim line, i.e. with S_{DD31}, or the quantity of differential-mode signal that is converted to common-mode with S_{CD} parameters.

DC-coupling capacitors

One source of impedance mismatch are the DC-coupling capacitors used to interconnect high-speed components with different standard logic [50]. The area increase due to the capacitor pad reduces the impedance of the trace and generates reflections. The use of small capacitor form factors as 0201 reduces the impedance mismatch since the pads are much closer in size to the trace width. In the TilePPr module, DC-coupling capacitors are used to interconnect the Readout and the Trigger FPGAs, for the communication with the RTM module through the backplane and for the Avago MiniPOD connectors. No DC-coupling capacitors are needed for the QSFP lines, since the 0201 capacitors are included in the optical module.

Figure 3.15 shows the 0201 model employed to compare the mismatch impedance produced by 0201 and 0402 packages using a 3D field solver software called ANSYS HFSS [51]. The model of the interconnect is composed of a pair of DC-coupling capacitors and the corresponding differential traces.

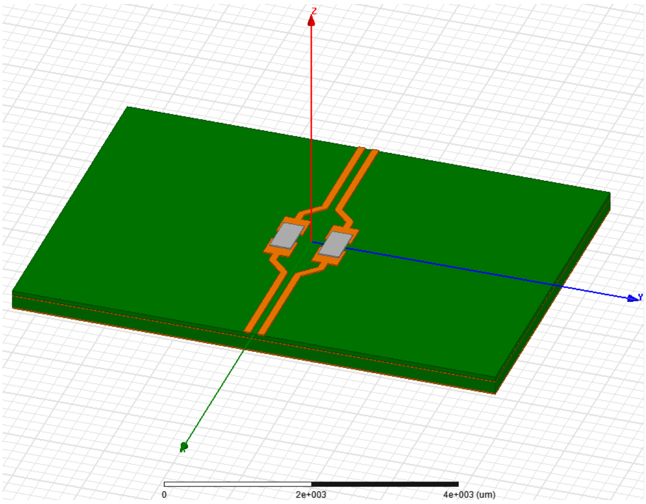
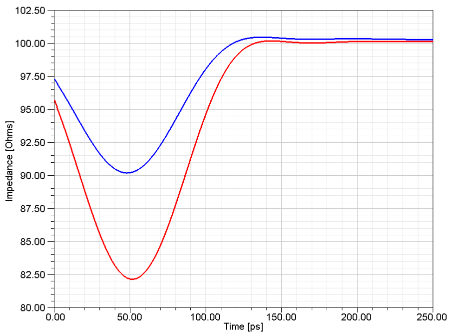
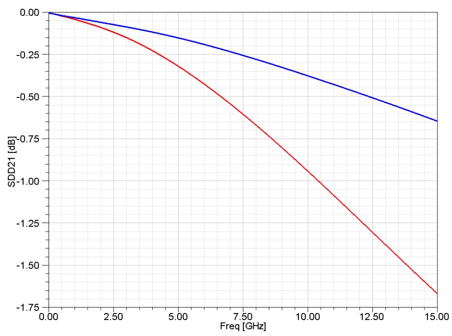


Figure 3.15: Model of a differential line with 0201 case DC-coupling capacitors (ANSYS HFSS software).

Figure 3.16 (a) shows the Time Domain Reflectometry (TDR) response of the 0201 and 0402 packages to a step signal with a rise time of 40 ps. The TDR technique is another common way to characterize the quality of the high-speed interconnects. A step signal with a fast rise time is transmitted through the interconnect and the reflected amplitude is measured in the time domain. The impedance discontinuity increases or decreases the returned step amplitude depending on its impedance.



(a) Comparison of the TDR response between differential interconnects with 0201 (blue) and 0402 (red) case DC-coupling capacitors using a step signal with a rise time of 40 ps.



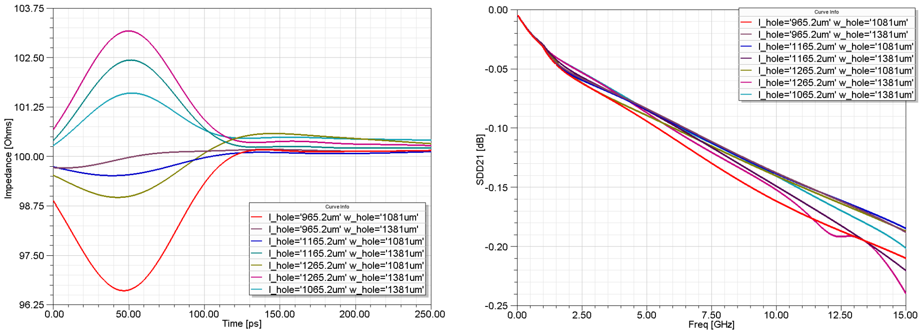
(b) Comparison of the insertion loss (S_{DD21} parameter) between differential interconnects with 0201 (blue) and 0402 (red) case DC-coupling capacitors.

Figure 3.16: Comparison of the TDR and insertion loss simulation results corresponding to two differential interconnects with 0201 and 0402 case DC-coupling capacitors.

As can be observed, the 0201 package generates a smaller impedance mismatch than the 0402 package and consequently the insertion loss (S_{DD21}) is also lower. Based on the results, 0201 package capacitors were used for the DC-coupling capacitors.

In addition, another technique to mitigate the effect of the 0201 DC-coupling capacitors is to cut a rectangular area of the reference plane under the pad to decrease the capacitance of the line. The TDR results and S_{DD21} parameters obtained from the simulation of different sizes of area cuts in the underneath power plane are shown in Figure 3.17.

As can be observed, the reduction of the capacitance formed by the capacitor pads results in a smaller impedance mismatch. However, the area cuts have not been implemented in the TilePPr prototype since the impedance discontinuity produced by the 0201 capacitors is already small and the implementation of this technique would split the reference plane due to the high number of capacitors and their proximity.



(a) TDR simulation results of a differential interconnect with 0201 case DC-coupling capacitors for different sizes of area cuts. The rise time of the step signal is 40 ps.

(b) Insertion loss (S_{DD21} parameter) of a differential interconnect with 0201 case DC-coupling capacitors for different sizes of area cuts.

Figure 3.17: Results of the TDR and insertion loss simulations corresponding to a differential interconnect with 0201 case DC-coupling capacitors with different sizes of area cuts.

Differential vias

When using a via to interconnect traces between different layers, there are some layout elements that compromise the signal integrity: Non-Functional Pads (NFP), via stub, and ground vias.

The NFPs are those pads of the via which are not connected to any layer along the PCB stack-up. Manufacturers include them in the stack-up to improve the mechanical stability of the via in the PCB laminate. One of the drawbacks of NFPs in high-speed designs is the impedance discontinuities introduced by the parasitic capacitances created between the NFPs and the neighboring reference layers. One way to avoid this problem is to remove the NFPs to decrease the via capacitance. Another approach is to enlarge the antipad size (area clearance between the via and the conductors in the same layer).

The second factor which creates a reflection is the via stubs. Via stubs are the remaining parts of the vias when interconnecting layers, i.e. if a via connects a trace from the TOP layer to layer 8, the rest of the via from layer 8 to the BOTTOM layer will create a reflection because an impedance discontinuity. This via stub creates a resonance that cancels the signal components at a frequency dominated by the length of the via stub ($\lambda/4$, where λ is the wavelength). The impedance mismatch due to via stubs can be eliminated by using the back-drilling technique or buried vias in the design at the expense of higher PCB manufacturing costs. However, a cost-effective technique is to route the high-speed lines in the more external layers of the PCB, thus reducing the stub length.

The third factor related to differential vias which compromises the signal integrity is the ground vias which provide the return path of the traveling signal. If no ground vias are placed at the proper near position, reflections will be produced.

The via structure used for the design of the TilePPr prototype was simulated to define the optimum size of the via antipad, the position of the ground vias and also to evaluate if back-drilling or buried vias were needed for the PCB layout. Figure 3.18 shows the 3D model employed to perform the simulations with a differential via connecting the top layer and layer 15.

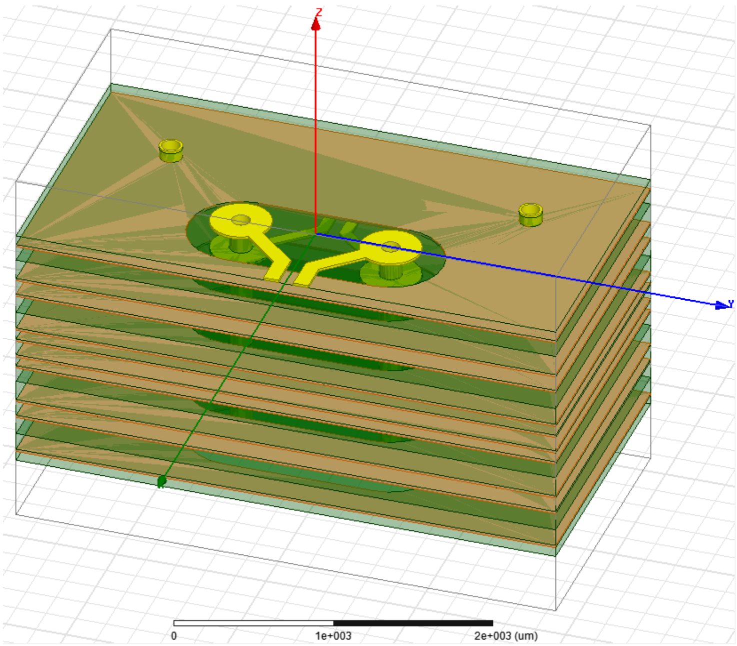
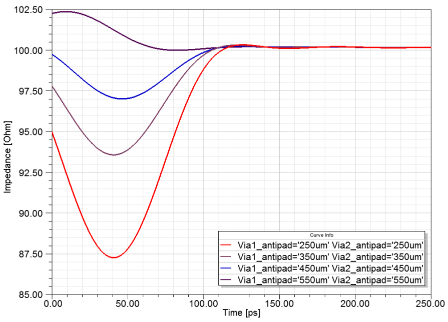
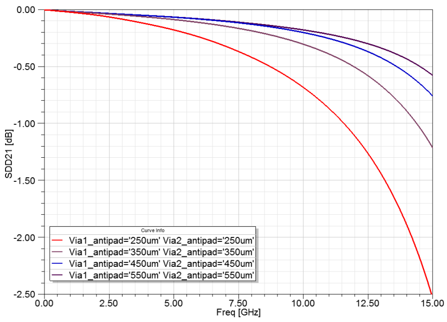


Figure 3.18: Model of the differential via used in the simulations with ANSYS HFSS.

Figure 3.19 shows the TDR and insertion loss comparison for a simulation where the radius of the via antipad is increased from 250 μm to 550 μm in steps of 100 μm. Radius of the via antipad between 450 μm and 550 μm produce an impedance mismatch below the 5% of the differential impedance and the minimum insertion loss factor.



(a) TDR simulation results of a differential via for different antipad radii. The rise time of the step signal is 40 ps.



(b) Insertion loss (S_{DD21} parameter) of a differential via for different antipad radii.

Figure 3.19: Results of the TDR and insertion loss simulations of a differential via layout for different antipad radii.

Finally, a different simulation is performed to determine the frequency of the via resonance in a worse case scenario where the via connects the TOP layer with layer 2 creating a long stub from layer 3 to 16. As can be observed in Figure 3.20 the via resonance appears above 20 GHz, out of the effective bandwidth and thus it does not degrade the quality of the signal.

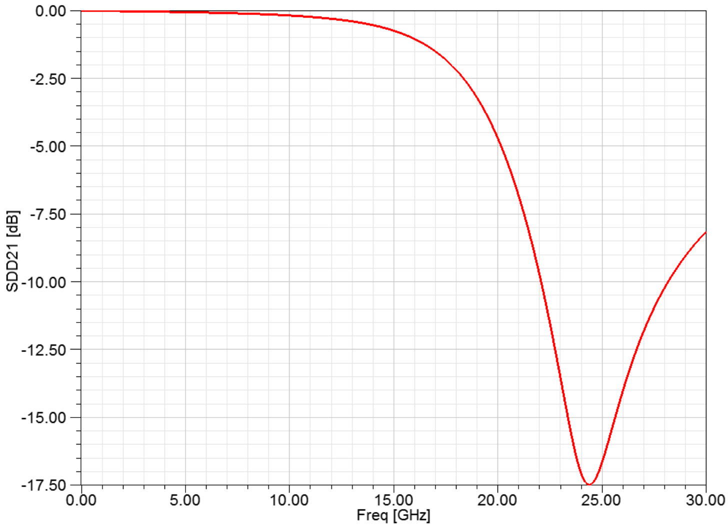


Figure 3.20: Insertion loss of a differential via with a stub from layer 3 to 16. The self-resonance frequency of the via is placed around 25 GHz.

3.3.3 IR drops

One critical point when designing boards with components that demands high currents are the voltage drops produced along the power planes due to the resistance of the conductors, called IR drops (I × R). The effective area of the power planes is reduced by the via holes, forming a swiss cheese effect that increases the DC resistance. If the power interconnects do not provide a low resistive path, voltages could drop enough to cause malfunctioning of some components.

In order to evaluate the impact of the swiss cheese effect in the power distribution, the IR drops were simulated using ANSYS SIwave software [52]. First, the maximum current consumption values of the FPGAs were calculated using the Xilinx Power Estimator (XPE) tool [53] considering a worst case defined by the next scenario of resource usage [54].

- 80% of Look-Up Tables and registers clocked at 245 MHz.
- 80% of block RAM and DSP at 491 MHz.
- 50% of the MMCM circuits and 25% of the PLLs at 500 MHz.
- 100% of the GPIO using SSTL 1.2 clocked at 1,200 MHz.
- All the routed GTX transceivers running at the specified data rate.

Table 3.6 shows a summary of the estimated maximum current carried by the different power rails of the TilePPr.

Power Rail	Voltage (V)	Virtex 7	Kintex 7	Total
		Current (A)	Current (A)	Current (A)
$V_{CCINT}+V_{CCBRAM}$	1.0	15.02	12.415	27.435
V_{CCAUX}	1.8	0.558	0.611	1.169
$MGTV_{CCAUX}$	1.8	0.062	0.062	0.124
$MGTAV_{CC}$	1.0	4.204	2.656	6.86
$MGTAV_{TT}$	1.2	2.531	1.24	3.771

Table 3.6: Summary of the maximum current consumption of the TilePPr power rails. Current consumptions were estimated using the Xilinx XPE tool.

According to the simulations, all power rails have a maximum voltage drop close or lower to the 3% of the operating voltage as recommended by the manufacturer. From all the IR drop simulations, the more restring value corresponds to the V_{CCINT} power rail. This power rail feeds the core of both Kintex and Virtex 7 FPGAs with a maximum estimated current that almost reaches 27.5 A.

Figure 3.21 shows the result of the IR drop simulation in layer 12 for the V_{CCINT} power rail. As can be observed, the IR drops for V_{CCINT} power rail reaches a minimum of 0.969 mV at the Virtex 7 location. This value is slightly lower than the operating voltage recommended by the manufacturer. The IR drop for this power rail could be reduced by using wider power vias or smaller via antipad in the area underneath the FPGA. Nevertheless, the TilePPr power monitoring circuitry includes capabilities for trimming the output voltage of the power modules in case the voltage in the power rails is under the recommended values.

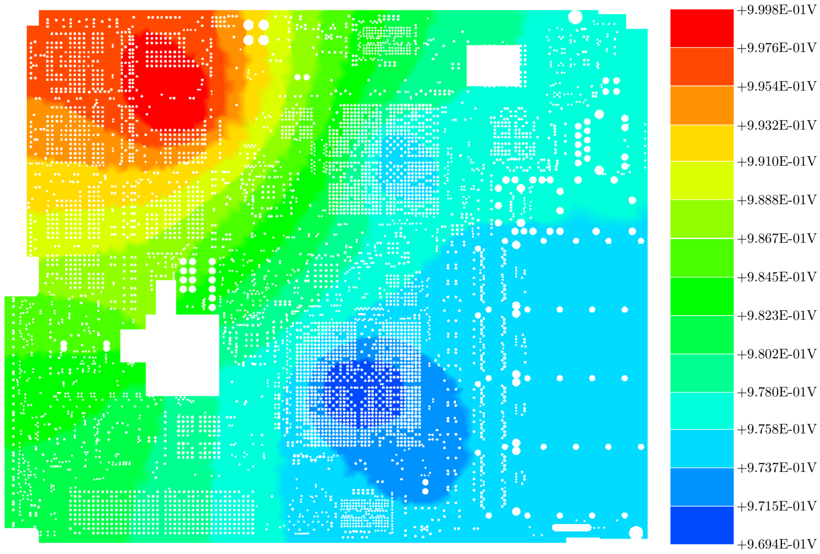


Figure 3.21: IR drops on layer 12 for the V_{CCINT} power rail. The Kintex 7 FPGA (top) is draining 12.415 A and the Virtex 7 FPGA (bottom) is consuming 15.02 A.

3.4 Post-layout simulations

Post-layout simulations were performed to validate the routing before manufacturing the PCB. The mixed-mode S-parameters were extracted using ANSYS tools and studied to verify that no signal integrity problems will cause errors in the communications.

The signal integrity studies presented here correspond to the QSFP1 RX0 and RX1 differential lines. The QSFP RX lines were selected for the simulations since will be used to receive the data from the front-end electronics at rates close to 10 Gbps. Figure 3.22 shows the physical model of lines RX0 and RX1 (highlighted in yellow) employed for the signal integrity simulations.

3.4.1 Insertion and return losses

Insertion and return losses of the high-speed lines were studied to quantify the energy not transmitted to the load and to determine if it affects the signal quality. Insertion and return losses are related according to Equation 3.7.

$$S_{DD21} = \sqrt{1 - {S_{DD11}}^2} \tag{3.7}$$

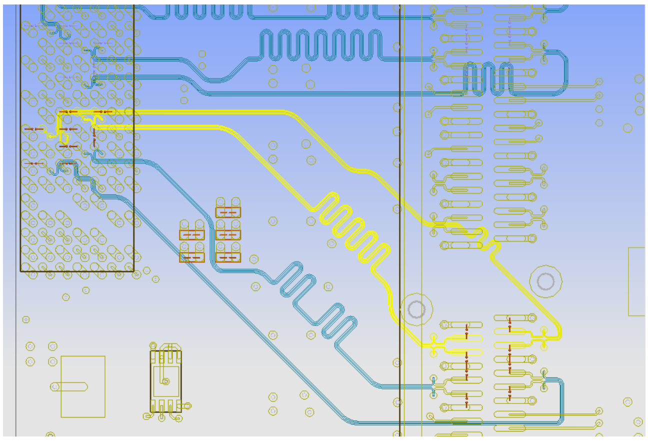
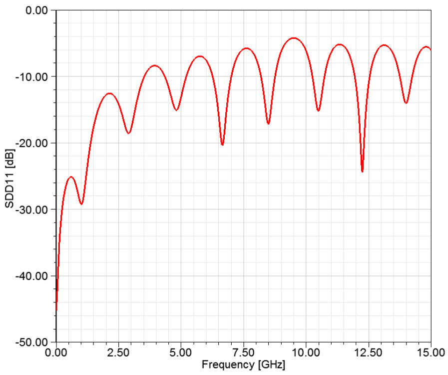
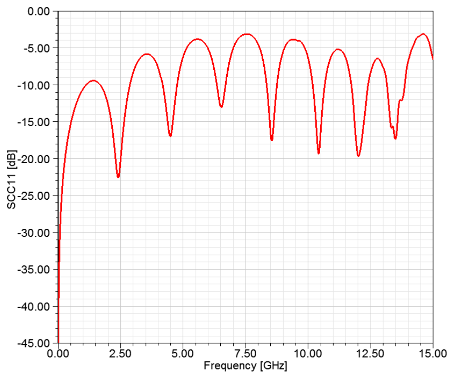


Figure 3.22: Snapshot of the physical model used for the signal integrity simulations with ANSYS Siwave software. RX0 and RX1 lines are highlighted in yellow.

Figure 3.23 shows the simulated S_{DD11} value for differential signals and S_{CC11} for common signal value from the QSFP1 RX0 channel. The reflected energy corresponds to the impedance mismatch produced by the pads of the FPGA and QSFP connector plus the impedance mismatch due to the separation of the differential pair and vias when the trace arrives to the QSFP connector and FPGA pads. The energy reflected back to the source will be translated as an addition to the insertion losses.



(a) Simulation of the S_{DD11} parameter.



(b) Simulation of the S_{CC11} parameter.

Figure 3.23: Simulation of the S_{DD11} and S_{CC11} parameters for RX0 line.

Figure 3.24 shows the result of the simulations of the S_{DD21} values for the RX0 line. Results show a low insertion loss of -2 dB at the Nyquist frequency 5 GHz, which will not degrade the signal quality [49]. The maximum Nyquist frequency referred to a serial link is half the data rate [46].

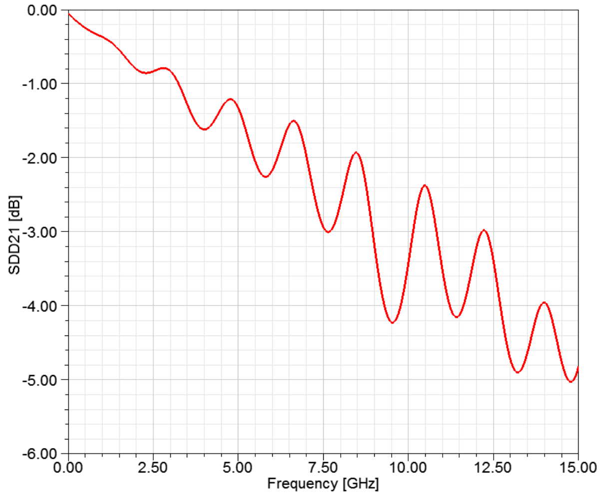


Figure 3.24: Simulation of the S_{DD21} parameter for RX0 line.

Line asymmetry

The asymmetry in length between the two traces of a differential pair produces impedance mismatches converting part of the signal from differential- to common-mode. Although the maximum length difference between the two traces was limited during the routing stage to 100 μm, simulations were performed to ensure that no significant quantities of energy are converted from the differential- to the common-mode.

Figure 3.25 shows the simulated S_{CD21} parameter corresponding to the RX0 line. As can be observed, there is a negligible part of the differential-mode signal being converted to common-mode.

Crosstalk studies

Crosstalk to neighboring traces can also be evaluated with mixed-mode S-parameters. Crosstalk in high-speed designs refers to part of the energy of the signal induced on the neighboring lines due to capacitance and inductance

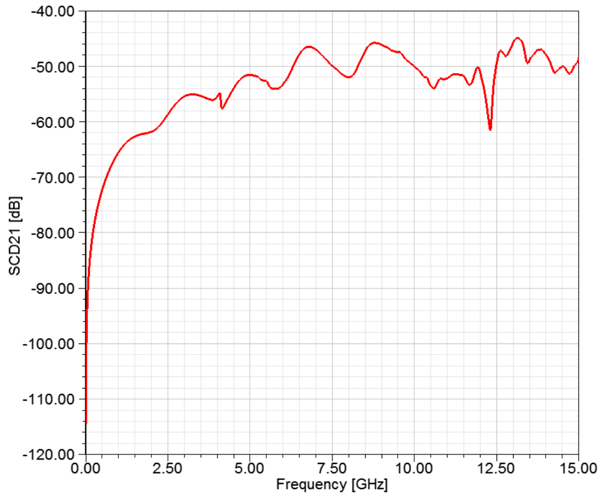
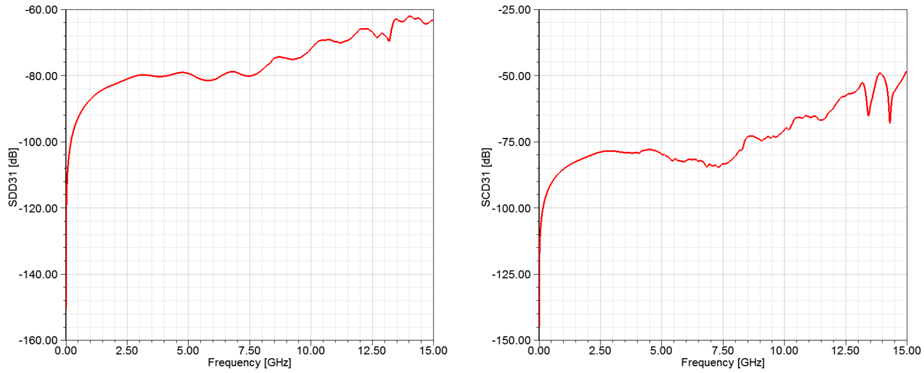


Figure 3.25: Simulation of the S_{CD21} parameter for RX0 line.

couplings between them. Crosstalk can be basically categorized in two types: Near-End crossTalk (NEXT) and Far-End crossTalk (FEXT). NEXT is the induced noise at the end of a victim line close to the transmitter of the aggressor, while FEXT refers to the induced noise at the opposite side of the victim line. Although the high-speed lines in the TilePPr prototype are separated as far as possible from possible victim or aggressor lines, a quantification of the NEXT and FEXT was performed.

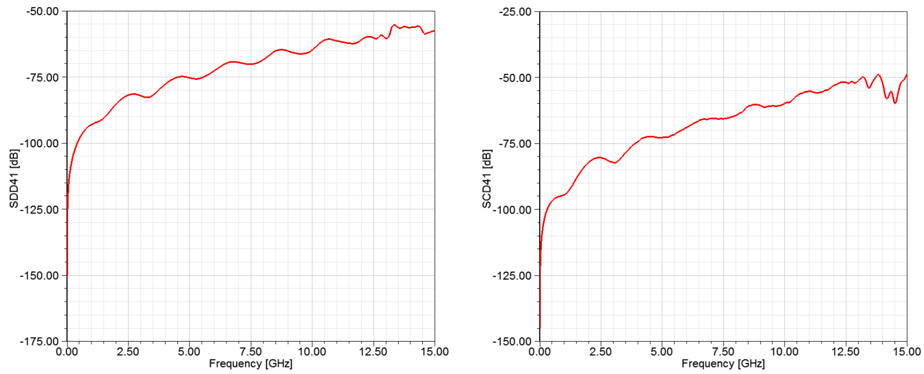
Figure 3.26 shows the NEXT from differential to differential signal (S_{DD31}) considering a 4-port network composed of two differential channels RX0 and RX1, and also the NEXT from differential to common signal (S_{CD31}) is shown. The simulated NEXT between RX0 and RX1 differential lines is negligible for both cases in the frequency range of interest.

Figure 3.27 shows the results of the FEXT simulation for differential to differential signals (S_{DD41}) and differential to common signals (S_{CD41}). As the NEXT, FEXT is negligible showing a induced noise of -75 dB at the Nyquist frequency for the differential to differential signals and below -70 dB for the differential to common signals. Following the results of the crosstalk studies, the induced noise in the high-speed lines for the communication between the Readout FPGA and the QSFP modules is negligible and does not contribute to degradation of signal quality.



(a) Simulation of the S_{DD31} parameter. (b) Simulation of the S_{CD31} parameter.

Figure 3.26: Simulation of the S_{DD31} and S_{CD31} parameters for the study of the NEXT between the RX0 and RX1 lines.



(a) Simulation of the S_{DD41} parameter. (b) Simulation of the S_{CD41} parameter.

Figure 3.27: Simulation of the S_{DD41} and S_{CD41} parameters for the study of the FEXT between the RX0 and RX1 lines.

3.5 Characterization tests

The goal of the characterization test of the TilePPr prototype was to study the jitter in the high-speed lines used to communicate the front-end and back-end electronics systems. As mentioned in Chapter 2, the TilePPr will send the LHC clock to the front-end electronics embedded with the data. For this reason, the lines associated with the communication with the front-end electronics have to provide sufficiently low jitter. The quality of these data signals was evaluated in terms of jitter.

3.5.1 Introduction to jitter

Jitter is defined as the time deviation of a signal with respect to its expected occurrence in time. This timing shift in the signal has a large number of causes including crosstalk, Inter Symbol Interference (ISI), impedance discontinuities, and thermal noise [55]. The total jitter (T_J) of a high-speed line can be decomposed in two main types: random jitter (R_J) and deterministic jitter (D_J), where the last one is categorized in different subtypes of jitter as depicted in Figure 3.28.

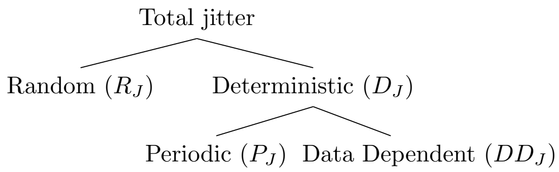


Figure 3.28: Classification of jitter.

Random jitter

R_J represents a jitter which is uncorrelated to any other signal in the design, thus producing unpredictable time variations. R_J is considered to follow a Gaussian distribution, therefore its peak-to-peak values are not mathematically bounded. Instead, R_J is usually expressed in Root-Mean-Square (RMS) seconds. The primary contributors to R_J are the thermal noise, shot noise and pink noise($1/f$) generated in electronic devices.

Deterministic jitter

The second contributor to the T_J is the (D_J). D_J is defined as a time deviation of a signal that is repeatable and therefore can be predicted. Since the jitter is repeated in time, the peak-to-peak value of this jitter is bounded. For this reason, D_J measurements are defined in units of peak-to-peak seconds. This class of jitter is again divided in two types of jitter based on its source.

- Periodic jitter (P_J) is referred to timing shifts following a periodic pattern. This jitter is typically caused by external deterministic noise sources, such as power supply noise or unstable PLLs oscillating, but it is not correlated to data.

- Data-Dependent Jitter (DD_J) is defined as the jitter correlated to the bit sequence in a data stream. DD_J is produced by a combination of impedance mismatches, frequency response of the transmission lines and asymmetries in the duty cycle of the transmitted signal.The main sources of DD_J are the Inter Symbol Interference (ISI) and the Duty-Cycle Distortion (DCD).

Total jitter

The total jitter probability density function (PDF) is the result of the convolution between R_J and D_J.

$$T_J = R_J * D_J \tag{3.8}$$

T_J is usually defined as the total jitter at a specific Bit Error Ratio (BER), since T_J is unbounded due to the contribution of R_J. It provides a jitter estimation related to the total jitter contribution to a specific BER as defined in Equation 3.9 [56].

$$T_J(BER) = 2 \cdot Q_{BER} \cdot R_J(RMS) + D_J(\delta\text{-}\delta) \tag{3.9}$$

where $D_J(\delta\text{-}\delta)$ is the D_J obtained through the dual-Dirac method and Q_{BER} is a factor derived from the complementary error function. Q_{BER} estimates the amount of eye closure produced by the R_J for a specific BER. Some values of Q_{BER} are shown in Table 3.7.

BER	Q_{BER}	**BER**	Q_{BER}
10^{-12}	14.069	10^{-16}	16.444
10^{-13}	14.698	10^{-17}	16.987
10^{-14}	15.301	10^{-18}	17.514
10^{-15}	15.882		

Table 3.7: Q_{BER} factor as a function of BER.

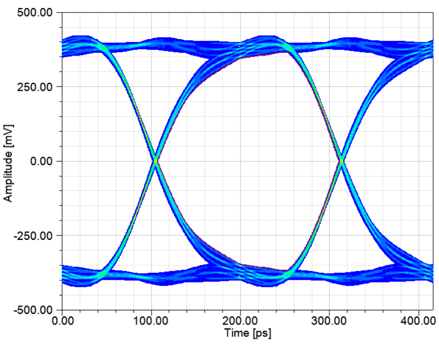
3.5.2 Eye diagrams

Eye diagram is a common technique to detect signal integrity problems in the time domain. Eye diagrams are generated by overlaying a high number of logic transitions in the time domain scale. The opening in time and amplitude of the eye diagram gives an estimation of the quality of the signal in terms of jitter and also adding a valuable information about the path attenuation.

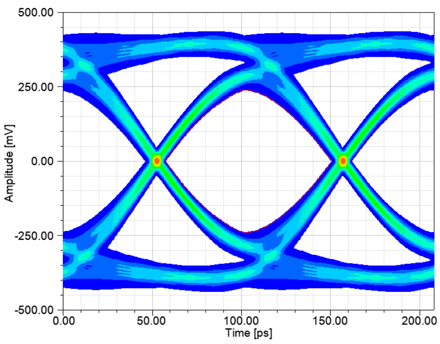
Simulations of high-speed lines

In this thesis, eye diagrams were simulated for the receiving and transmitting lines used for the communication with the front-end electronics. The simulation was carried out using the ANSYS software tools, where the S-parameters of lines were extracted and co-simulated using IBIS-AMI models for the drivers and receivers. Two different sets of simulations were performed corresponding to the two data rates of 4.8 Gbps and 9.6 Gbps used in the TilePPr prototype.

Figure 3.29 shows the simulated eye diagrams. Both diagrams show wide-open eyes in amplitude and time, indicating a good layout design of the high-speed lines and low attenuation. The estimated jitter from the simulations is 1.083 ps_{RMS} for the transmitter lines at 4.8 Gbps (Figure 3.29 (a)), and 2.043 ps_{RMS} for the receiver lines at 9.6 Gbps (Figure 3.29 (b)). Both values can be considered very low for the data rates of operation.



(a) Eye diagram for the transmitter lines at the QSFP connector pins. The simulation is performed with a data rate of 4.8 Gbps and a PRBS31 pattern.



(b) Eye diagram for the receiver lines at the Readout FPGA pins. The simulation is performed with a data rate of 9.6 Gbps and a PRBS31 pattern.

Figure 3.29: Simulated eye diagrams using the IBIS-AMI models provided by Xilinx.

The high-frequency losses degrade the rising and falling times thus reducing the eye opening in amplitude. This effect is more evident for the receiver lines operating at 9.6 Gbps than for the transmitter lines running at 4.8 Gbps.

Jitter and BER measurements

A set of measurements was done to evaluate the quality of the signals transmitted to the front-end electronics. The different types of jitter were measured in the optical signals transmitted through an Avago AFBR-79Q4Z QSFP module [57] using a Keysight DCA-X 86100D sampling oscilloscope [58] equipped with the optical module 86105C.

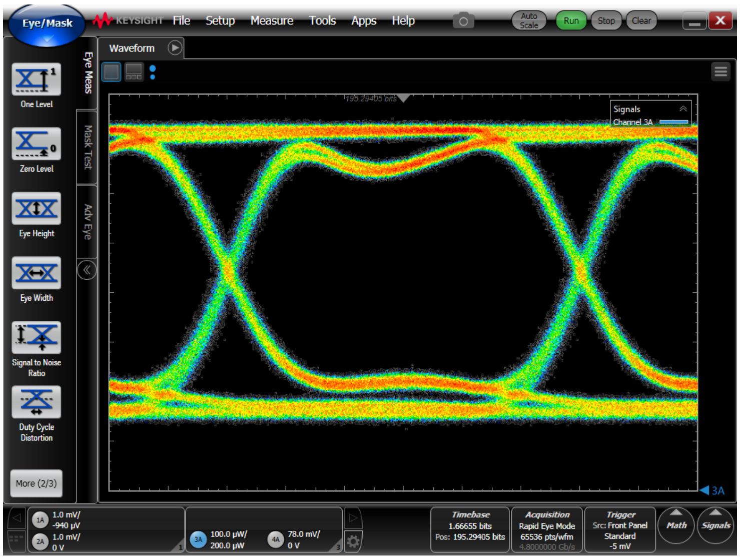
These measurements were employed to validate the correct design and production of the TilePPr prototype since these tests include not only the high-speed lines but also the rest of the components involved in the data communication such as clocks, jitter cleaners, and power supplies. An IBERT IP core from Xilinx [59] was implemented in the Readout FPGA to transmit a PRBS31 pattern. Table 3.8 shows the jitter measurement results done at 4.8 Gbps and 9.6 Gbps data rates with the corresponding standard deviations, and Figure 3.30 shows the eye diagrams generated measuring the optical signal of one QSFP transmitter.

	4.8 Gbps		**9.6 Gbps**	
	μ **(ps)**	σ **(ps)**	μ **(ps)**	σ **(ps)**
R_J**(RMS)**	2.74	0.28	2.97	0.25
$D_J(\delta\text{-}\delta)$	2.44	1.31	5.94	1.29
$T_J(10^{-12})$	39.85	3.46	46.5	3.15
$T_J(10^{-13})$	41.61	3.31	48.42	3.02
$T_J(10^{-14})$	43.31	3.16	50.25	2.88
$T_J(10^{-15})$	44.94	2.99	52.02	2.74
$T_J(10^{-16})$	46.51	2.83	53.71	2.59
$T_J(10^{-17})$	48.03	2.65	55.36	2.43
$T_J(10^{-18})$	49.5	2.48	56.95	2.27

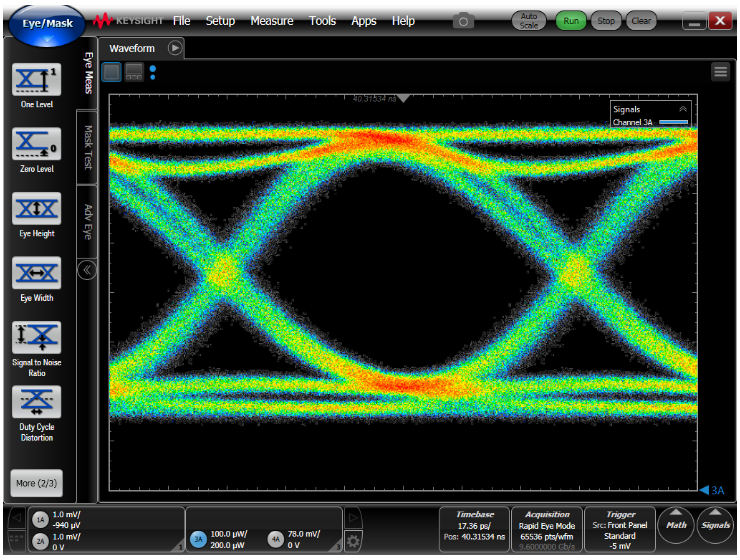
Table 3.8: Jitter measurement results for one transmitter of the TilePPr prototype at 4.8 Gbps and 9.6 Gbps rates.

The jitter measurements show a good quality of the signal transmitted towards the front-end electronics with low jitter values. The estimated T_J ensures that the design is robust enough to operate at the required data rates showing a $T_J(10^{-18})$ of 0.23 Unit Interval (UI) at 4.8 Gbps and 0.55 UI at 9.6 Gbps. While the R_J takes similar values for 4.8 Gbps and 9.6 Gbps cases, the deterministic component presents a higher value at 9.6 Gbps. The Keysight DCA-X 86100D provided a resolution of 5 fs and 2 fs in the R_J(RMS) measurement for 4.8 Gbps and 9.6 Gbps respectively. The resolution in the rest of measurements was 50 fs for 4.8 Gbps and 20 fs for 9.6 Gbps.

Finally, as part of the validation test for the TilePPr prototype, a BER test was performed during a period of 115 hours [60]. A Xilinx IBERT IP core was implemented to control the 16 transceivers connected to the QSFP modules. The QSFP modules were connected in loopback mode using fibers and the transceivers were configured to transmit a PRBS31 data pattern at 9.6 Gbps. Since no error were detected during all the test period the obtained BER was better than $5 \cdot 10^{-17}$ with a confidence level (CL) of 95% [61].



(a) Optical eye diagram corresponding to one transmitter of the QSFP module running at 4.8 Gbps.



(b) Optical eye diagram corresponding to one transmitter of the QSFP module running at 9.6 Gbps.

Figure 3.30: Optical eye diagrams generated with the Keysight DCA-X 86100D oscilloscope.

Chapter 4

Integration of the TilePPr in the Demonstrator

As already covered in Chapter 2, the Demonstrator project aims to evaluate the proposed DAQ architecture and detector readout electronics for the HL-LHC prior to its installation into the ATLAS detector.

A Demonstrator module was populated with prototypes of all the new components and tested during the testbeam campaigns. This module is composed of four minidrawers containing the required electronics to operate and read out up to 48 PMTs. Each minidrawer includes twelve 3-in-1 cards, one MainBoard, one DaughterBoard and, depending on the minidrawer, an HVOpto board or an HV distribution board. In the back-end electronics, the Tile PreProcessor prototype distributes the configuration commands and sampling clock to the front-end electronics and receives the digitized data for every period of the LHC clock.

The DAQ architecture employed for the readout and operation of the Demonstrator electronics is similar to the one proposed for the HL-LHC, with the difference that the Demonstrator module is also be able to provide analog trigger signals to the L1Calo system permitting its installation into the current ATLAS detector.

This chapter gives a detailed description of the different firmware modules included in the DaughterBoard and TilePPr prototype for the Demonstrator.

4.1 GBT protocol

The GigaBit Transceiver (GBT) protocol [62] was developed at CERN for the data transmission between the front-end and the back-end electronics in the HL-LHC era as part of the GBT project [63]. This protocol establishes a common transmission path for the TTC, DAQ and Slow Control (SC) information.

The GBT project includes the development of different radiation tolerant ASICs implementing the GBT protocol, such as the GBTx or the GBT-SCA [64], as part of the front-end electronics where COTS components cannot operate due to the radiation levels. However, in the counting rooms where the radiation levels are not a concern, the GBT protocol can be implemented in FPGAs.

The VHDL-based firmware version of the GBT protocol, called GBT-FPGA IP core [65], is supported by CERN and can be implemented in various FPGA models with embedded transceivers.

Figure 4.1 shows a block diagram of the GBT-FPGA IP core indicating the frequencies at which each block operates and the data flow. The GBT protocol transmits a 120-bit frame at the LHC clock frequency of 40 MHz, resulting in a line rate of 4.8 Gbps.

The implementation of the GBT-FPGA IP core in FPGA employs four clocks to handle the data across the different blocks.

- *tx_frame_clk*: this clock corresponds to the LHC clock frequency.
- *tx_word_clk*: the FPGA transceiver generates this clock internally to transmit 40-bit words and its frequency is 3 times the *tx_frame_clk* frequency, this is 120 MHz.
- *rx_frame_clk*: a Mixed-Mode Clock Manager (MMCM) is used to generate it from the *rx_word_clk* and its frequency corresponds to the LHC clock frequency.
- *rx_word_clk*: the FPGA transceiver recovers this clock from the incoming data and has a frequency of 120 MHz. A 40-bit word is received for every rx_clock_cycle.

The first block in the transmitter side is the Scrambler. It is implemented as a Linear Feedback Shift-Register (LFSR) which produces pseudorandom bit sequences reducing the occurrence of long streams of ones or zeros, maintaining the DC-balance in the serial transmitter output signals.

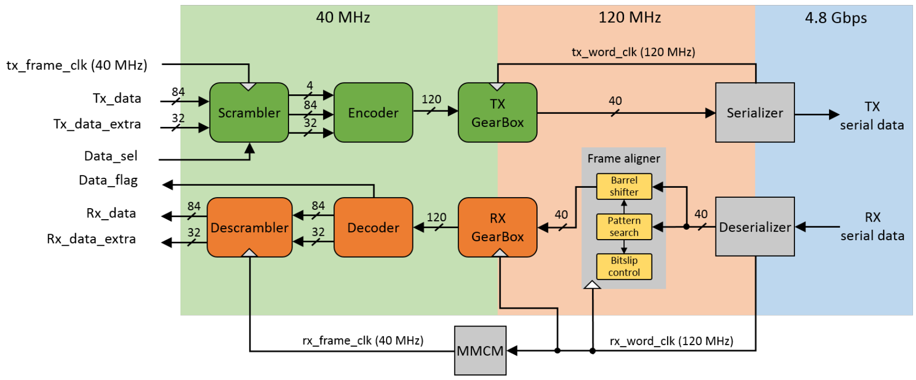


Figure 4.1: Block diagram of the transmitter and receiver blocks of the GBT-FPGA IP core.

Then, the scrambled data is driven into a double interleaved Reed Solomon (RS) encoder capable of correcting up to 16 consecutive errors per 120-bit GBT word. The use of the RS error correction reduces the data bandwidth by about 30%, so the available data bandwidth is 3.2 Gbps. However, the RS block can be bypassed to use the Forward Error Correction (FEC) field (32-bits) for data. This operation mode is called GBT Wide-Bus, and it provides an increased user data bandwidth of up to 4.48 Gbps.

The output of the RS block is sent to the TX Gearbox block which manages the data transmission between the GBT-FPGA IP core and the FPGA transceivers, performs the Clock Domain Crossing (CDC) between the two domains, and adjusts the data path widths.

The inverse process is performed in the GBT receiver side, where the received data passed through Descrambler, Gearbox, and Decoder blocks. Additionally, the GBT receiver includes the Frame Aligner block which aligns the 40-bit words from the transceiver using the received patterns and builds the complete 120-bit GBT word.

Since the front-end electronics is supposed to use the recovered clock to transmit data to TilePPr, both *rx_frame_clk* and *tx_frame_clk* in the TilePPr are in the same clock domain. However, the phase relationship between them is unknown, and thus safe data transferences between these clock domains cannot be guaranteed due to metastability issues. This unknown phase difference results in a challenge for those readout systems which have to combine data from both clock domains. For example, in the TilePPr the received data are stamped with its corresponding BCID, where the BCID is in the *tx_frame_clk* clock domain and the received data is in the recovered *rx_frame_clk* clock domain. A solution to this problem is proposed in the BE Tile GBT-FPGA IP core section.

GBT data format

The data format of the GBT protocol is described for the GBT Frame mode in Table 4.1 and for the GBT Wide-Bus mode in Table 4.2, where 4 bits are reserved for the Header (H), 4 bits for Slow Control (SC) and 80 bit for user data.

119 116	**115 112**	**111 32**	**31 0**
H	SC	Data	FEC

Table 4.1: Standard GBT data format with FEC.

119 116	**115 112**	**111 0**
H	SC	Data

Table 4.2: Wide-Bus GBT data format without FEC.

Another important feature of the GBT protocol is the header encoding. The GBT header is encoded by the transmitter into two symbols via the *Data_sel* signal (Figure 4.1) adding some extra information to the contents of the frame.

- "0110": when the GBT word is an IDLE word.
- "0101": when the GBT word includes a data word.

In the GBT receiver side, the *Data_flag* signal permits the identification of the received word.

Standard and Latency Optimized GBT version

The GBT-FPGA IP core can be configured in two different modes depending on the latency requirements: the Standard and the Latency Optimized (LO) version.

The Standard version is intended for non-timing critical applications since it does not provide a deterministic latency, while the LO version guarantees a low, fixed and deterministic latency of the clock and data in both directions at the cost of a more complex implementation in the FPGA.

The implementation of the LO GBT-FPGA version requires to bypass those blocks of the FPGA transceiver that cannot guarantee a fixed and deterministic latency, such as the elastic buffers used to resolve the phase differences between the transceiver and logic clock domains. In addition, the LO GBT-FPGA version includes a phase alignment circuit to guarantee the deterministic phase of the recovered *rx_frame_clk* with respect to the *tx_frame_clk* used in the source.

4.2 Tile GBT-FPGA IP core

The Tile GBT-FPGA IP core was designed based on the original LO GBT-FPGA code to fulfill the requirements for the Tile Calorimeter readout system at the HL-LHC.

One of the main differences between the LO GBT-FPGA version and the Tile GBT-FPGA version is the data bandwidth. While the original code implements a communication path operating at 4.8 Gbps in both directions, the Tile GBT-FPGA block implements an asymmetric communication path where the downlink (back-end to front-end) operates at 4.8 Gbps and the uplink (front-end to back-end) at 9.6 Gbps.

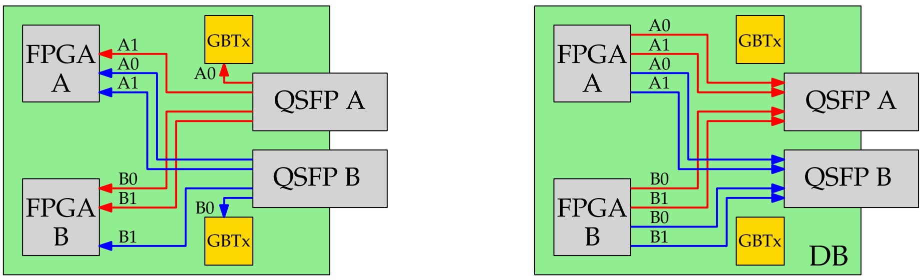
As discussed in Chapter 2, each redundant link of the DaughterBoard transmits two 12-bit samples corresponding to 2 gains for 6 channels per LHC clock cycle. Then, the total data bandwidth required in the uplink to transmit the digitized data reaches 5.7 Gbps. Doubling the rate of the GBT protocol would provide a total data bandwidth of 6.72 Gbps (using the SC bits as data), and the remaining data bandwidth would be insufficient to transmit both the integrator and slow control data to the TilePPr modules.

For this reason, the uplink Tile GBT-FPGA blocks were configured to operate in Wide-Bus mode, where the upper 16 bits of the 32-bit FEC field were utilized to transmit data and the lower 16 bits were reserved for a Cyclic Redundancy Check (CRC) word to provide error detection, achieving a total data bandwidth in the uplink of 8 Gbps. It is important to remark here that the transceivers are operated outside of the manufacturer specifications, since the Quad PLL (QPLL) used to generate the internal clocks for the transceiver has a frequency gap between 8 GHz and 9.8 GHz[1]. This issue made critical the study and correct selection of the clocking structure and transceiver configuration.

Related to the downlink, the Tile GBT-FPGA block was configured to operate in Frame mode (using the error correction capabilities) at the nominal rate of the GBT protocol. Minor changes on the original code were made to adapt it to the TileCal needs. The Tile GBT-FPGA IP core and its implementation in the DaughterBoards and TilePPr boards is described in detail below.

4.2.1 Front-end Tile GBT links

A total of four FE Tile GBT links were implemented in the DaughterBoard, corresponding to two links per FPGA to communicate with the back-end electronics through a QSFP module. Figure 4.2 depicts a sketch of the DaughterBoard showing the link connections between the QSFPs and the FPGAs for the downlink (a) and uplink (b).



(a) Connections between the QSFPs and the FPGAs for the downlink communication.

(b) Connections between the QSFPs and the FPGAs for the uplink communication.

Figure 4.2: DaughterBoard link connections.

Depending on which QSFP module is used to operate the minidrawer up to two downlinks are routed to the FPGA transceivers, although in the current firmware version only A1 and B1 downlinks from QSFP A are implemented for simplicity. When QSFP A is used, the GBTx A recovers a multiple of the LHC clock (160 MHz) from the A0 channel which is routed to both FPGAs to drive

[1]This gap only occurs in the GTX transceivers and not to the GTH transceivers.

the clocking circuitry of transceivers. In the same way, if QSFP B is used, the GBTx B extracts the recovered clock from the B0 channel.

The recovered 160 MHz clock is connected to a Channel PLL (CPLL) which generates all the necessary clocks to operate the FE GBT-FPGA block receiver. In the case of the uplink, the CPLL cannot drive the transmitter at 9.6 Gbps, and the high-performance QPLL has to be used instead. However, although the uplink rate is in the QPLL range of operation (despite the gap already commented), the values of its multipliers and dividers do not permit the generation of the required clocks to drive the high-speed serializer in the transceiver.

A solution to overcome this limitation is to connect the 120 MHz clock extracted from the Clock and Data Recovery (CDR) of the receiver directly to the QPLL reference clock input using a Horizontal clock buffer (BUFH). This technique, which is not recommended by the manufacturer [66], carries the risk of adding jitter into the transceiver circuitry causing errors and instabilities in the communication links due to the fact that the reference clock is routed through the fabric clocking network.

In the first version of the GBT-FPGA IP core, the recovered clock from the transceiver (*rx_word_clk*) was used as clock source for the QPLL with satisfactory results. However, the stability of the transmitter was compromised by the quality of the recovered clock. The proposed solution to enhance the robustness of the links was to configure the CPLL of the unused receiver (A0, B0) to generate 120 MHz from the 160 MHz provided by the GBTx. To implement this, the auto-adapting algorithm of the CDR unit of the receiver was disabled to interrupt the transceiver to lock to incoming data.

The clocking structure implemented for the Tile GBT-FPGA blocks is presented in Figure 4.3. All the internal clocks needed for the operation of the DaughterBoard are generated from the *rx_word_clk* keeping the uplink and downlink synchronized in the same clock domain. In addition, the *rx_frame_clk* (40MHz) is derived from the *rx_word_clk* keeping a fixed and deterministic phase difference with the *tx_frame_clk* clock from the TilePPr. It is crucial that both clocks keep a fixed and deterministic phase difference to provide the correct time stamp to the data in the TilePPr, since the *rx_frame_clk* is used as sampling clock for the digitization of the PMT pulses in the MainBoard.

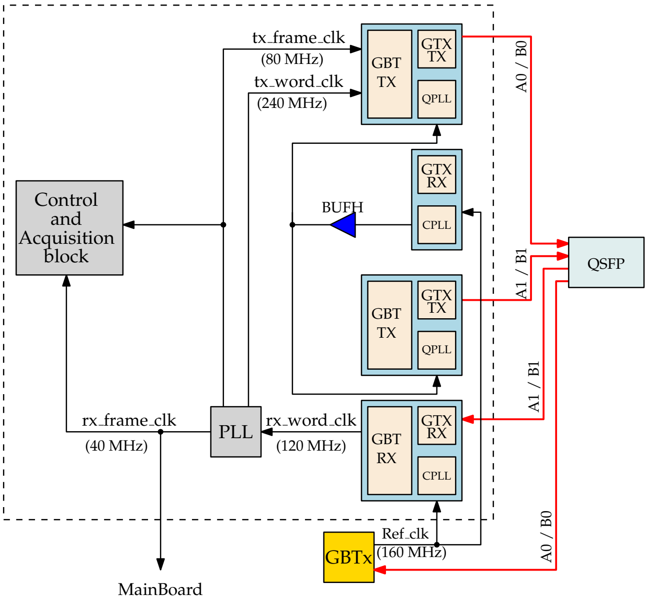


Figure 4.3: Block diagram of the clocking distribution for the Tile GBT links in the DaughterBoard.

4.2.2 Back-end Tile GBT links

Sixteen BE Tile GBT-FPGA links were implemented in the Readout FPGA for the communication with the Demonstrator module. The transmitter part of the Tile GBT-FPGA was configured in Frame mode and operated at the nominal GBT data rate of 4.8 Gbps. Only minor modifications were done to accommodate the original code to the downlink requirements. A proper clock distribution was planned in order to share the maximum number of clock resources, reducing the number of clock domains.

However, the receiver part required major modifications in order to fulfill the requirements of the data rate and to fit the high number of links in the Readout FPGA. The BE Tile GBT-FPGA receiver was designed to operate at the double nominal GBT data rate (9.6 Gbps) and in Wide-Bus mode, making the Tile GBT receiver compatible with the Tile GBT transmitter implemented in the DaughterBoard. A major problem was found when implementing the 16 links due to the limited number of clocking resources available in the Readout FPGA and to the complexity of managing such a high number of clock domains. As already shown in Figure 4.1, each GBT-FPGA receiver requires a MMCM block to generate the *rx_frame_clk* from the *rx_word_clk*, while the Readout FPGA only contains 14 MMCMs.

A proposed solution to overcome this limitation and to implement the 16 Tile GBT links in the Readout FPGA was to replace the functionality of the MMCM by Blind Oversampling CDR (BO-CDR) circuits [67] [68] [69].

The first modification was performed in the Descrambler block of the GBT-FPGA IP core. The Descrambler block was modified to be clocked with the *rx_word_clk* (Figure 4.4), where a multiplexer located between the RX Gearbox and the Descrambler handles the data between both blocks. Since the *Header* signal is received every 3 *rx_word_clk* clock cycles, a new GBT word is built for every LHC half clock cycle (the uplink operates at 9.6 Gbps).

After modifying the Descrambler block, the *rx_frame_clk* is not required anymore for the reception of the GBT words, and thus the MMCM can be removed from the GBT receiver. Nevertheless, the data is still in the *rx_word_clk* clock domain and has to be retimed to the TilePPr clock domain (*tx_frame_clk*), where the phase relationship between both clocks unknown.

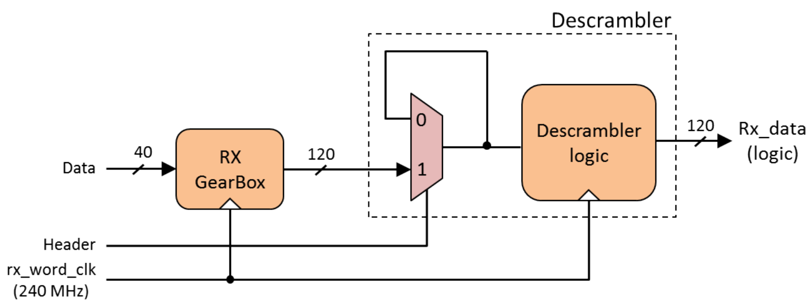


Figure 4.4: Block diagram of the modified Descrambler of the BE Tile GBT-FPGA module.

The latter issue is solved with the implementation of the BO-CDR circuit shown in Figure 4.5. This circuit is composed of a set of samplers and synchronizers with 3 shift registers and one multiplexer (MUX) which are implemented for each GBT word bit, and a unique MUX decision block for the complete GBT link.

The BO-CDR circuit retimes individually each received GBT word bit from the recovered *rx_word_clk* clock domain to the local *rx_frame_clk* clock domain (indicated as ϕ_0 in Figure 4.5), with the exception of the 4 bits of the header field which are not used by other firmware blocks in the TilePPr. This solution requires the implementation of 116 BO-CDR circuits per GBT link for a total of 1,856 circuits to retime the 4 GBT links.

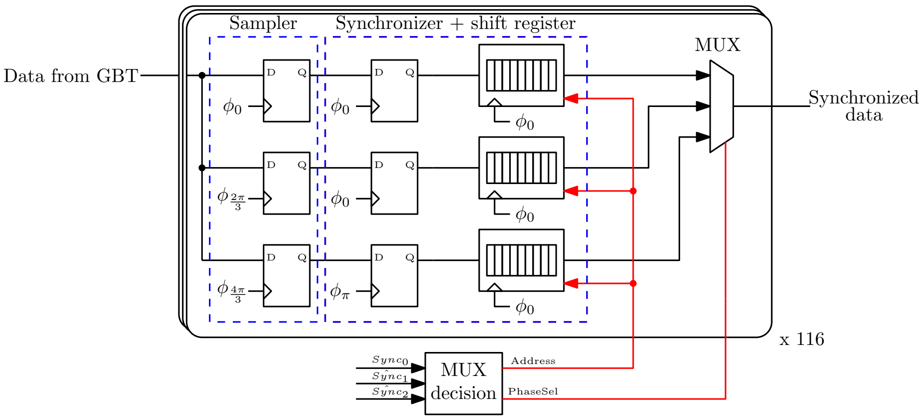


Figure 4.5: Block diagram of the BO-CDR circuit.

The principle of operation of the BO-CDR consists of oversampling the received data using 3 copies of a local generated *rx_frame_clk* shifted 120° in phase from each other. This technique, called 3X oversampling, is represented in Figure 4.6.

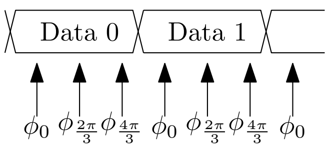


Figure 4.6: Concept of the 3X oversampling technique.

Therefore, the received data is registered using the 3 samplers shown in Figure 4.5 and retimed into the local *rx_frame_clk* clock domain using the synchronizers and shift registers. The retimed data is stored in the 3 shift registers and the MUX decision block selects which of the 3 copies will be sent out of the GBT-FPGA IP core versions through the data multiplexer (MUX).

Figure 4.7 shows a block diagram of the decision MUX block. It implements a phase picking algorithm which performs the selection for the entire GBT word based on the value of the $sync_x$ signals at the *rx_frame_clk* frequency for every received GBT word.

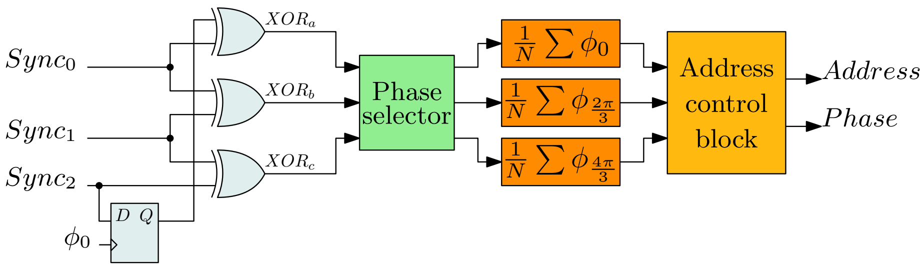


Figure 4.7: Block diagram of the MUX decision block.

The $sync_x$ corresponds to the resulting signals of 3X oversampling the HG/LG bit with the circuit shown in Figure 4.8. As will be covered in the uplink data format section, the HG/LG bit is used to identify the sample gain of the incoming data. This bit was found to be the more adequate since it toggles each clock cycle, providing more statistics to the decision block than any other bit.

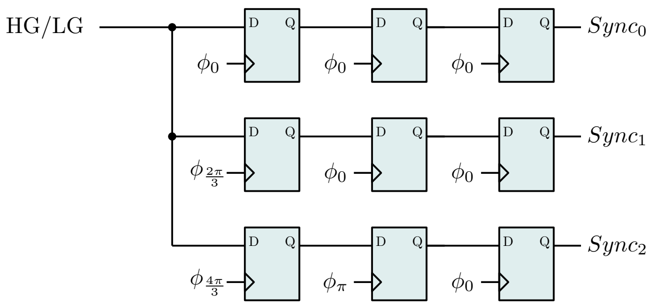


Figure 4.8: Synchronization circuit implemented for the acquisition and retiming of the HG/LG bit.

After the reception of the $sync_x$, the transition edges of the HG/LG are easily found by applying the XOR operation between two adjacent samples. The results of the XOR operation are passed to the Phase Selector which provides the result to the moving average blocks. Then, the Address Control block compares the output of the moving average blocks and the position of the MUX changing the shift register addresses if needed.

The phasor diagram corresponding to the implemented phase picking algorithm is shown in Figure 4.9, where the black arrow represents the phase of the transition edge with respect to the local *rx_frame_clk*, the red arrow is the phase of the selected data and φ_d is the phase between the received data and the local *rx_frame_clk*.

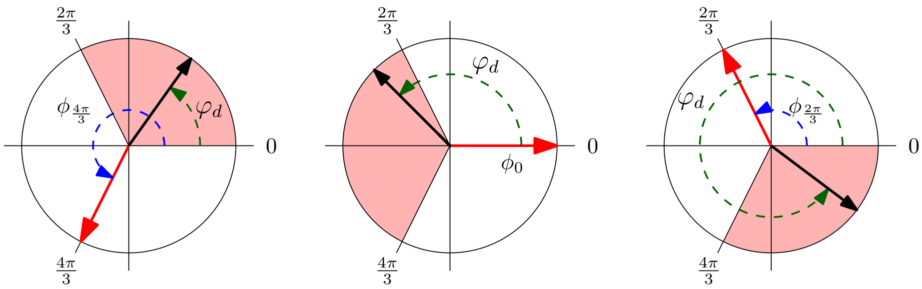


Figure 4.9: Phasor diagram describing the operation of the phase picking algorithm implemented in the MUX decision block.

Therefore, the MUX decision block can select the output data depending on three different situations:

- If $0 < \varphi_d < 2\pi/3$ then the selected clock phase is $\phi_{4\pi/3}$.
- If $2\pi/3 < \varphi_d < 4\pi/3$ then the selected clock phase is ϕ_0.
- If $4\pi/3 < \varphi_d < 2\pi$ then the selected clock phase is $\phi_{2\pi/3}$.

This circuit is also capable of compensating the phase drifts produced between the clocks due to temperature and/or voltage variations in the electronics, since it is continuously selecting the most appropriate clock phase to register the incoming data. However, a special situation occurs when the phase between both varies and the MUX decision block changes the selected data from ϕ_0 to $\phi_{\frac{4\pi}{3}}$, or vice versa. Since the same address of the three shift registers points to data acquired at different LHC clock cycles, this situation produces the displacement of one local *rx_frame_clk* clock cycle in the received data stream. In order to prevent this mis-synchronization the MUX decision block compensates the missing or added clock cycle adjusting the address of the shift registers in real time.

Finally, there is another important operation that the MUX decision performs to time stamp the received data properly. As already commented, the front-end electronics transmit the high and low gain samples at the LHC frequency corresponding to one LHC clock accompanied with the HG/LG bit. In order to time stamp the samples with the correct BCID, during the initialization of the BE GBT-FPGA links the MUX decision block checks the value of the HG/LG with respect to the local *tx_frame_clk*. If both signals are not properly aligned the MUX decision block adds a delay of half *tx_frame_clk* cycle to the output data with the shift registers.

The final architecture of the Tile GBT-FPGA IP core implemented in the TilePPr is shown in Figure 4.10, where the MMCM was replaced by a BO-CDR circuit and the *rx_frame_clk* clocks are generated with the same MMCM (not shown in this figure) used to generate the local *tx_frame_clk* clock.

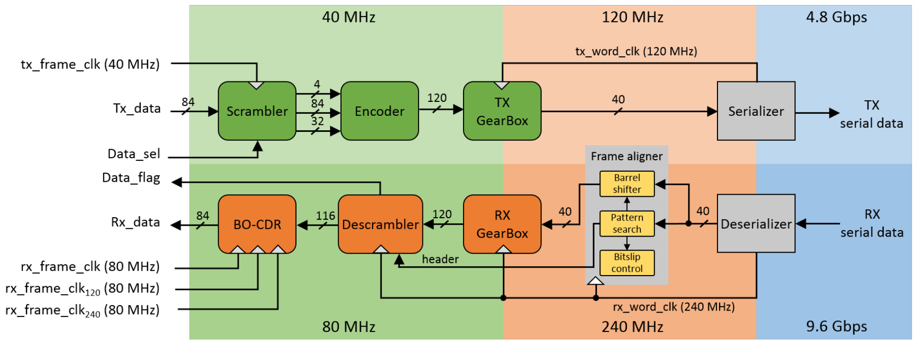


Figure 4.10: Block diagram of BE Tile GBT link.

4.3 Data format

The data format for the communication with the upgraded readout electronics was defined to fulfill the requirements. All configuration commands needed for the operation of the module, the JTAG data for the remote configuration and the LHC clock are distributed via the downlink. The uplink path transports all the readout data from the front-end electronics, monitoring data and configuration status of the module.

4.3.1 Downlink data format

The downlinks communicate the TilePPr prototype with the GBTx chips and FPGAs in the DaughterBoard using a GBT link configured in Frame mode. The data format for the downlink is different depending on its destination.

FPGA downlink

The FPGA downlink is used to transmit the configuration commands, read back requests and the Bunch Counter Reset (BCR) signal. The 84-bit words are distributed as indicated in Table 4.3. Commands are addressed to different DB registers by encoding the DB Address field.

83 50	**49**	**48**	**47 32**	**31 0**
Not used	BCR	N	DB Address	Data

Table 4.3: Data format fields in the downlink. Bit N indicates that the received command is new and therefore the corresponding register has to be updated with the data contained in the Data field.

GBTx downlink

The GBTx downlink is employed to distribute the LHC clock to the FPGA transceivers, to transmit the JTAG signals for remote configuration and reset of the DaughterBoard FPGAs. In the back-end electronics, the TilePPr prototype encodes the JTAG and reset signals into the downlink GBT word and the GBTx propagates the decoded signals to the FPGAs. The TMS, TCK and TDI signals are transmitted through the GBTx while the corresponding TDO is transmitted by the FPGA not being programmed. The data format for controlling the remote programming and resets is shown in Table 4.4. Only the lower 24 bits of the GBT word are used.

A sketch of the connections between the GBTx in side A and the DaughterBoard FPGAs is represented in Figure 4.11. The second GBTx in side B is

23 22	**21 20**	**19 18**	**17 16**	**15 8**	**7 6**	**5 4**	**3 2**	**1 0**
TMS B	TDI B	RST B	TCK B	N.U.	TMS A	TDI A	RST A	TCK A

Table 4.4: GBTx downlink data format.

connected to the FPGAs in the same way but receiving the signal through the QSFP in side B.

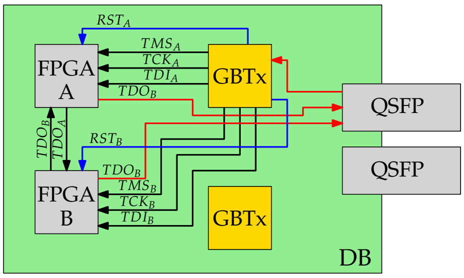


Figure 4.11: Connections between the GBTx chip and the DaughterBoard FPGAs for QSFP A.

4.3.2 Uplink data format

The DaughterBoard transmits a data word including high and low gain samples, integrator data and monitoring data at the LHC clock frequency. As already described in the previous section, the uplink implements the Wide-Bus GBT mode in order to increase the data bandwidth. Thereby, since the Wide-Bus mode does not implement the FEC algorithms, the last two bytes of the uplink GBT word are reserved for the CRC that uses bits from 115 to 16 bits as input. Then, the CRC permits the detection of errors occurred in the uplink communication path. The CRC algorithm was implemented as a LSFR circuit and XOR gates. The polynomial G(x) employed for the communication is stated in Equation 4.1.

$$G(x) = 1 + x^1 + x^2 + x^4 + x^7 + x^{12} + x^{16} \tag{4.1}$$

The readout and integrator data are transmitted at the LHC clock frequency using 80 bits of the GBT word. Table 4.5 describes data format used for the uplink. For every period of the LHC clock, two GBT words are transmitted to the TilePPr prototype. In the first half period the low gain samples from 6 PMTs are transmitted, and in the second half period the high gain samples of the 6 PMTs. Five bits are reserved for the integrator data. The integrator data words are divided in 5 bit words following the format described in the Integrator block section. Additionally, the BCR signal received in the front-end electronics is transmitted back to the TilePPr prototype. As will be discussed in next chapter, the BCR signal is used to calculate the latency of the links in units of BC.

95 91	**90**	**89**	**88**	**87 76**	**75 64**	**63 52**	**51 40**	**39 28**	**27 16**
Integrator	NU	HG/LG	BCR	PMT6	PMT5	PMT4	PMT3	PMT2	PMT1

Table 4.5: Data format fields in the uplink for the readout and integrator data. The HG/LG bit represents the gain, being 1 the high gain and 0 low gain.

The upper bits of the GBT word are used to read back the front-end electronics configuration and to monitor the DCS values. As for the DB commands, it consists of a 16-bit address and 32-bit argument. Since the DCS and TTC field has 20 bits, each transmission is performed using three consecutive GBT words. The two Most Significant Bits (MSB) are used to index the parts of the total message. The format of a fragment to read back the configuration is defined in Table 4.6.

Word	**113 112**	**111 96**
1	00	0x0000
2	01	DB Address
3	10	Parameter[31..16]
4	11	Parameter[15..0]

Table 4.6: Data format fields in the uplink for the TTC and DCS data.

4.4 Front-end electronics firmware

In this section the firmware blocks implemented in the DaughterBoards are described. Figure 4.12 shows a block diagram of the main functional blocks of the firmware.

4.4.1 Data Packer

The Data Packer handles the DB registers that are used for remote operation and configuration of the front-end electronics and builds the uplink GBT word with the readout and monitoring data. A set of nine 32-bit registers interface the different blocks shown in Figure 4.12 with the TilePPr in the back-end

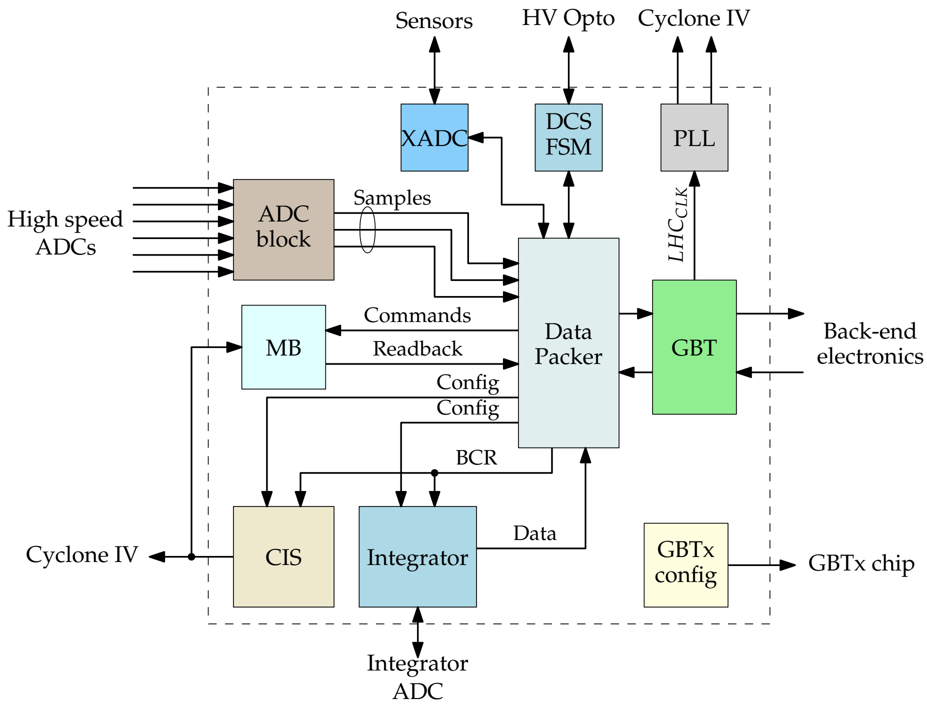


Figure 4.12: Block diagram of the DaughterBoard firmware.

electronics. A summary of the register list and the description is shown in Table 4.7.

The Data Packer decodes the downlink GBT words to fill the corresponding DB registers that are used for controlling the rest of the firmware blocks. Moreover, the Data Packer builds the uplink GBT word with the data received from the different firmware blocks as the Integrator and the DCS module. The Data Packer also extracts the data contained in the DB registers adding it to the uplink GBT word. The DB registers are continuously read in a circular way only interrupted when the TilePPr prototype requests the reading of a MainBoard register.

The Data Packer uses the received BCR signal to synchronize the data transmission sending a complete set of high and low gain samples for every LHC clock cycle. Therefore, the data packing of the samples is deterministic in terms of latency since samples corresponding to the same BCID are aligned with the BCR.

Description	**Type**
MainBoard command	W
Firmware version	R
Read back commands FPGA 0	R
Read back commands FPGA 1	R
XADC reading	R
Soft Error Mitigation	R
Integrator	R/W
Status/ operation of the HVOpto	R/W
Read back / direct CIS commands	R/W

Table 4.7: Registers for the operation of the DaughterBoard, where the W indicates that the register can be only written, R that the register can be only read and R/W that the register can be either read or written.

4.4.2 MainBoard Interface module

The MainBoard Interface module provides a communication path between the DaughterBoard and the MainBoard through an SPI port. The MainBoard is populated with four Altera Cyclone IV FPGAs each one controlling 3 channels. The DaughterBoard receives the commands from the Data Packer and routes them to the appropriate MainBoard FPGA. The MainBoard commands permit the complete configuration of the FEBs, integrator ADCs, and fast readout ADCs.

The MainBoard commands use 24 bits: 3 bits are reserved for the type of command, 5 bits for the MainBoard FPGA and channel ID, and 16 bits for the command and data. The data format is presented in Table 4.8.

23	**22**	**21**	**20 18**	**17 16**	**15 0**
T	E	B	FPGA	channel	command and data

Table 4.8: Data format of the commands transmitted to the MainBoard FPGAs.

The encoding of the 3 MSB bits for the selection of the command type is represented in Table 4.9. Bits from 20 to 16 are used to select the FPGA and channel or to send the commands in broadcast. The encoding of the FPGA and channel fields are indicated in Table 4.10 and 4.11.

T	E	B	Command type
1	0	0	CIS timing and ADC commands (T commands)
1	0	1	Read back of timing and ADC register values (B commands)
0	1	0	TTC commands (E commands)
0	0	1	Read back of TTC commands (B commands)

Table 4.9: Header identification code for the 3-in-1 commands.

20 18	FPGA
000	A0
001	A1
010	B0
011	B1
1XX	All FPGAs

Table 4.10: MainBoard FPGA identification code.

The distribution of the command and data fields depends on the type of command. For the TTC commands (E), the 4 MSB bits are reserved to define the type of command and the 12 LSB bits for data. In the case of the Timing and ADC commands (T) the 3 MSB bits are reserved to define the type of command and the 13 LSB bits are for data.

TTC commands

The TTC commands (E) are used for configuration of 3-in-1 boards and integrator ADCs on the MainBoard. These commands allow the configuration of 3-in-1 cards for physics, CIS calibration runs or to disable the trigger outputs. A summary of the functionalities controlled through the E commands is listed below:

- Configuration the DACs driving the pedestal of the fast ADCs.
- Configuration of the internal switches of the 3-in-1 for physics data taking or CIS.
- Control of DAC that charge the capacitors for CIS.
- Charge and discharge of the capacitors for CIS.
- Configuration of the Integrator gain.
- Enable / disable the trigger output.

17 16	**PMT**
00	Channel 1
01	Channel 2
10	Channel 3
11	All channels

Table 4.11: PMT identification code.

Timing and ADC commands

The Timing and ADC commands (T) can be CIS phase timing commands or ADC commands. The CIS timing commands configure the phase of the TPH and TPL pulses that initiate the charge and discharge the capacitors. The T commands permits the adjustment of the peak CIS pulse with the sampling clock in steps of 16/25 ns. Also T commands are used to configure the ADCs. Through the MainBoard FPGAs, the ADCs can be configured to send data patterns for the alignment of the serial data in the DB, reset, or read internal values of the ADC.

Read back commands

The execution of read back commands (R) generates a 18-bit word which includes the PMT ID, last executed command and the corresponding data field. The use of R commands is very helpful during the operation of the module to verify that the commands have reached the FPGAs in the MainBoard. After the execution of a R command, the DB collects the requested data from the MainBoard FPGAs and transmits it to the TilePPr through the uplink.

4.4.3 Charge Injection System block

The Charge Injection System can be controlled using the TPH and TPL lines which connects the DB with the Cyclone IV FPGAs, or executing E commands to configure the internal switches of the 3-in-1 cards.

The CIS block controls the charge and discharge of the small and large capacitors by toggling the TPH and TPL lines. TPH controls the small capacitor to calibrate the high gain circuitry while TPL controls the large capacitor for low gain calibration. This block is configured from the back-end electronics with the BCID positions when the capacitor has to be charged and discharged. The value of the DAC is configured through a non-synchronous command from the TilePPr.

4.4.4 Integrator block

The Integrator block reads out the integrator ADCs in the MainBoard through the I^2C bus. Each 16-bit ADC present in the MainBoard digitizes the integrated current from the 3-in-1 card integrator. The integrator block requests a new ADC sample every pre-programmed number of orbits, and then transmits the samples to the Data Packer. The number of orbits is configured through the Integrator DB register from Table 4.7.

Since 4 bits of the uplink word are reserved for the integrator data, the transmission of an integrator sample requires 5 clock cycles of *tx_frame_clk*. Thus, the integrator data is divided in 5 blocks as indicated in Table 4.12.

Word	95	94 91
1	V	Channel ID
2	V	3..0 bits
3	V	7..4 bits
4	V	11..8 bits
5	V	16..12 bits

Table 4.12: Data format and sequence of the integrator words transmitted to the TilePPr. The V bit indicates that the received data is valid.

4.4.5 GBTx configuration module

The GBTx configuration module is implemented with a 8-bit PicoBlaze Processor [70] which configures the GBTx chips via a I^2C interface. The PicoBlaze is connected to a 100 MHz local oscillator and loads the configuration of the GBTx chip every time the DaughterBoard is powered on. This module configures the GBTx enabling all the output clocks required to drive the GTX transceivers and the e-links needed for the remote JTAG configuration and resets through the GBTx chip. In addition, timeout and watchdog capabilities are included in the present GBTx configuration to monitor the correct operation of the chip and reset the internal FSMs if needed. Once the configuration of the GBTx satisfies the requirements for the Demonstrator, the GBTx chips will be permanently programmed with the desired configuration, and the PicoBlaze processor will be used to reconfigure the GBTx chip and for monitoring purposes.

4.4.6 Monitoring block

Xilinx series 7 FPGAs include a Xilinx Analog-to-Digital Converter (XADC) block composed of a dual 12-bit ADC operating at 1 Msps and some on-chip sensors to measure internal voltages and temperatures. Some of the Daughter-Board FPGA pins can be used to connect analog signals and digitize with the internal XADC block. In the DaughterBoard 10 analog inputs are connected to the XADC block for remote monitoring of the module parameters. The monitor block reads out four internal FPGA measurements from the XADC block, including voltages and temperatures, and eight external measurements corresponding to the MainBoard voltages and the module temperatures. All these values are sequentially written in the XADC register and transmitted to the TilePPr.

4.4.7 DCS module

The DCS module handles the communication with the HVOpto board for the operation and monitoring of the PMT blocks through the 40-pin connector in the DB. This module is only functional in minidrawers equipped with the HVOpto board to provide the high voltage to the PMTs. The communication protocol used between the DaughterBoard FPGA and the MAX chip in the HVOpto board is SPI. The DCS module converts the received commands from the TilePPr to SPI and communicates with the MAX chip in the HVOpto board. The DCS module receives the commands from the TilePPr through the HVOpto register. DCS commands are used to enable or disable the HV channels, set the HV values or request a measurement reading from the MAX chip temperature and voltage sensors.

4.4.8 ADC block

The ADC block module is one the most critical pieces in the DB firmware. This block deserializes the data coming from 6 dual-channel 12-bit ADCs (LTC2264-12) at a data rate of 560 Mbps per ADC channel. The MainBoard ADCs generates a 14-bit word samples in serial mode per channel corresponding to the digitization of the analog input signal, where the 12 MSB bits contain the sample data and the two remaining bits are present to ensure software compatibility with the 14-bit version of these ADCs. Synchronous with the serial data, the ADC provides two auxiliary signals: a 280 MHz clock signal, called *bit_clk*, which is used to register the serial data in Double Data Rate (DDR) mode; and a 40 MHz clock signal, called *frame_clk*, which delimits the word boundaries of deserialized word. Figure 4.13 shows the timing diagram of data and clock signals provided by the ADC chip for the configuration used in the MainBoard.

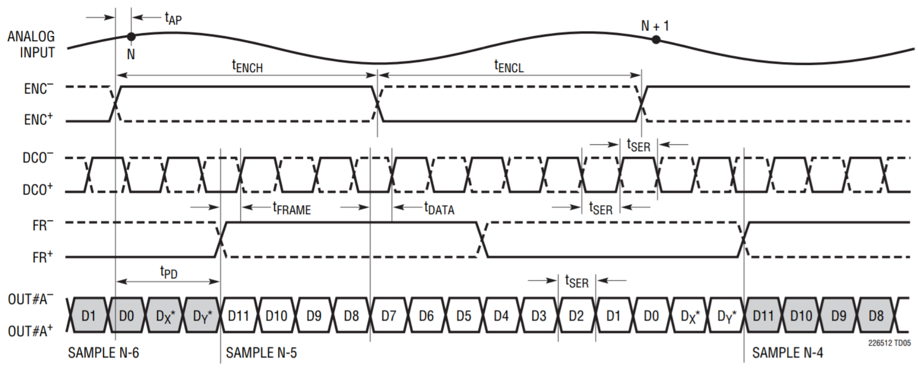


Figure 4.13: Timing diagram of the ADC data and clock signals. *FR* signal is the *frame_clk*, *DCO* is the *bit_clk* and *OUT* the output data. Extracted from [71].

In the DaughterBoard, two ISERDESE2 blocks [72] are used per ADC channel to deserialize the serial data into a 14-bit parallel word. The selection of a proper clocking architecture to provide the clocks to the ISERDESE2 is crucial for the correct deserialization. Most common clocking architectures for the implementation of ADC interfaces in FPGA includes an I/O clock buffer (BUFIO) to provide the *bit_clk* to the ISERDESE2 blocks through a dedicated clocking network, and a second clock seven times slower than the *bit_clk*, called *frame_clk_local*, which is generated from the *bit_clk* with a regional clock buffer (BUFR). This clocking architecture is recommended for source-synchronous data capture since it ensures phase alignment between the *bit_clk* and the *frame_clk_local*.

However, the phase relationship between the generated *frame_clk_local* and the incoming *frame_clk* is unknown since the output phase of the BUFR after its initialization can not be predicted. Figure 4.14 shows a timing diagram of the deserialization process using the ISERDESE2 blocks with a factor 4, where *frame_clk_local* and *frame_clk* have a different phase.

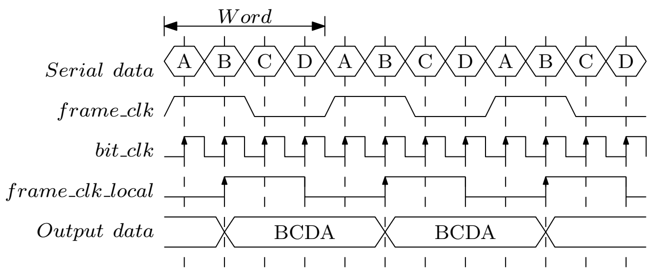


Figure 4.14: Timing diagram for the deserialization of a 4-bit word with the ISERDESE2 block.

Most applications not requiring deterministic latency implement this clocking architecture and uses a dedicated block of the ISERDESE2 to shift bits of the parallel data up to it is aligned with *frame_clk*. This shift-bit operation in the ISERDESE2 could introduce a non-deterministic latency in the outputs under some situations [73]. Furthermore, since the deserialized data is clocked with *frame_clk_local* and has to be retimed to the *rx_frame_clk* domain a latency uncertainty of one LHC clock cycle is introduced in the output of the ADC block.

Therefore, an alternative method was developed to achieve word alignment with deterministic and fixed latency using the ISERDESE2 blocks and the recommended clocking architecture.

As shown in Figure 4.15 the proposed method keeps the same clocking architecture, where the *frame_clk_local* is generated from the *bit_clk* using a BUFR. After the initialization of the DaughterBoard, the *frame_clk* is deserialized using the *bit_clk* and the *frame_clk_local*. The parallel word is passed to the Word

Alignment FSM (WA-FSM) which reinitializes the BUFR with a reset signal until the deserialized *frame_clk* is equal to 11111110000000, indicating that *frame_clk* and *frame_clk_local* are phase aligned. In order to obtain a different output phase after resetting the BUFR, the WA-FSM delays the reset signal for every iteration in steps of one *bit_clk* period using a shift register.

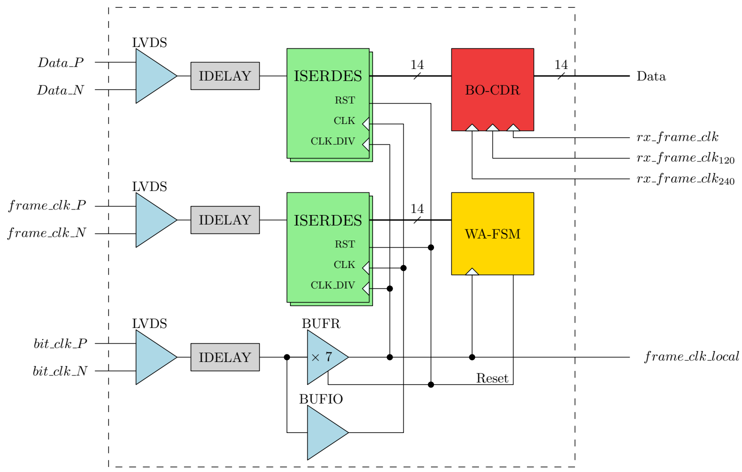


Figure 4.15: Block diagram of the ADC block including the WA-FSM and the BO-CDR.

Thereby, the ADC block monitors and aligns the *frame_clk_local* and *frame_clk* phases, where it is important to remark that the phase difference between *frame_clk* and *rx_frame_clk* (sampling clock distributed to the ADCs) is fixed by design [71]. In addition, input data signals were delayed using the IDELAY blocks in order to compensate the internal delays between the clock and the data and provide sufficient timing margin for sampling the data.

Finally, there still exists a CDC issue since the data is synchronous with *frame_clk* and has to be retimed to the LHC clock in the DaughterBoard for the transmission to the Data Packer. This CDC issue was resolved adding a BO-CDR circuit at the output of the ISERDESE2.

4.5 Back-end electronics firmware

Different blocks were implemented in the TilePPr for the operation of the Demonstrator module. This section gives a detailed description of the design of the TilePPr prototype firmware. Figure 4.16 depicts a block diagram of the main functional blocks of the TilePPr firmware.

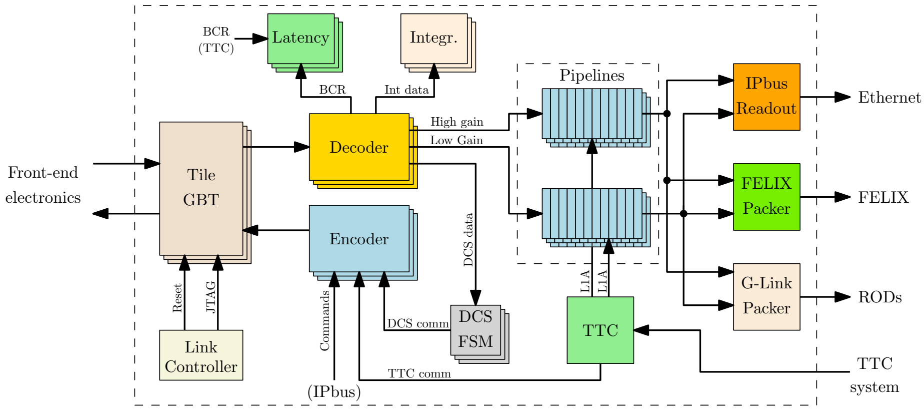


Figure 4.16: Simplified block diagram of the TilePPr prototype firmware designed to operate the Demonstrator module.

4.5.1 IPbus

The Readout FPGA is controlled via a Gigabit Ethernet port operated with the IPbus protocol [74]. The IPbus protocol is a IP-based control protocol designed for handling the data transaction between FPGA-based ATCA systems and computers.

The software communicates with the FPGA-based devices through standard UDP or TCP connections establishing a bidirectional client-server architecture. The remote access to the clients is achieved by software through the mapping of a virtual 32-bit address space to 32-bit registers in the FPGAs. The IPbus protocol supports individual read and write operations on all the registers in the FPGAs.

The data handling between the software applications and the IPbus module in the TilePPr is managed by a software application called Control Hub. The Control Hub manages simultaneous access of multiple software applications to the TilePPr. The communication between the software applications and the

Control Hub is implemented using TCP/IP while the communication between the Control Hub and the TilePPr is UDP/IP.

The TilePPr IPbus registers are accessed through specific-designed software applications written in C++ and Python which permits the control and configuration of the TilePPr and the Demonstrator. For this purpose, almost one thousand 32-bit registers were implemented in the TilePPr firmware.

4.5.2 Link Controller

The Link Controller manages the resets and remote JTAG chain through two IPbus registers. It can individually reset the transmission and reception parts of the GBT links by the assertion of specific bits of the IPbus register. In addition, the Link Controller can also reset the DB FPGAs remotely.

The second register is used to decide which DaughterBoard and FPGA is included in the remote JTAG chain. Therefore, through this register, the Link Controller configures the internal multiplexers to access one FPGA at a time externally.

4.5.3 Encoder

The Encoder builds the GBT word which will be transmitted to the front-end electronics. It encodes the commands with the proper data format and BCR signals. There is one Encoder per GBT link, where each can receive commands from three different sources: IPbus registers, DCS FSM, and from the TTC module.

From the IPbus registers the Encoder manages two types of commands: asynchronous or synchronous commands. The asynchronous commands are formatted and transmitted to the front-end electronics as soon as they are received, while the synchronous commands are transmitted every orbit at a specific BCID.

Commands received from the IPbus path are defined using 2 IPbus registers: address and argument registers. The address register indicates to the Encoder the destination of the command specifying minidrawer, DB side, and the DB register. The argument register contains the data to be written in the DB register. Table 4.13 presents the data format for the synchronous and asynchronous commands.

31	30 28	27 16	15 14	13	12	11 0
NU	MD Index	BCID	NU	Broadcast	DB side	DB register address

Table 4.13: Data format of the address register for the propagation of commands. Where the MD index field indicates the minidrawer destination and the BCID field is maintained empty for the asynchronous commands.

Synchronous and asynchronous commands can be transmitted to a single DaughterBoard FPGA specified with the 16 upper bits of the address register, or in broadcast reaching to all the DaughterBoard FPGAs asserting the corresponding bit. An example of synchronous commands are the TTC commands. They are used to configure the switches of the 3-in-1 cards during the CIS calibration runs. Other kind of commands as the configuration of the input bias voltage of the ADCs or the high voltage settings are not required to be executed at a certain BCID and are encoded as asynchronous commands.

The TTC commands received from the TTC module are translated into commands that the front-end electronics can process. Since the legacy TTC commands are directly formatted by the Encoder and transmitted to the front-end electronics, the type of TTC command defines if they have to be executed at a specific BCID or not.

Finally, the DCS commands are received from the DCS FSM. They are only transmitted for those minidrawers hosting the HVOpto boards since these commands are employed for the management of the high voltage system in the front-end electronics.

4.5.4 DCS FSM

The DCS FSM in the TilePPr prototype interfaces the DCS software and the TilePPr prototype to control and monitor the HVOpto boards. The DCS computer sends commands and requests to the TilePPr through the IPbus interface which are received and formatted in the DCS FSM before being transmitted to the Encoder. In addition, the DCS FSM handles the DCS information of the HVOpto boards. The FSM sends the voltage and temperature from the individual HVOpto channel to the DCS computer.

4.5.5 TTC module

One of the key modules implemented in the Readout FPGA is the TTC module. This module, in combination with the ADN2814 chip presented in Chapter 3, emulates some of the functionalities of the TTCrx chip. The ADN2814 chip recovers a version of the LHC clock with four times the original frequency (160 MHz), in addition to the encoded TTC data at 160 Mbps. The recovered clock and data are then passed to the TTC module in the Readout FPGA where the TTC stream is decoded.

The TTC information is encoded in BiPhase Mark (BPM) to provide a proper DC-balance, and includes two Time Division Multiplexed (TDM) channels (channel A and B). The channel A is dedicated for the propagation of the L1A signals and channel B is used to transmit commands from the TTC crates to the detector electronics. The TDM BPM encoding of the TTC channels is shown in Figure 4.17.

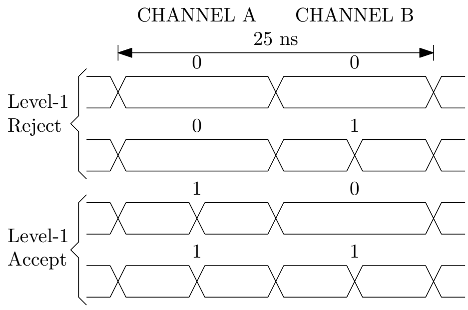


Figure 4.17: TDM BPM encoding.

There are two types of B-channel commands: broadcast and addressed commands. Broadcast commands are executed by all the receivers, while the addressed commands are only executed by those receivers which have the indicated TTC address. The B-channel commands are also Hamming encoded providing the capability to detect up to two bit errors and correct a single bit error per frame. Some examples of broadcast commands are the BCR or ECR signals, while the commands used for the configuration of the internal switches of the 3-in-1 cards are addressed.

Therefore, the TTC module implements all the functionalities required to decode the legacy TTC stream. The decoded B-channels are converted to the new commands and transmitted to the Encoder for its transmission to the front-end electronics and the L1A signals are propagated to the pipeline memories and L1A counters.

In addition, the TTC module can be configured to operate in two different modes:

- External mode: where the L1A and BCR received from the TTC system are propagated to the front-end electronics.
- Internal mode: where the propagated TTC signals are generated locally in the TilePPr. The BCR is generated internally with a 12-bit counter with the possibility of limiting to 3563 BC (1 orbit) and the L1A signal is controlled with an IPbus register.

For the physics operation mode, the TTC module is set to external mode to receive the L1A and B-commands from the legacy TTC system, while the internal mode is used for calibration runs and testing.

4.5.6 Decoder

The Decoder is the first module after the GBT receiver module. Each Decoder (Figure 4.18) routes the data received from four GBT links (A0,A1,B0 and B1) to other firmware blocks.

The link selection between the redundant A0 and A1 channels or B0 and B1 channels can be configured in auto or manual mode. When configured in auto mode, the Decoder blocks selects dynamically one of the two redundant links based on the result of the comparison between the computed and the original CRC codes included in the incoming frame. If an error is detected in one of the redundant links, then the other link is flagged as valid. However, when configured in manual mode, the Decoder selects a specific channel regardless the result of the CRC checking.

Finally, after the channel has been selected, the Decoder converts the frame in subframes and routes them to the different firmware blocks for further processing.

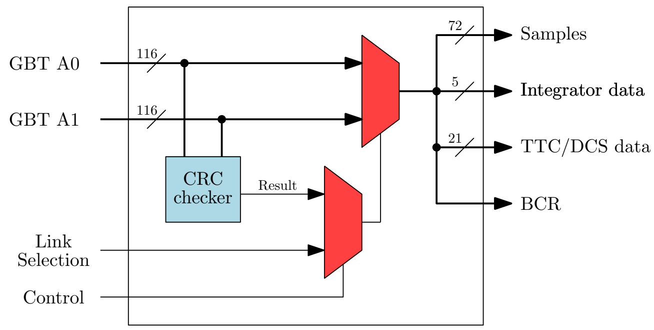


Figure 4.18: Block diagram of the Decoder. Only A0 and A1 channel are shown for simplicity.

4.5.7 Integrator Readout block

There is one Integrator Readout block per GBT link receiving the integrator subframes from its corresponding Decoder. Each Integrator Readout block includes a FSM to build the integrator data from the received subframes and to store the results in twelve 512-position FIFO memories, each one dedicated to a FEB channel.

The integrator data is read out from the FIFO memories using the IPbus interface. The FIFO memories act as elastic buffers to prevent the data loss when the FIFOs can not be read during short periods of time since the CPU does not allocate time for the execution of the integrator readout application.

4.5.8 Pipeline module

The pipeline modules store the received data from high-speed ADCs in internal memories. Upon the reception of a L1A signal, the selected samples are transferred to different readout paths. This module acts as a elastic buffer to absorb the data generated by consecutive L1A signals, thus avoiding the data loss.

The pipelines were implemented using dedicated RAM-blocks in order to save FPGA logic resources. There is one complete pipeline module per gain and channel for a total of 96 pipeline modules (48 channels x 2 gains). Figure 4.19 shows the complete block diagram of a pipeline module.

A pipeline module consists of one Main Pipeline (MP), two Derandomizer Memories (DM) connected to the ROD and FELIX interfaces and one IPbus Memory Block (IMB) for the IPbus readout path. The MP blocks are implemented using a 18 Kb RAM-block segmented in 512-sample positions, being capable of storing up to 12.8 μs of samples. The DM are implemented in the same type of RAM-blocks but segmented in 16 pages of 16-sample positions each, and IMB blocks in 16 pages with 32-sample positions.

Three Control blocks handle the storage of the samples into the 96 pipeline modules and the data transfer to the Event Packers.

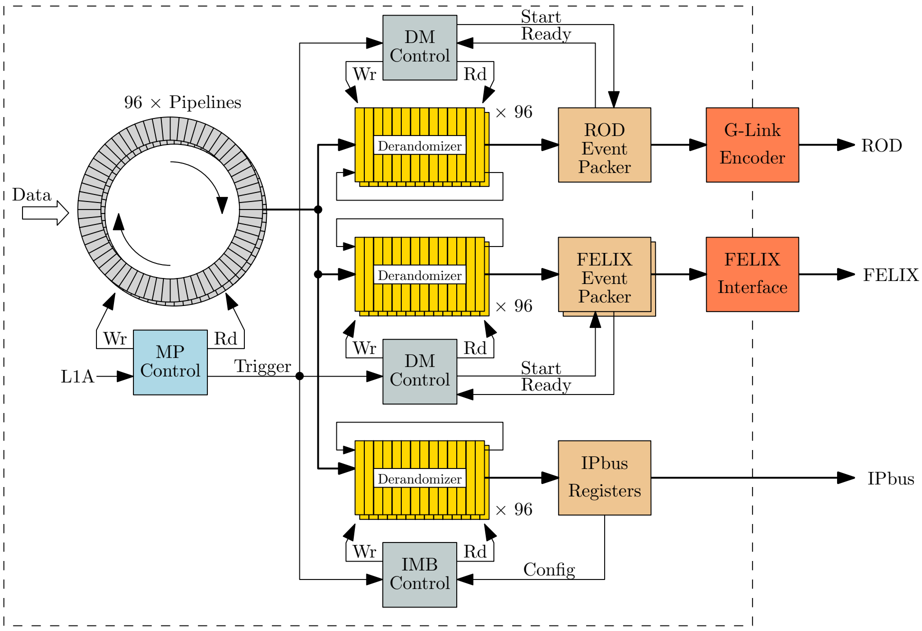


Figure 4.19: Block diagram of the pipeline modules, Event Packers and readout interfaces.

The MP receives samples from the Decoder and stores them in a circular buffer at the LHC clock frequency. The MP control block timestamps the incoming sample with the corresponding BCID and manages the write address port by incrementing a 9-bit counter by 1 for each LHC clock cycle.

When the MP Control block receives a L1A signal from the TTC system, the current write address is copied to a pointer table. Then, the Control block transfers to the DM and IMB memories the 16 data samples previous to the memory address stored in the pointer table. This handling of pointers avoids the event loss when a second L1A is received during the transaction of data selected by a previous L1A.

The DM control block handles the data flow between the DM memories and the Event Packers. The DM control block receives and stores the selected data from the MP in the DM memories, and initiates a handshake (start, ready) with the Event Packers to transfer the data corresponding to 96 channels at once. Again, the DM blocks includes a table of pointers with memory addresses to avoid data loss during the transaction of selected data to the Event Packers, and the transmission of event fragments to the FELIX and ROD systems.

The IMB operates in a different way than the DM. It can be configured in blocking or unblocking modes. When it is configured in unblocking mode, the IMB operates similarly to the DM block but storing 32 samples instead of 16 samples. However, since the data bandwidth of the IPbus interface is not fast enough to read out all the selected data the IMB memories are eventually overwritten. The unblocking operation mode is only intended for testing and to adjust the pipeline delay with respect to the time arrival of the L1A signal. This is achieved by adjusting the memory addresses stored in the pointer table of the MP block. On the other hand, when the IMB is configured in blocking mode, the reception of new L1A signals is blocked until the selected data is read from the memories.

4.5.9 Readout interfaces

The TilePPr prototype is read out through two different interfaces: the legacy ROD and the FELIX system.

The Event Packers format the selected samples before they are transmitted to the legacy ROD and FELIX system through dedicated interfaces. They also handle the data flow between the pipelines and the interface paths through the Control blocks. Both Event Packers operate in the same way, when the MP receives a L1A signal, 16 high and low gain samples are copied from the DM blocks to an intermediate register-based memory. After the handshaking process between the Event Packers and the DM Control blocks is completed, the Event Packers build an event fragment which is transferred through the interface blocks to the next systems in the DAQ architecture.

ROD interface

The ROD Event Packer builds the event fragment using the ROD format and controls the G-Link encoder to transmit the data to the RODs. The TilePPr formats the data using the same format as the legacy modules to be the backward-compatible with the legacy system.

Table 4.14 shows the general ROD packet structure composed of a header and trailer, 16 DMU blocks with samples from 3 PMTs each, DMU chip mask word and the computed CRC word. The size of the all DMU block is the same and depends on the configuration parameters of the Event Packer. The following options can be tuned:

- Number of samples: 1 to 16 samples (7 samples is the default value).
- Truncate mode: selected sample bits are 10 MSB, 10 to 1 MSB or 10 LSB. This option is not configurable in the legacy system, being intended to perform more accurate studies on the digital noise of the Demonstrator module.
- Gain: high/low gain, auto-gain or bi-gain. In the auto-gain mode the high gain samples are transmitted unless the samples are overflowed or underflowed. If this happens, low gain samples are transmitted. In the bi-gain mode both gains are transmitted at the same time.

Header - Start of Packet
DMU 1 Data block
...
DMU 16 Data block
DMU Chip Mask Word
Global CRC
Trailer - End of the Packet

Table 4.14: TileCal ROD data event format. The size of the DMU data blocks depend on the operation mode.

Finally, the G-Link encoder encodes the formatted words in frames of 20 bits using the Conditional Inversion with Master Transition (CIMT) coding, and drives a FPGA transceiver for data transmission to the ROD. The G-Link encoder block was designed based on the functionalities implemented by the

Agilent HDMP 1032 transmitter chip [75] used in the Interface boards of the current system.

FELIX interface

The FELIX interface block includes four Event Packers, where each one collects the data from the pipelines of one minidrawer and builds a FELIX event packet. The FELIX packet structure, shown in Table 4.15 includes 16 high and low gain consecutive samples for 12 channels from one minidrawer. As before, the number of samples included in the event fragment can be configured from 1 to 16 samples, with 16 as the default value.

FELIX Header - Start of Packet	
Run parameters	
BCID	MD ID
L1A ID	
HG sample 2 Ch1	HG sample 1 Ch1
...	
HG sample 16 Ch12	HG sample 15 Ch12
LG sample 2 Ch1	LG sample 1 Ch1
...	
LG sample 16 Ch12	LG sample 15 Ch12
FELIX Trailer - End of Packet	

Table 4.15: FELIX raw data event format. The Run parameters field defines all the relevant parameters such as the number and type of run, or the DAC value in the case of a CIS run. On the other hand, the MD ID field includes the minidrawer number, BCID field includes the BCID corresponding to the first sample and L1A ID field the L1A number in the run.

The selected data is transmitted through a standard GBT link to the FELIX system at 4.8 Gbps. The GBT link used for communication with the FELIX system is operated in Frame mode. The user data field is divided into 10 frames of 8 bits, with each frame corresponding to one e-link [24].

4.5.10 Latency block

There are four Latency blocks in the Readout FPGA to measure the Round-Trip Time (RTT) of the GBT links in units of LHC clock cycles. The Latency block counts the number of clock cycles between the transmitted BCR to the front-end electronics and the received BCR. The result is accessed through an

IPbus register. This block permits a fast way to detect latency variations in the digital path greater than 25 ns which would produce the incorrect time stamping of the incoming data.

4.6 Data path delays and latency measurements

This section presents the measurements performed to obtain the latencies of the data acquisition path of the Demonstrator module. The data acquisition path can be separated in two different paths: the digital and the ADC interface paths. The digital delay path only includes the communication latency between the DaughterBoardd and the TilePPr through the GBT links, while the ADC interface path delay comprehends the delays between the fast ADCs and the deserialization and retiming modules in the DaughterBoard.

4.6.1 Digital path latency measurements

The digital path delay (δ_t) for the Demonstrator is not symmetric. The delays associated to the downlink transmission (δ_d) and the uplink transmission (δ_u) are not equal due to the different structure and configuration of the GBT links. As indicated in Equation 4.2, the digital path latency is calculated as the sum of δ_d and δ_u.

$$\delta_t = \delta_d + \delta_u \tag{4.2}$$

As mentioned above, the TilePPr firmware contains a block to calculate the RTT in number of LHC clock cycles. Equation 4.3 defines the RTT of the digital path as the sum of both delays rounded to the higher integer number.

$$RTT = \left\lceil \delta_d + \delta_u \right\rceil \tag{4.3}$$

The RTT was measured in a testbench composed of a TilePPr prototype and a DaughterBoard connected through a 3 meter fiber (Figure 4.20). The delay between the transmitted and received BCR was measured using a Lecroy WavePro 760Zi oscilloscope. The result of the measured RTT is 450 ns, which agrees with the value of 18 clock cycles (18 × 25 ns) measured with the Latency block. Figure 4.21 shows a screenshot of the Chipscope software [76] used to perform this test.

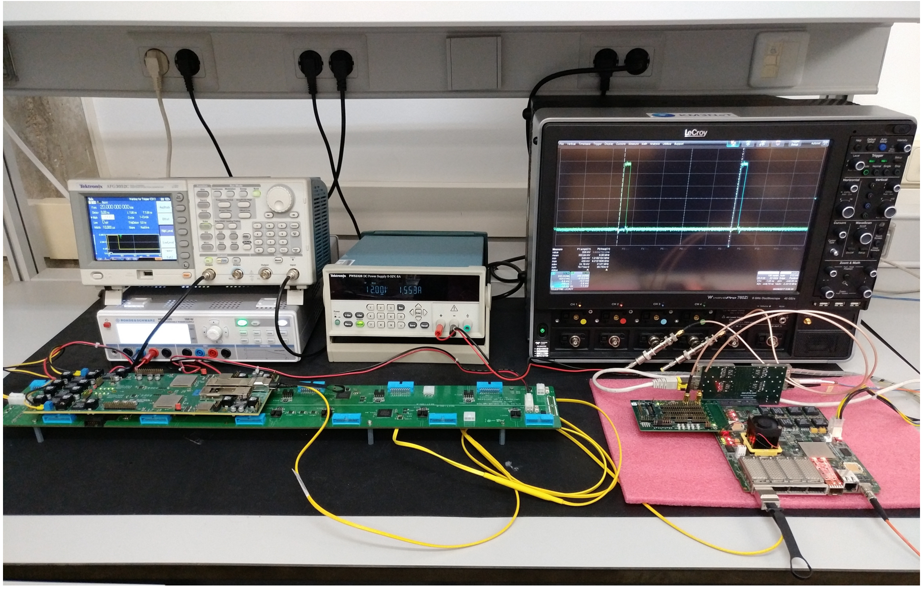


Figure 4.20: Testbench for the digital path delay measurement.

The delays of the uplink and downlink were measured individually with the oscilloscope to obtain the δ_u and δ_d values. For this measurement, BCR signals in the DaughterBoard and TilePPr were connected to external pins. The δ_d measured between the transmitted BCR signal in the TilePPr and the received BCR signal in the DaughterBoard results in a delay of about 242 ns. However, the measured latency in the uplink is lower with a value of about 208 ns since the Tile GBT block and the transceivers for the uplink operates two times faster.

The measured latency values agree with the expected latencies for the uplink and downlink. Table 4.16 and Table 4.17 summarize the latency introduced by each transmitter and receiver block of the GTX transceiver, according with the information provided by Xilinx [77]. The latencies added by the Tile GBT-FPGA IP core and other firmware blocks involved in the uplink and downlink communication are shown in Table 4.18.

An amount of latency is added when received data is retimed into the local *rx_frame_clk* (80 MHz) domain. The added latency depends on the arrival time of the data and the selected clock phase in the BO-CDR for sampling the data. For this reason, the retiming process introduces a latency between 11 and 14

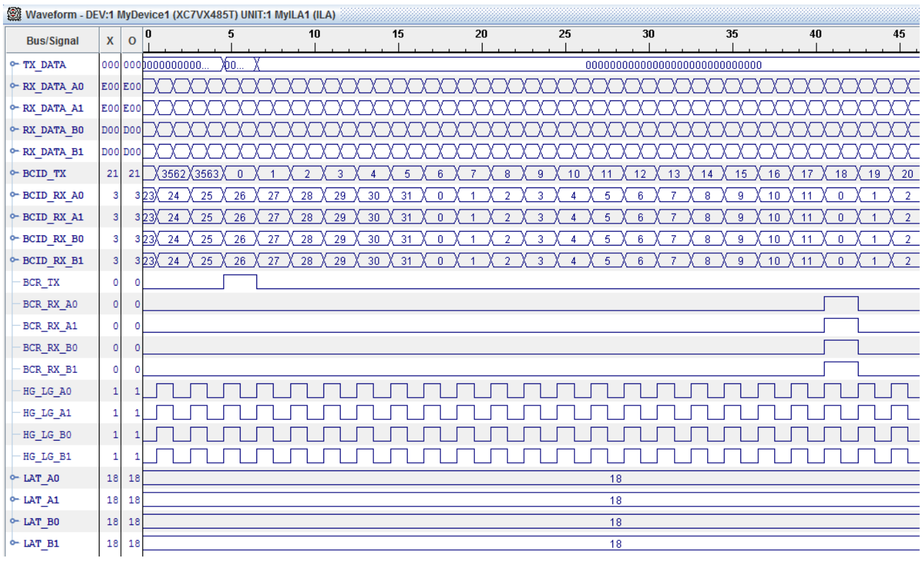


Figure 4.21: Screenshot of the Chipscope software where BCR_TX signal corresponds to the transmitted BCR, the BCR_RX signals to the received BCR, and LAT values corresponds to the RTT calculated by the Latency block.

rx_word_clk (240 MHz) cycles. In addition, the BO-CDR could add three more *rx_word_clk* cycles in order to adjust the RTT latency to the higher integer number of LHC clock cycles.

The rest of the delay is due to the optical modules and propagation delay over the fibers (estimated as 4.9 ns/m for single mode fibers [78] [79]), propagation delay over the PCB traces and latencies of the clock distribution inside the FPGAs.

	Downlink		Uplink	
Block	***tx_word_clk* cycles (120 MHz)**	**Time (ns)**	***tx_word_clk* cycles (240 MHz)**	**Time (ns)**
FPGA interface	2	16.63	2	8.32
Buffer (bypassed)	1	8.32	1	4.16
PMA interface	1	8.32	1	4.16
PMA	1.54	12.78	1.54	6.39
Total	**5.54**	**46.05**	**5.54**	**23.02**

Table 4.16: Latency introduced by the transmitter GTX transceiver blocks according to the downlink and uplink configuration. PMA stands for Physical Medium Attachment sublayer.

Block	Downlink *rx_word_clk* cycles (120 MHz)	Downlink Time (ns)	Uplink *rx_word_clk* cycles (240 MHz)	Uplink Time (ns)
FPGA interface	2	16.63	2	8.32
Comma detect	1	8.32	1	4.16
PMA	5.21	43.35	5.21	21.67
Total	**8.21**	**68.3**	**8.21**	**34.15**

Table 4.17: Latency introduced by the receiver GTX transceiver blocks according to the downlink and uplink configuration.

Module		Downlink *tx/rx_word_clk* cycles (240 MHz)	Downlink Time (ns)	Uplink *tx/rx_word_clk* cycles (240 MHz)	Uplink Time (ns)
TX	**Tile GBT**	7	58.22	4	16.33
	Data Packer	-	-	3	12.48
RX	**Tile GBT**	6	49.9	7	29.11
	BO-CDR	-	-	15	62.38
Total		**13**	**108.12**	**29**	**120.59**

Table 4.18: Latency introduced by the firmware blocks for the downlink and uplink communication. The Data Packer and BO-CDR blocks are only present in the uplink.

4.6.2 ADC interface path latency

The time between the arrival time of the pulse signal by the ADCs and the reception of the digitized pulse in TilePPr prototype was also measured. The complete latency of the uplink (δ_{fe}), including the ADC interface path, is defined in Equation 4.4 and corresponds to the sum of δ_u and the acquisition time of the digitized signals (δ_{ADC}).

$$\delta_{fe} = \delta_u + \delta_{ADC} \tag{4.4}$$

Figure 4.22 shows a block diagram of the testbench used for the measurement of the ADC interface path delay. The function generator Tektronix AFG3052C was configured to generate a 10 μs wide square pulse triggered with the transmitted BCR signal from the TilePPr, and then the output of the function generator was connected to the input of one ADC.

In order to measure the delay from the ADC input to the output of the deserialization block (δ_{ADC}), the MSB of the deserialized ADC data in the DaughterBoard was routed to an external pin. Then, the δ_{ADC} was measured as the time difference between the rising edge of the square pulse in the input

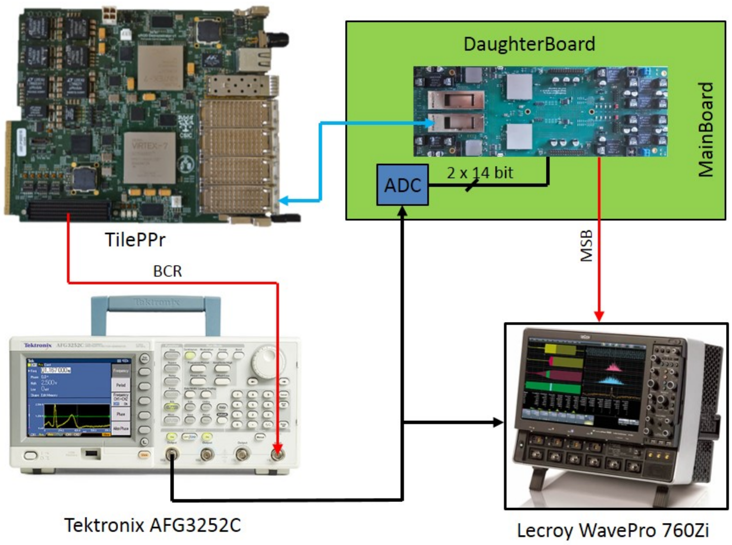


Figure 4.22: Testbench for the ADC interface path delay measurement.

of the ADC and the rising edge of the MSB.

The measurement showed a δ_{ADC} of about 297 ns. According to the manufacturer specifications, the ADC pipelines introduce a latency of 6 LHC clock cycles, plus about 4.67 ns associated with the propagation delay of the acquired signal in the ADC [71]. Also, 5 LHC clock cycles more corresponds to the delay introduced by the deserialization block and the BO-CDR implemented in the DaughterBoard FPGA. The rest of the latency is due to the data retiming process and the propagation delay over the PCB traces.

Therefore, according to Equation 4.4, δ_{fe} takes a value of about 505 ns using a 3 meter long fiber. Again, this value was confirmed by measurement of the time difference between the pulse injection into the ADC and the reception of the digitized pulse in the TilePPr.

ADC deserializer tests

A similar setup was also used to validate the deterministic behavior of the deserialization block in terms of latency. The delay between the arrival time of the received BCR and the arrival time of the pulse signal (δ_p) was measured in number of LHC clock cycles. For the realization of this measurement, a simple pulse detector (Figure 4.23) was connected to the output of the GBT receiver.

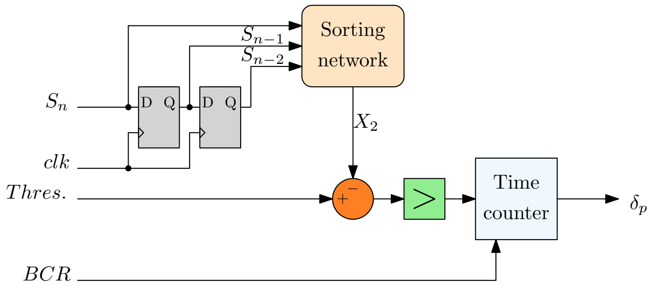


Figure 4.23: Block diagram of the pulse detector block.

The pulse detector includes a sorting network [80], a comparator, a subtractor and a time counter. The implemented sorting network sorts the last three received samples S_{n-2}, S_{n-1} and S_n to X_1, X_2 and X_3 where is always satisfied that $X_1 \leq X_2 \leq X_3$. The sorting network filters possible sample spikes that would produce false triggers by the selection of the X_2 sample.

Figure 4.24 shows a diagram of the implemented sorting network, where each branch joining two paths represents a block containing a 2-input comparator and a switch. The branches switch the paths when the bottom input is higher than the top one, and keep unchanged the paths when the bottom input is lower or equal to the top one.

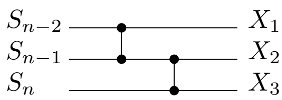


Figure 4.24: Representation of a sorting network for sorting 3 inputs.

The measured δ_p value kept constant during extensive tests where the testbench was power cycled and the transceivers were reset. Therefore, the fixed and deterministic latency of the ADC interface path was confirmed.

Chapter 5

Clock distribution in the Tile Calorimeter

After the ATLAS Phase II Upgrade, the PreProcessor will be responsible for the distribution of the clock to digitize the PMT analog signals in the front-end electronics, and also for the synchronization of the readout electronics with the overall ATLAS DAQ system.

Variations in the propagation delay of the transmitted clock could occur during the operation due to voltage and temperature variations in the electronics and fibers. Moreover, some elements of the high-speed communication links could also have a non-deterministic latency producing time variations in the distributed clock.These time variations will cause phase shifts of the clock distributed to the front-end electronics which have to be detected and monitored for compensation prior to data taking.

In this thesis, a FPGA based circuit called OverSampling to UnderSampling (OSUS) is proposed for the detection of latency variations and phase drifts between clocks with a precision of about 30 ps_{RMS}. The performance of the proposed OSUS circuit is also compared with the Digital Dual Mixer Time Difference (DDMTD) circuit. This chapter also discusses the implementation of the OSUS circuit in the TilePPr prototype to synchronize the TTC system and the TilePPr, studies of the clock quality, phase drift monitoring and stability of the link latency.

5.1 Current clock distribution architecture

As described in Chapter 1, in the current DAQ architecture the TTC system distributes all the signals needed for the synchronization of the whole detector electronics and the LHC clock. Figure 5.1 shows a block diagram of the TTC distribution in the TileCal detector.

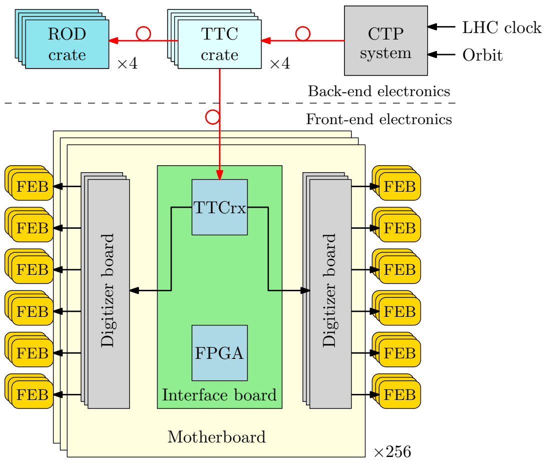


Figure 5.1: Sketch of the current clock distribution architecture for the TileCal detector.

During physics data taking, the CTP receives the LHC clock and the orbit signal from the LHC accelerator, and propagates them together with the Event Counter Reset (ECR), L1A and configuration signals to the Tile TTC crates [81]. Then, the TTC modules distributes the LHC clock and control signals to each one of the 256 TileCal modules through an individual optical fiber.

In the front-end electronics, the TTCrx ASIC recovers and distributes the LHC clock for the digitization of the PMT signals. When the front-end electronics receives a L1A signal from the CTP, the Interface board transmits the data and the corresponding BCID associated with the triggered event to the RODs. This BCID is compared with the one registered in the ROD to confirm that front-end and back-end systems are synchronized.

The TTCrx ASIC includes a dedicated circuitry to delay the recovered clock in steps of 104 ps in order to compensate the particles' time of flight and propagation delays associated with the signal acquisition. This delay is measured with timing calibration runs where the laser system [82] sends controlled light pulses to the PMTs via dedicated fibers and the TTCrx ASICs are configured to shift the phase of the sampling clock as close as possible to the peak of the digitized pulse. Finally, the fine tunning of the sampling clock phase is done with physics samples.

5.2 Clock distribution architecture in the HL-LHC

The clock distribution schema of the ATLAS experiment will be revised for the HL-LHC. In this new scenario, the TTC information will be distributed from the CTP to a number of Local Trigger Interface (LTI) boards and then to the FELIX systems. The LHC clock and TTC information will be transmitted between the different elements of the back-end electronics system using a bi-directional optical network running at 9.6 Gbps, called TTC Passive Optical Network (TTC-PON) [83].

Finally, the TilePPr will receive the clock and TTC information from the FELIX system through optical links using the GBT protocol and will propagate the TTC signals to the front-end electronics, where the clock will be recovered for the digitization of the analog signals and for the transmission of the digitized data to the back-end electronics. Figure 5.2 depicts a complete block diagram which describes the clock distribution schema in Tilecal for the HL-LHC.

Following the same clock distribution schema used in the current system, the front-end electronics will be equipped with a GBTx chip to recover and distribute the LHC clock to the FEBs for digitization.

5.2.1 Synchronization of the Demonstrator module

The architecture employed to distribute the clock to the Demonstrator module is a combination of the legacy system and the architecture proposed for the HL-LHC. In the Demonstrator, the legacy TTC system provides the LHC clock and TTC information to the TilePPr prototype. Then, the TilePPr prototype distributes the LHC clock to the front-end electronics over 16 GBT links running

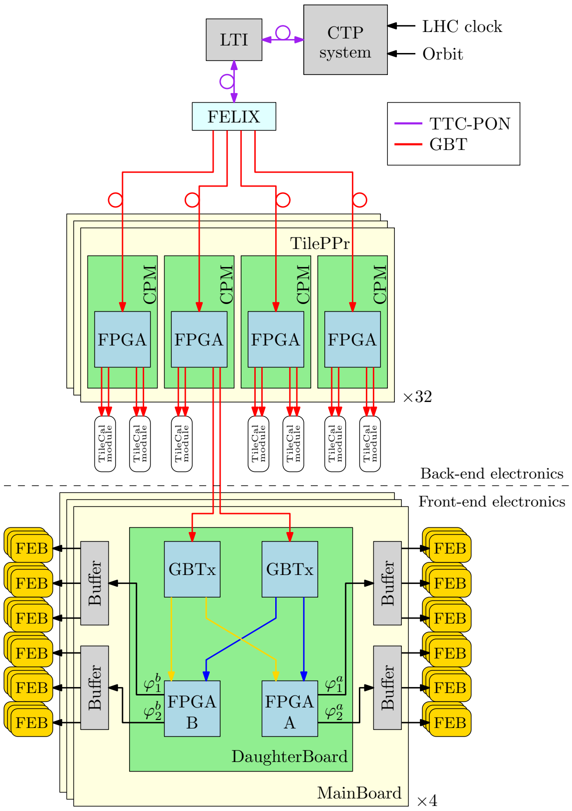


Figure 5.2: Sketch of the clock distribution schema in TileCal for the HL-LHC.

at 4.8 Gbps. The LHC clock is then recovered by the GBTx in the Daughter-Boards, and distributed to the ADCs in the MainBoard for the digitization of the PMT signals.

However, the clock distribution to the front-end electronics requires the measurement of the phase difference between the LHC clock, recovered from the TTC system, and the internal clocks generated in the TilePPr prototype to ensure the synchronization with the legacy DAQ system.

The main source of mis-synchronization is produced by the clock recovery stage in the TilePPr, where the recovered LHC clock takes an unknown phase due to the frequency conversions performed with the jitter cleaner (CDCE62005) to generate the frequency values required for the operation of the GBT links. In addition, the LHC clock phase can suffer small variations due to voltage and temperature drifts producing changes in the propagation delay of the electronics and fibers.

Therefore, the TilePPr prototype requires of a method to measure the phase difference between the clock provided by the TTC system and the clock transmitted to the front-end electronics. This method will provide synchronization between the front-end and back-end electronics by detecting and compensating for phase drifts during operations.

5.3 DMTD method

One popular circuit employed to measure the phase difference between periodic signals is the Dual Mixer Time Difference (DMTD) circuit. The DMTD circuit was present first by D.W. Allan in [84] to measure phase differences between analog signals. The DMTD circuit permits to obtain the phase relationship between two periodic signals with high resolution. Figure 5.3 presents a block diagram of the DMTD circuit.

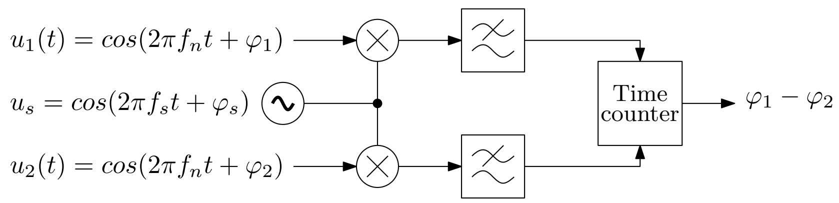


Figure 5.3: Block diagram of the analog DMTD circuit.

The two clocks $u_1(t)$ and $u_2(t)$ have the same clock frequency but an unknown phase relationship given by the difference between φ_1 and φ_2. Both clocks are mixed with a third clock signal $u_s(t)$ with slightly smaller frequency. Figure 5.4 shows the waveform of the signal resulting of multiplying u_s and u_1.

The mixing operation is mathematically described in Equation 5.1 as the multiplication of cosine signals.

$$\begin{aligned} u_1(t) \cdot u_s(t) &= cos(2\pi f_1 t + \varphi_1) \cdot cos(2\pi f_s t + \varphi_s) \\ &= \frac{1}{2} \cdot (cos(2\pi(f_1 + f_s)t + \varphi_1 + \varphi_s) + cos(2\pi(f_1 - f_s)t + \varphi_1 - \varphi_s)) \end{aligned} \tag{5.1}$$

The mixing operation between $u_1(t)$ and $u_s(t)$ results in a low frequency signal, called $U_1(t)$ and a high frequency signal which is filtered with a low pass

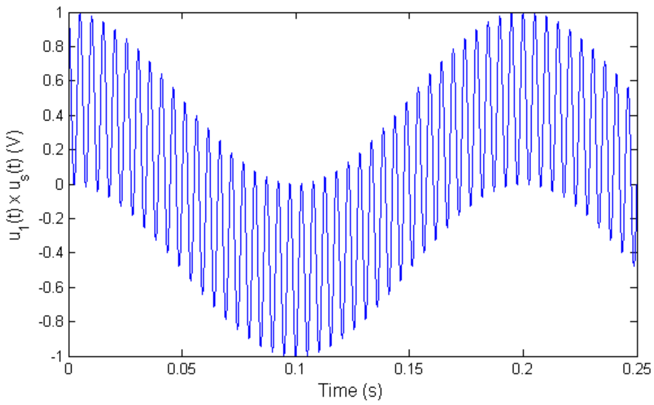


Figure 5.4: Waveform signal resulting from multiplying a 100 Hz signal (u_1) and a 95 Hz signal (u_s).

filter. $U_2(t)$ is obtained following the same procedure. The phase difference ($\Delta\varphi$) between the two resulting $U(t)$ signals is equal to the phase difference between the original clock signals.

$$U_1(t) = cos(2\pi f_U t + \varphi_1 - \varphi_s) \tag{5.2}$$

$$U_2(t) = cos(2\pi f_U t + \varphi_2 - \varphi_s) \tag{5.3}$$

$$\Delta\varphi = \varphi_1 - \varphi_2 \tag{5.4}$$

Therefore, the phase difference between $u_1(t)$ and $u_2(t)$ can be easily calculated using a time counter to measure the time difference between $U(t)$ signals (ΔT_U).

$$\Delta\varphi = \Delta T_U 2\pi f_U \tag{5.5}$$

The smaller difference between the frequency of the input signals and u_s results in a decrease of f_U as can be deduced from Equation 5.1, and then in an increase of the resolution of the method.

5.3.1 Digital approximation of the DMTD method

The digital approximation of the analog DMTD technique is based on sampling the input signals with a sampling rate close to the input frequency signal. The Nyquist theorem [85] establish that in order to sample all the changes of a signal, the minimum sampling rate has to be at least two times the highest frequency contained in the signal. Equation 5.6 refers to this condition in mathematical terms.

$$f_s \geq 2f_p \tag{5.6}$$

where f_s represents the sampling frequency and f_p the highest frequency contained in the signal.

Sampling the signals above f_s results in lower frequency signals, called alias signals. This technique is known as undersampling or subsampling. Figure 5.5 shows an example of an alias signal produced when a signal with a frequency f_p is undersampled at a sampling rate of $0.95 \cdot f_p$.

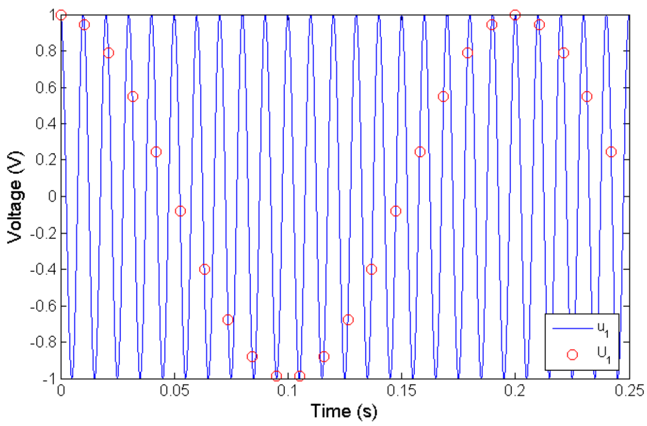


Figure 5.5: Waveform signal (U_1) resulting from undersampling a sinusoidal signal of 100 Hz (u_1) at 95 Hz.

The frequency of the alias (f_a) signal can be obtained from Equation 5.7.

$$f_a = |R \cdot f_s - f_p| \tag{5.7}$$

where R represents the closest integer multiple of f_s to f_p.

When a signal is undersampled, a fixed number of samples are generated for each period of the input signal. The number of alias samples can be derived from the aliasing theorems presented in [86].

$$L = \frac{1}{0.5 - \left|0.5 - \left(\frac{f_p}{f_s} mod 1\right)\right|} \tag{5.8}$$

where *mod* is the modulus operation.

The Digital DMTD circuit (DDMTD) [87] [88] uses two Flip-Flops (FFs) to sample two periodic digital signals with the same frequency and compares the phase difference between the output product signals. Figure 5.6 shows a block diagram of the digital implementation of the DMTD. The digital undersampling circuit or DDMTD is composed of two FFs for sampling the input signals, a PLL which generates the sampling clock, two debouncer blocks to filter glitches, and time counters to measure and monitor the phase difference of the resulting alias signals.

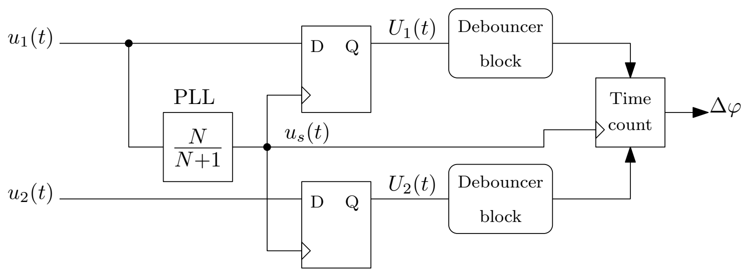


Figure 5.6: Block diagram of the DDMTD circuit.

Equation 5.7 shows that the closest frequency between the sampling clock and the input signal will produce the lower frequency of the alias signal. Since the alias signal phase is proportional to the input signal, the lower frequency will provide more accurate measurements. For this reason, the sampling clock is generated from one of the input clock signals using a PLL with a fractional factor close to 1. The frequency f_s of the sampling clock is presented in Equation 5.9.

$$f_s = \frac{N}{N+1} f_1 \tag{5.9}$$

where N corresponds to a positive number greater than 0.

Figure 5.7 shows an example of how the digital undersampling technique works. The U_1 and U_2 signals correspond to the alias signals resulted of undersampling u_1 and u_2 with u_s.

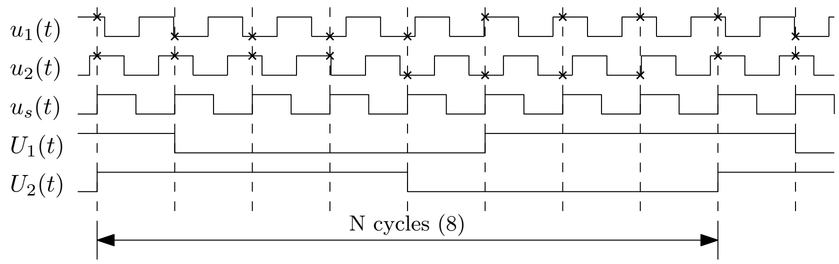


Figure 5.7: Timing diagram of the DDMTD circuit with N = 8.

Therefore, the resolution of the DDMTD circuit corresponds to the maximum time difference between u_1 and u_s, and it can be obtained by subtracting the input period and the sampling period as shown in Equation 5.10.

$$\begin{aligned}\Delta t_{max} &= T_s - T_1 = \frac{N+1}{N}T_1 - T_1 \\ &= \frac{1}{N}T_1 = \frac{1}{N+1}T_s\end{aligned} \tag{5.10}$$

The phase difference between u_1 and u_2 (ϕ_{12}) corresponds to the number of cycles of u_s from the rising edge of U_1 and the rising edge of U_2 multiplied by the time resolution.

$$\phi_{12} = \frac{1}{N+1}T_s n_{cycles} \tag{5.11}$$

where n_{cycles} is the number of cycles of u_s between the rising edges of U_1 and U_2.

Since f_s/f_1 is close to 1, the number of samples for each period of the input signal is equal to N. This equality can be easily deduced from Equation 5.12 for $N > 1$.

$$L = \frac{1}{\frac{f_1}{f_s} - 1} = N \tag{5.12}$$

A demonstration of the equivalence between the operation of the digital DMTD circuit and the analog one is presented below. Equation 5.13 shows the discretized form of Equation 5.1 where t has been replaced by nT_s.

$$
\begin{aligned}
u_1(n) \cdot u_s(n) = &\frac{1}{2} \cdot (cos(2\pi(f_1 + f_s)nT_s + \varphi_1 + \varphi_s) \\
&+ cos(2\pi(f_1 - f_s)nT_s + \varphi_1 - \varphi_s)) \\
&= \frac{1}{2} \cdot (cos(2\pi f_1 nT_s + n2\pi + \varphi_1 + \varphi_s) \\
&+ cos(2\pi f_1 nT_s - n2\pi + \varphi_1 - \varphi_s)) \\
&= \frac{1}{2} \cdot (cos(2\pi f_1 nT_s + \varphi_1 + \varphi_s) + cos(2\pi f_1 nT_s + \varphi_1 - \varphi_s))
\end{aligned} \tag{5.13}
$$

where n corresponds to the sample number and is a natural number.

Applying the Euler identity for the cosine, Equation 5.13 can be rewritten as follows.

$$
\begin{aligned}
u_1(n) \cdot u_s(n) &= \frac{1}{2}\left(\frac{e^{j(\alpha+\varphi_s)} + e^{-j(\alpha+\varphi_s)}}{2} + \frac{e^{j(\alpha-\varphi_s)} + e^{-j(\alpha-\varphi_s)}}{2}\right) \\
&= \frac{1}{2}\left(e^{j\varphi_s} \cdot \frac{e^{j\alpha} + e^{-j\alpha}}{2} + e^{-j\varphi_s} \cdot \frac{e^{j\alpha} + e^{-j\alpha}}{2}\right) \\
&= \frac{1}{2}\left(e^{j\varphi_s} \cdot cos(\alpha) + e^{-j\varphi_s} \cdot cos(\alpha)\right) = cos(\varphi_s) \cdot cos(\alpha)
\end{aligned} \tag{5.14}
$$

where $\alpha = 2\pi f_1 nT_s + \varphi_1$.

Then, the discretized form of the multiplication of u_1 and u_s can be expressed as Equation 5.15.

$$
\begin{aligned}
u_1(n) \cdot u_s(n) &= cos(\varphi_s) \cdot cos(2\pi f_1 T_s n + \varphi_1) \\
&= cos(\varphi_s) \cdot cos(2\pi \frac{N+1}{N} n + \varphi_1) \\
&= cos(\varphi_s) \cdot cos(2\pi \frac{1}{N} n + \varphi_1)
\end{aligned} \tag{5.15}
$$

The frequency of the signal product of u_1 and u_s is equal to the frequency f_U of the alias signal in the DDMTD circuit shown in Equation 5.16.

$$
f_U = f_1 - f_s = \frac{1}{N} f_s \tag{5.16}
$$

Finally, $u_1 \cdot u_s$ is redefined as U_1 under the conditions shown in 5.17 to represent it as a digital signal.

$$U_1(n) = \begin{cases} 1, & \text{if } -\frac{\pi}{2} < (2\pi\frac{1}{N}n + \varphi_1) < \frac{\pi}{2}. \\ 0, & \text{if others.} \end{cases} \tag{5.17}$$

Note that, since the generated U signals are referenced to u_s, the argument φ_s presented in Equation 5.15 is equal to 0.

5.4 OverSampling to UnderSampling method

Implementing multiple DDMTD circuits in a FPGA for the monitoring of different frequency signals is a complex task since each DDMTD circuit requires a complete set of PLLs and clock buffers for the generation of the u_s signal. The reduced number of clocking resources in FPGAs limits the possibility of implementing a large number of DDMTD circuits in the same design.

A modification of the original architecture of the DDMTD circuit is proposed in this thesis. The OverSampling to UnderSampling (OSUS) circuit makes possible to measure the phase difference between multiple clock signals with different frequencies using a unique PLL component.

The principle of operation of the OSUS circuit consists of oversampling the input signals with a sampling clock that has a fractional frequency multiple of u_1 and bigger than one. Then, the oversampling signal is decomposed in alias signals, called U, by selecting and grouping the output samples. The frequency of the sampling clock for the OSUS circuit is defined in Equation 5.18.

$$f_s = M\frac{N}{N+1}f_1 \tag{5.18}$$

where M and N are natural numbers. M corresponds to the oversampling factor and N is the PLL factor also used in the DDMTD circuit.

Figure 5.8 depicts a block diagram of the OSUS circuit describing its operation. The OSUS circuit produces M alias signals that are sent to M debouncer blocks and M time counters. A Phase Control block passes the selected samples to the debouncer blocks controlling a demultiplexer.

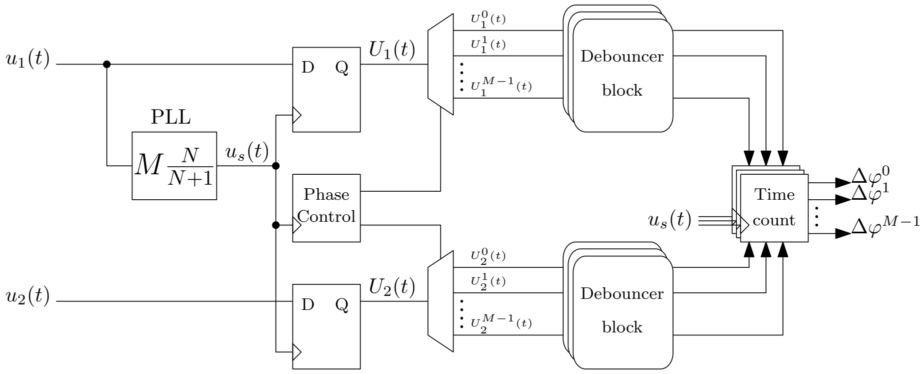


Figure 5.8: Block diagram of the OSUS circuit.

The complete operation of an OSUS circuit with $N = 8$ and $M = 4$ is presented in the timing diagram of Figure 5.9. Signal u_1 corresponds to one of the two input signals and is sampled with u_s generating the oversampled U_1 signal. Finally, the Phase Control block constructs the four U_1^k signals separating the samples in intervals of MT_s.

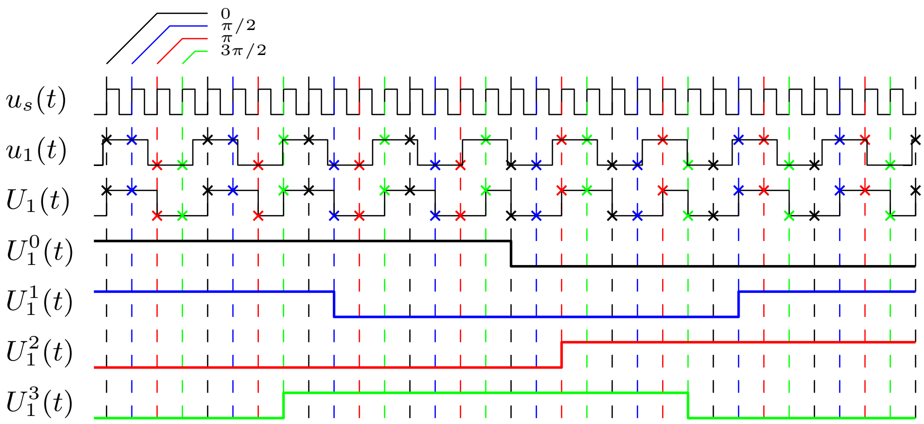


Figure 5.9: Timing diagram of the OSUS circuit with $N = 8$ and $M = 4$.

The waveform of the oversampled U signal in the digital domain is defined in Equation 5.19.

$$U(n) = \begin{cases} 1, & \text{if } -\frac{\pi}{2} < (2\pi\frac{1}{N}Mn + \varphi_1) < \frac{\pi}{2}. \\ 0, & \text{if others.} \end{cases} \tag{5.19}$$

In addition, as can be observed in Figure 5.9, each of the decomposed alias signals U^k have a different phase offset corresponding to a multiple of $\frac{2\pi}{M}k$. The U^k signals are constructed selecting the value of the oversampled U signal each $k+M$ samples. The waveform of the decomposed alias signals can be expressed as follows.

$$U^k(n) = \begin{cases} 1, & \text{if } -\frac{\pi}{2} < (2\pi\frac{1}{N}n + \frac{2\pi}{M}k + \varphi_1) < \frac{\pi}{2}. \\ 0, & \text{if others.} \end{cases} \tag{5.20}$$

where k represents the index of U and takes values from 0 to $M-1$.

Therefore, as can be deduced from Equation 5.20 the advantage of the OSUS method over the DDMTD circuit is the increase in statistics with the factor M, since the OSUS circuit produces M times more measurements than the DDMTD circuit keeping the same time resolution.

5.4.1 Performance of the OSUS circuit

In this section the performance of the OSUS circuit and the DDMTD circuit are compared considering two figures of merit: the measurement rate and the acquisition time.

Measurement Rate

The measurement rate is referred here as the minimum time between two phase measurements. While the phase measurements done with the DDMTD circuit are separated in time a complete period of U^k, the OSUS circuit provides phase measurements separated in time in steps of U^k/M. Thereby, the measurement rate increments by a factor M with respect to the DDMTD. The improvement in the measurement rate could be useful for applications using the DDMTD circuit as part of a control loop.

Acquisition time

On the other hand, the acquisition time refers to the number of T_s periods needed to collect a complete set of measurements. For the DDMTD method the acquisition time is defined in Equation 5.21.

$$Ft_{uc} = (K-1)NT_s + \Delta\varphi_U \tag{5.21}$$

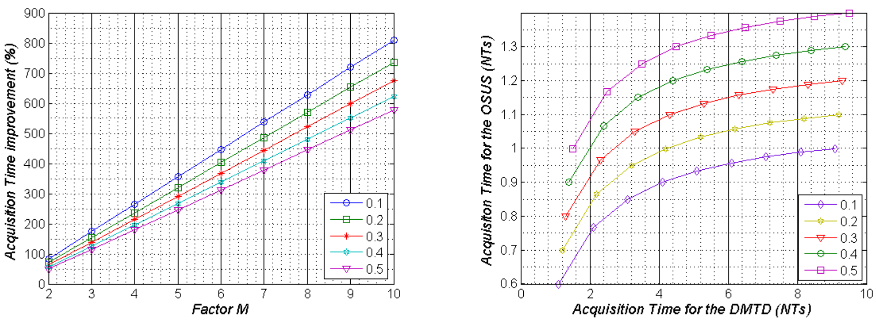
where K corresponds to the number of samples to be acquired and $\Delta\varphi_U$ is the phase difference between the U signals being compared.

The acquisition time for the OSUS circuit is lower than for the DDMTD circuit. Equation 5.22 refers to the time needed to acquire K samples with an OSUS circuit with $M = K$.

$$Ft_{OSUS} = \frac{K-1}{K}NT_s + \Delta\varphi_{U^k} \tag{5.22}$$

where $\Delta\varphi_U^k$ is the phase difference between the U^k signals being compared.

A comparison between the acquisition time of the DDMTD and the OSUS circuit is presented in Figure 5.10 (a) and (b). Each line represents a different $\Delta\varphi_U$ with values between $0.1 \cdot T_U$ and $0.5 \cdot T_U$.



(a) Acquisition time improvement of the OSUS circuit over the DDMTD circuit. Each line represents the acquisition time improvement in percentage for M measurements varying the factor M. Five $\Delta\varphi$ cases are presented taking values from $0.1 \cdot T_U$ to $0.5 \cdot T_U$.

(b) Comparison between the OSUS circuit and the DDMTD circuit acquisition times. Each line corresponds to the acquisition time for M measurements. Five $\Delta\varphi$ cases are presented taking values from $0.1 \cdot T_U$ to $0.5 \cdot T_U$.

Figure 5.10: Comparison of the acquisition time of the OSUS and the DDMTD circuit for different phase shifts.

Debouncing techniques

The theoretical resolution of the DDMTD and OSUS circuits is affected by the jitter in the clock signals and metastability in the samplers. During the sampling of the input signals, a high number of glitches are produced in the transition edge of the U^k signals affecting to the precision of the measurements and the transition edge of the U^k. Different debouncing methods to estimate position of the positive edge of U signals were presented in [89] and [90] to mitigate this problem in the DDMTD circuit: First Edge (FE), Positive Edge Median, Zero Count(ZC) and Center-Of-Mass. The debouncing circuit provides a time estimation of the rising edge of the U^k signal.

In this thesis, a new method based on the Average Position (AP) is used to estimate the position of the positive edges. The AP method is compared with other techniques with similar complexity as the FE, Last Edge (LE) or ZC methods.

A brief description of the compared debouncing methods is given below.

- First Edge estimates the positive edge time position as the first positive edge detected.
- Last Edge estimates the positive edge time position as the last positive edge detected.
- Zero Count counts the number of ones and zeros produced during the glitch period and estimates the positive edge position where the number of zeros and ones are equal.
- Average Position calculates the positive edge time position as the average value between the time position provided by the First Edge and Last Edge methods.

Figure 5.11 presents a timing diagram of the debouncing operation with AP method. The AP method estimates the positive edge using the values obtained with the FE and LE methods. The FE_x and LE_x pulses are generated to detect the first and the last positive glitches of the U_x signals. Then, the estimated positive edge of the U_1 (t_{start}) and U_2 (t_{stop}) is obtained by calculating the average time between the arrival time of the corresponding FE and LE pulses.

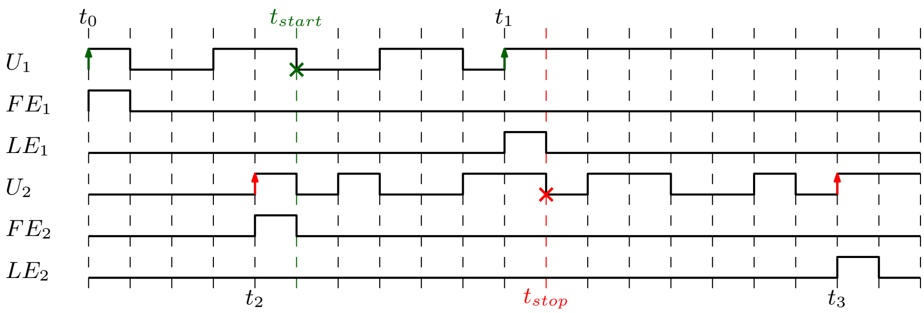


Figure 5.11: Timing diagram of the AP debouncing method describing the process to estimate the positive edge position of the U_1 and U_2 signals.

As expressed in Equation 5.23, the estimated phase difference between the U_x corresponds to the time difference between the t_{start} and t_{stop} signals.

$$\Delta t = t_{stop} - t_{start} = \frac{(t_3 + t_2)}{2} - \frac{(t_1 + t_0)}{2} \tag{5.23}$$

Finally, Equation 5.23 can be rewritten as presented in Equation 5.24 to facilitate the implementation of the algorithm in the FPGA.

$$\Delta t = \frac{(t_2 - t_0)}{2} + \frac{(t_3 - t_1)}{2} \tag{5.24}$$

Thereby, the AP method is implemented in the FPGA with two time counters, where the number of clock cycles between the FE_x and LE_x signals are counted separately and then subtracted.

Debouncing techniques comparison

The four debouncing techniques were tested to compare the resolution of the AP method. An OSUS circuit was implemented in the Readout FPGA containing four different sets of debouncer blocks. The result of the comparison is presented in Figure 5.12, where each histogram contains 500,000 measurements corresponding to the phase difference between a pair of 240 MHz clocks. The OSUS circuit was implemented with a factor M equal to 1 and the PLL was configured a factor N equal to 16384.

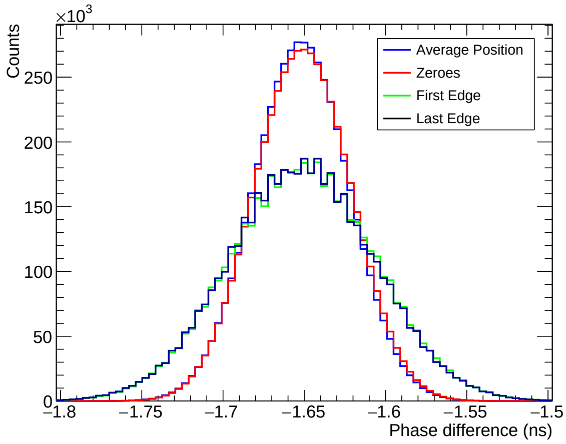


Figure 5.12: Comparison of the four debouncing methods measuring two 240 MHz clocks. The OSUS circuit was configured with $M = 1$ and the PLL with $N = 16384$.

Table 5.1 shows the time resolution corresponding to the four methods compared in Figure 5.12.

Debouncing technique	**Resolution$_{\mathbf{RMS}}$**
Average Position	29.12 ps
Zero Count	29.5 ps
First Edge	44.66 ps
Last Edge	44.57 ps

Table 5.1: Time resolution obtained with the AP, ZC, FE and LE methods.

As can be concluded from Figure 5.12 and Table 5.1, the AP and ZC methods provide a much better resolution than the FE and LE techniques, with an improvement of about 15 ps_{RMS}. Although the number of logic resources needed to implement the AP and ZC algorithms are very similar, the AP shows a slightly better time resolution than the ZC method. For this reason, the AP method was used in the TilePPr prototype to debounce the output signals coming from the OSUS samplers.

5.5 Implementation of the OSUS circuit

The design of the OSUS circuit permits the synchronization of the front-end electronics with the LHC clock and monitoring of the clock phase stability during the operation of the Demonstrator module.

As will be described in the next subsections a total of 17 OSUS circuits were implemented in the Readout FPGA. The u_s signal used for sampling is generated from a 240 MHz clock with an MMCM and a PLL circuits connected in series. Equation 5.25 shows the multipliers and dividers of the clocking resources which were selected to obtain a factor N with a value of 16384. Moreover, both clocking elements were connected without buffers through dedicated clock lines to reduce the additive jitter [91].

$$\begin{aligned} f_s = f_{in} \cdot \frac{M_{MMCM}}{D_{MMCM} \cdot O_{MMCM}} \cdot \frac{M_{PLL}}{D_{PLL} \cdot O_{PLL}} = 240 \text{ MHz} \cdot \frac{64}{1 \cdot 3.625} \cdot \frac{64}{10 \cdot 113} \\ = 240 \text{ MHz} \cdot \frac{16384}{16384 + 1} = 239.985 \text{ MHz} \end{aligned} \tag{5.25}$$

where M_{MMCM} and M_{PLL} correspond to the value of the multipliers, D_{MMCM} and D_{PLL} to the value of the input dividers, and O_{MMCM} and O_{PLL} to the value of the output dividers.

Table 5.2 describes the features of the implemented OSUS circuit with respect to the factor M for the selected u_s clock frequency and N.

f_{in} (MHz)	240 MHz	120 MHz	80 MHz	40 MHz
factor M	1	2	3	6
R_t	254.313 fs	508.626 fs	762.939 fs	1,525.878 fs
f_U	14.647 kHz	7.323 kHz	4.882 kHz	2.441 kHz
Counter Nbits	14	15	16	17

Table 5.2: Characteristics of the implemented OSUS circuit with respect to the different clock frequencies that can be measured with the current configuration. R_t represents the theoretical time resolution of the OSUS circuit.

Each pair of samplers corresponding to one OSUS circuit was implemented in the same SLICEL block. Slices SLICEL and SLICEM are the logic elements of the Xilinx Series 7 FPGAs. Each slice contains four Look-Up Tables, four Shift Register Logic blocks, that can be configured as FFs or latches, arithmetic carry logic and multiplexers to enlarge possible interconnections between the different blocks.

Figure 5.13 shows how the input signals u_x were connected to the FF A and B through the input AX and BX of a SLICEL block. Then, the AQ and BQ outputs transmit the sampled signals to the Phase Control unit where they will be decomposed into the U_x^k signals. The placement of rest of the blocks is not critical and they are placed in the nearby slices.

It is important to remark here that the clock skew of the u_s signal between the samplers is negligible since both samplers are placed in the same SLICEL. However, the different propagation delays from the origin of the u_x input signals and the samplers have to be measured and calibrated to avoid systematic phase errors in the measurements. The delay associated with the internal FPGA routing of the u_x signals was extracted using the Xilinx FPGA Editor software [93] and compensated at the software level.

5.5.1 Synchronization of the Demonstrator with the TTC system

The synchronization of the Demonstrator module with the TTC system is achieved through the TilePPr. As introduced in Chapter 4, the ADN2814 chip recovers a clock with a frequency 4 times the LHC clock frequency (160 MHz) which is converted by the CDCE62005 chip in a low jitter clock with a frequency 3 times the LHC clock (120 MHz). This low jitter clock will drive the transceivers and will be used to generate all the required clocks for the different firmware blocks in the Readout FPGA. Figure 5.14 depicts a block diagram showing all the blocks involved in the synchronization process and its interconnections.

However, the phase relationship between the LHC clock and the local LHC clock (LHC_{local}[1]) generated in the Readout FPGA is fixed but unknown. Furthermore, the phase between the two clocks could change every time the system is initialized due to the frequency conversion in the CDCE62005 chip and other latency uncertainties as the non-deterministic output delay of the CDCE62005 [94]. These latency variations could produce two different prob-

[1]This clock is referred as tx_frame_clk in Chapter 4.

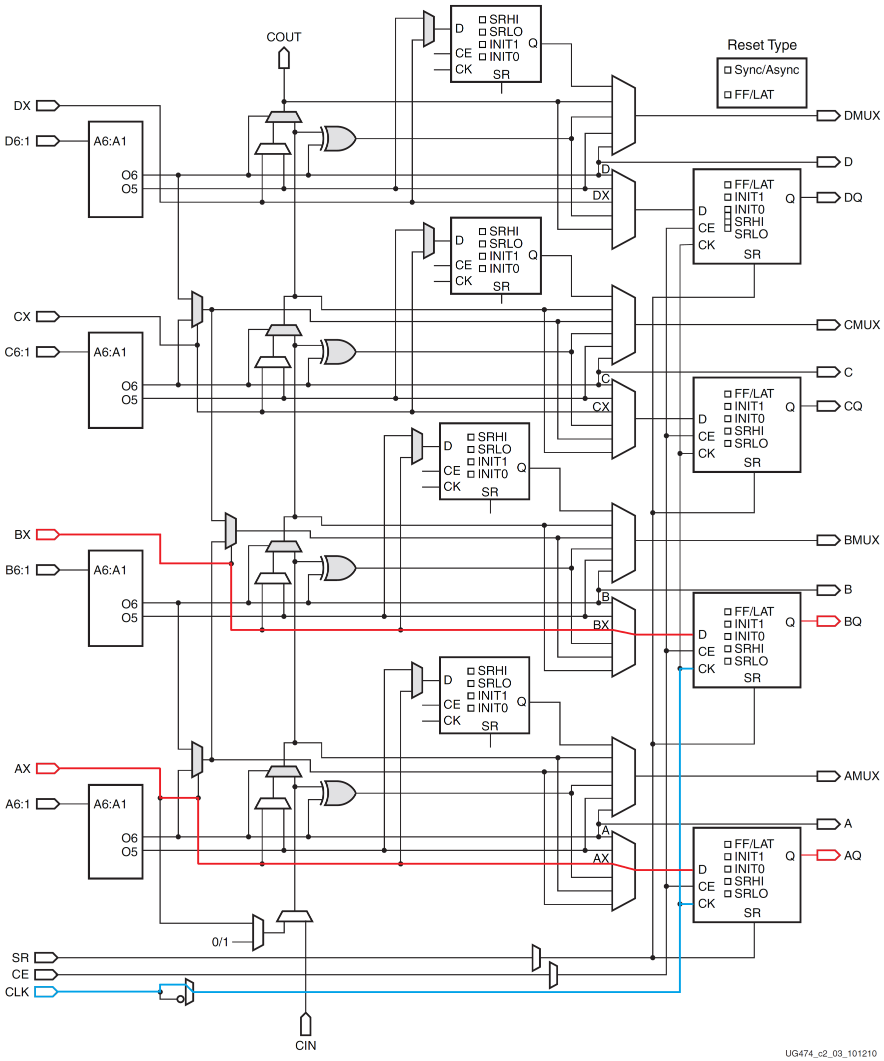


Figure 5.13: Block diagram of a SLICEL. The two clock signals (red) are connected to two registers in the same SLICEL block to minimize the skew delay of the sampling clock (blue). Figure extracted from [92].

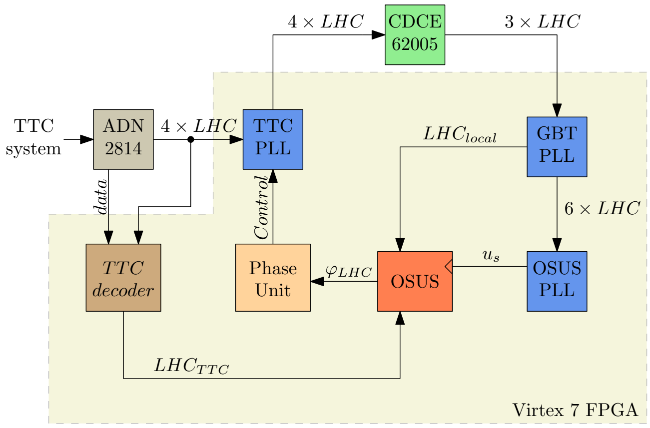


Figure 5.14: Block diagram of the synchronization block.

lems: the mis-synchronization of the front-end electronics with respect to the LHC clock, and errors during the transmission of received TTC commands due to CDC issues.

The method for the synchronization of the Demonstrator with the TTC system presented here combines the dynamic reconfiguration capabilities of the MMCMs with the phase measurements provided by the OSUS circuit.

First, the Slow Control FPGA configures the local oscillator (Si570) and the CDCE62005 chip to provide a local clock for the initialization of the transceivers. Once the TTC decoder block asserts the TTC locked signal, indicating that the LHC clock provided by the TTC system is present, the Slow Control FPGA configures the CDCE62005 chip to switch the input clock from the local to the recovered clock. In addition, the TTC decoder block generates a clock signal synchronized with the LHC clock (LHC_{TTC}) using logic resources for monitoring purposes.

The phase difference between the LHC_{TTC} and the LHC_{local} signals is obtained with the OSUS circuit. The phase measurements are transmitted to a computer using the IPbus protocol where a dedicated software calculates the number of steps of 11 ps needed to align both clocks. The computed number is passed to the Phase Unit which configures dynamically the TTC PLL to shift the phase of the recovered clock sent to the CDCE62005. This process is repeated until the averaged phase difference measured with the OSUS circuit is below 15 ps.

Figure 5.15 shows a histogram of the phase difference between the LHC_{local} and LHC_{TTC} extracted from the synchronization process between the Demonstrator and the TTC system after the calibration of the OSUS circuit. As can be observed, after synchronization of the clocks the OSUS circuit measures a phase difference between both clocks of ~3.7 ps.

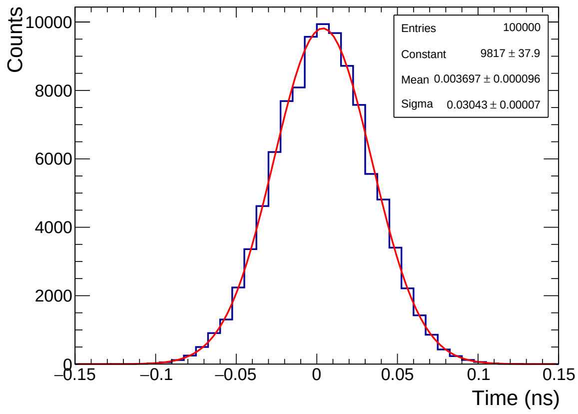


Figure 5.15: Histogram corresponding to 100,000 measurements corresponding the phase difference between the synchronized LHC_{local} and LHC_{TTC} signals.

In addition, the phase difference between both clock signals was measured with a Lecroy WavePro 760Zi oscilloscope to compare the results obtained with the OSUS circuit. Figure 5.16 shows the histogram obtained with the oscilloscope corresponding to the phase difference between the LHC_{local} and LHC_{TTC} signals.

The measurement shows a phase difference of 2.005 ns, which corresponds to the propagation delay difference from the LHC_{local} and LHC_{TTC} sources to the output pins connecting the TilePPr with the oscilloscope. The measured value agrees with the delay difference of 2.004 ns estimated with the Xilinx FPGA Editor software.

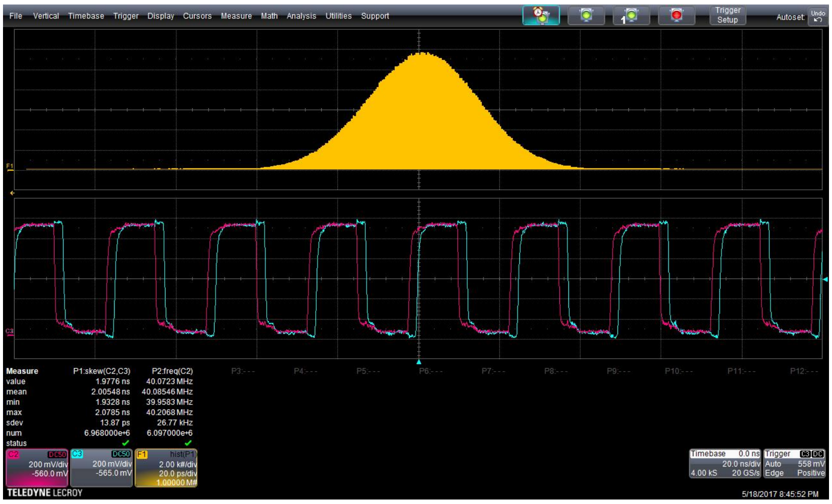


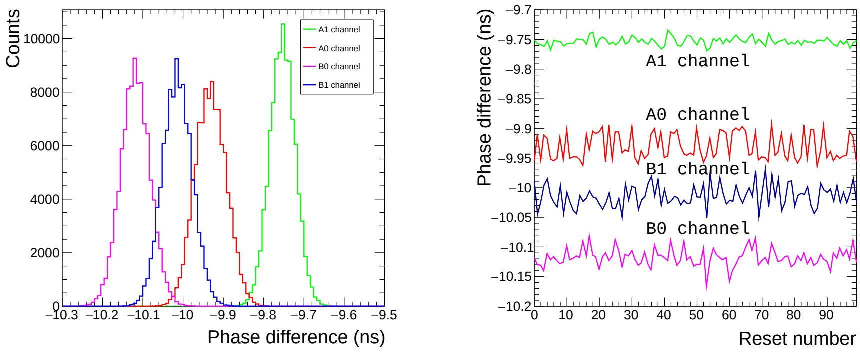
Figure 5.16: Histogram of the phase difference between the synchronized LHC_{local} and LHC_{TTC} obtained with a Lecroy WavePro 760Zi oscilloscope.

5.5.2 Studies on clock stability

The OSUS circuit was also used to study the stability of the LHC clock distributed through the GBT links in two different scenarios: after resetting the GBT links and long term operations.

Each GBT link is equipped with an OSUS circuit measuring the phase difference between the recovered clock from the front-end electronics LHC_{FE} and the LHC_{TTC} extracted from the legacy TTC system. The LHC_{FE} signal corresponds to the HG/LG bit of the GBT word (see Chapter 4) before being retimed by the BO-CDR circuits.

During the first test, the DaughterBoards were remotely reset 100 times from the TilePPr prototype. After every reset, 1,000 measurements of the phase difference between the LHC_{FE} and the LHC_{TTC} were acquired for the four links (A0, A1, B0 and B1) receiving data from the DaughterBoard. Figure 5.17 (a) shows a histogram containing all the measurements taken during the 100 resets for all the channels, and Figure 5.17 (b) presents the mean value of each set of measurements acquired during the overall test. As can be observed, the maximum delay variations between resets is below 100 ps. The channel-to-channel skew is produced by internal delays in the distribution of the reference clock to the transmitter part of the transceivers [39].

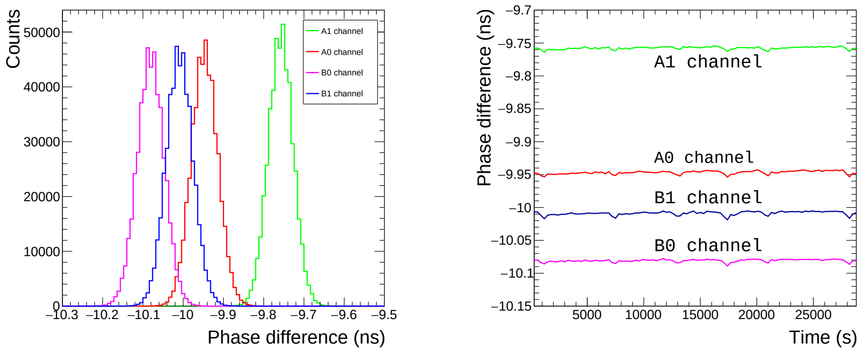


(a) Histogram of the phase difference between the LHC_{FE} and the LHC_{TTC} for the 4 links after resetting the DaughterBoards 100 times.

(b) Phase difference between LHC_{FE} and the LHC_{TTC} with respect to the reset count.

Figure 5.17: Phase difference variations between the LHC_{FE} and the LHC_{TTC} signals after 100 resets.

In the second test, the phase difference between the LHC_{FE} and the LHC_{TTC} clocks was measured 5,000 times every 5 minutes for a total period of 8 hours. The delay variations with respect to the time are presented in Figure 5.18. As expected, the phase difference between the clock signals was stable throughout the test showing small variations below 10 ps.



(a) Histogram corresponding to the phase measurement the LHC_{FE} of the 4 links and the LHC_{TTC} during a period of 8 hours.

(b) Phase difference variations between the LHC_{FE} of the 4 links and the LHC_{TTC} over the time.

Figure 5.18: Phase difference variations between the LHC_{FE} and the LHC_{TTC} during a period of 8 hours.

The results validate the capability of the TilePPr to provide a stable clock for the digitization of analog pulses. Both studies reflect that the expected phase variations between the transmitted and the received LHC clocks are below 100 ps. In any case, phase drifts are detected and corrected by the periodic monitoring of clock phases during the operation of the Demonstrator module.

Chapter 6

Testbeam setup and results

Three testbeam campaigns were conducted at the H8 beam line of the CERN SPS accelerator in the Prevessin area during 2015 and 2016. During 2017, two more testbeam periods will be conducted to continue with the evaluation of the upgraded readout electronics presented in Chapter 2. Usually, each testbeam period consists of 14 days of beam time to complete a set of measurements, where modules are tested using different energy beams and particles along η and in perpendicular positions with respect to the beam. This chapter includes a detailed description of the testbeam setup, facilities, trigger and readout architecture, as well as an introduction to the physics and calibration results obtained during the testbeam campaigns.

6.1 Introduction

The main motivations of the testbeam campaigns are to study the stability of the readout electronics and to validate the trigger and readout architectures envisaged for the Phase II upgrade. The performance of the three FEB options and back-end electronics for the HL-LHC was studied with data generated with electrons, pions and muons, permitting its full characterization in conditions close to real operation.

During the last two testbeam campaigns in 2016, the TilePPr prototype was installed in the H8 control room and it was used to read out and operate the Demonstrator module and to transfer selected data to the legacy RODs and FE-

LIX prototype. However, during the testbeam session in 2015 the TilePPr functionalities were implemented in a commercial Xilinx VC707 evaluation board since the TilePPr prototype was still under development.

6.2 Testbeam setup

The calorimeter setup was located in the H8 beam line of the CERN SPS North Area. The setup was composed of three TileCal modules placed on a scanning table capable of placing modules at any combination of angle and position with respect to the incident beam. Two modules, one Extended Barrel and one Long Barrel, were instrumented with the legacy readout electronics described in Chapter 1. These modules included PMT blocks with 3-in-1 cards, Digitizer boards and Interface boards, for the communication with the back-end electronics. The legacy modules played a crucial role during the testbeams permitting the comparison between the legacy and the new readout electronics.

Figure 6.1 presents the configuration and position of the modules during the testbeam periods, and Figure 6.2 a picture of the testbeam modules on the scanning table.

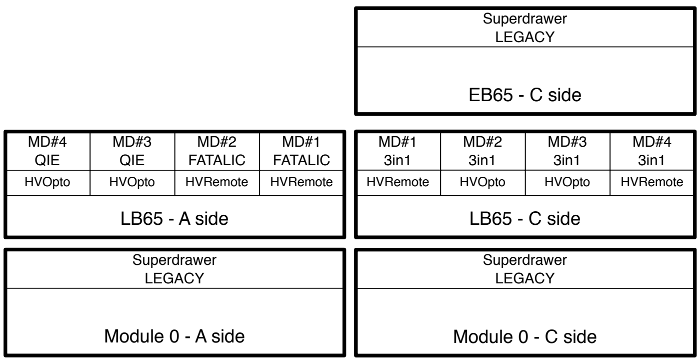


Figure 6.1: Configuration of modules and electronics during the October 2016 testbeam period.

One additional Long Barrel module was instrumented with the upgraded electronics: the FATALIC/QIE module and the Demonstrator module. The upgraded modules included four minidrawers connected to a cooling system which controlled the internal temperature of the modules. Each minidrawer

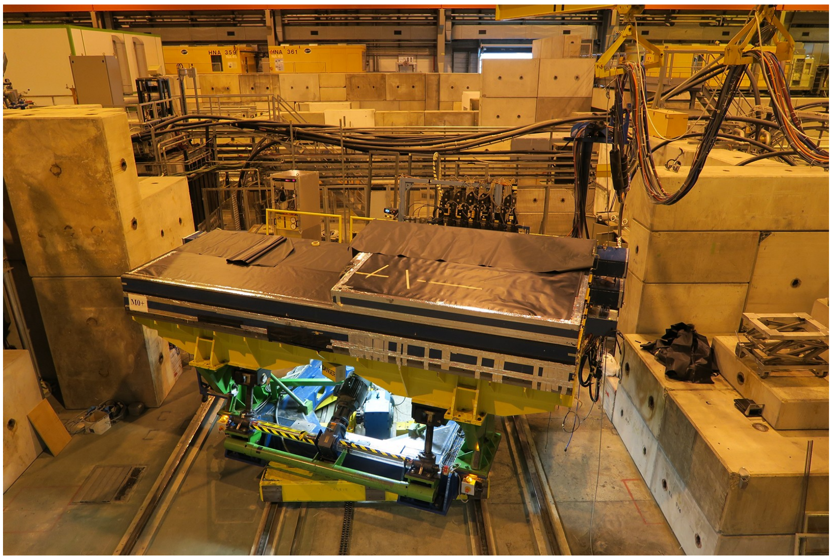


Figure 6.2: Picture of the testbeam module on the table.

contained one DaughterBoard, one MainBoard and 12 PMT blocks with the upgraded FEBs.

The QIE/FATALIC module was instrumented with both QIE and FATALIC technologies. Two minidrawers were populated with PMT blocks with QIE FEBs and two minidrawers with PMT blocks with FATALIC FEBs. Each FEB option was connected to the corresponding MainBoard version which is specific for each FEB option.

The Demonstrator module was equipped with 45 PMTs with 3-in-1 cards, a 3-in-1 MainBoard and a DaughterBoard.

Related to the services, both HVPS options were installed in the upgraded modules to provide high voltage to the PMTs. The two FATALIC minidrawers were powered with the remote HV system while the QIE minidrawers were populated with the HV internal system. The Demonstrator module included a combination of both options: the PMT blocks located in the outer minidrawers were fed with the HV remote system and the PMTs in the middle minidrawers were powered with the HV internal system. Each upgraded module received the low voltage power from a fLVPS attached to the extreme of the module and controlled from the legacy DCS software via CANBus.

The back-end electronics combined the legacy and the new readout electronics. It included a reduced version of the legacy back-end electronics composed of one ROD, one SBC and one TBM. The upgraded modules transmitted the data to two TilePPrs integrated within the legacy TDAQ software through the TTC and ROD interfaces.

Finally, a TTC system was also present in the testbeam setup composed of a LTP, a TTCvi and a TTCex. The TTC system was used to configure the upgraded and legacy electronics using the TDAQ software and also to provide the clock for the readout electronics.

6.2.1 Beam elements

A variety of detectors were installed in the beam line to monitor the quality, position and particle composition of the beam [95]. Figure 6.3 depicts a diagram of the beam elements installed in the testbeam line.

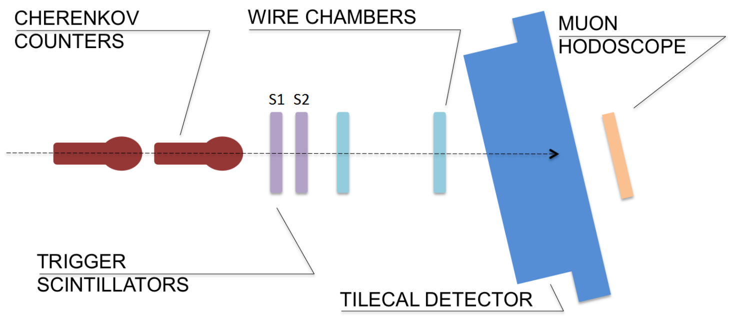
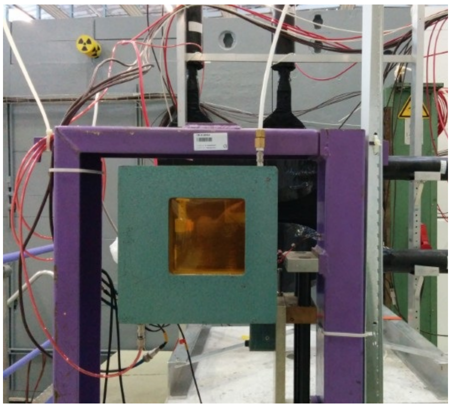


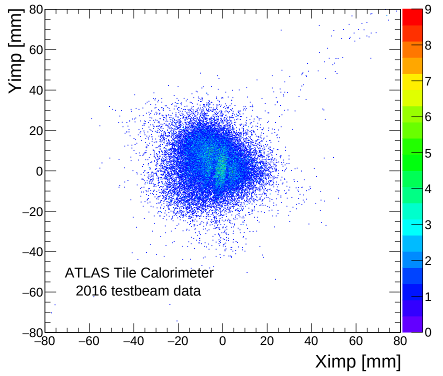
Figure 6.3: Sketch of the beam elements in the testbeam setup.

Two beam chambers were used to measure the beam position with a resolution of 0.2 mm. The beam chambers used at the testbeam are Delay Wire Chambers (DWC) [96], developed at CERN. The DWC is formed by two sandwich parts, each composed of two cathode planes surrounding a central anode wire-plane. The sandwich parts are placed orthogonally each other giving a two dimensional position measurement. Figure 6.4 shows a picture of an instrumented DWC.

Since the beam is not composed of a single type of particle, a Muon Hodoscope (MH) and two Cherenkov Counters (CCs) were placed to help during



(a) Delay Wire Chamber.



(b) Beam position extracted from the beam chambers data.

Figure 6.4: Picture of one of the beam chambers used for the testbeam setup and the beam position data.

the offline data analysis adding information for the particle identification. The MH, also called Muon wall, is a movable detector made of 12 scintillators placed behind the Tile modules. It is primarily used in offline analysis to suppress the low energy tail of the pions in high energy hadrons runs.

The CCs were placed in the beam line to improve the particle identification separating pions and electrons at energies below 50 GeV. During the two first testbeam campaigns in September 2015 and June 2016 two CCs were installed in the beam line. One CC was configured to report interactions with kaons, pions and electrons, but not protons, while the second one only reported interactions with pions and electrons. During the testbeam of September 2016 a third CC was installed and configured for identification of electrons.

Two scintillators S1 and S2 (Figure 6.3) were installed in the beam line as part of the beam trigger system. The scintillator signals were transmitted to the beam trigger system in the control room via coaxial cables. Since the scintillator cable lengths were different, signals were time-equalized using delay boxes before reaching the trigger system.

The beam trigger logic was implemented in a NIM crate using timer counters, discriminators and Fan-in/Fan-out modules. The beam trigger generates a Master trigger signal when a beam particle produces a signal on both scintillators. Then, the Master signal is transmitted to a second NIM crate initiating the TDC measurement of the beam chamber signals and reading out the ADCs used for the digitization of the scintillator signals.

In addition to the generation of the Master trigger, the trigger logic propagated the L1A signal to the LTP in the TTC crate, unless the busy signal was asserted indicating that the readout path was not available. Then, the LTP transmitted the L1A signal to the TilePPr, RODs and front-end electronics via the TTCvi and TTCex systems.

6.3 Clock distribution

The TTC system distributed the LHC clock to the legacy modules, RODs and to the TilePPr prototypes through dedicated optical fibers. As described in Chapter 1, the TTCrx ASIC located in the Motherboards of the legacy front-end electronics recovers and fans out the LHC clock to the ADCs. In the back-end electronics, the RODs also receive the LHC clock and TTC data for event synchronization.

The clocking architecture employed for transmitting the LHC clock to the upgraded modules is close to the proposed one for the Phase II Upgrade already described in Chapter 5. The difference between the clocking distribution in the testbeam setup and the proposed one for the Phase II is that the LHC clock source is the legacy TTC system and not the FELIX system.

In the TilePPr, dedicated circuitry was employed to recover the LHC clock and a jitter cleaner was used to reduce the jitter before the clock is passed to the FPGA transceivers. The LHC clock was then distributed to the front-end electronics embedded with the downlink GBT data.

In the DaughterBoard, the GBTx recovered and routed to the FPGA transceivers a clock with four times the LHC clock frequency. Finally, the recovered LHC clock was extracted from the transceiver CDR clock and transmitted to the ADCs as sampling clock. In addition, the DaughterBoard FPGAs also implemented the uplink communication at 9.6 Gbps using the recovered clock and unifying the uplink and downlink clock domains.

Moreover, during the testbeam operation the TilePPr received commands to configure the front-end electronics either through the IPbus registers or the TTC fiber. In the latter scenario, the TilePPr converted the legacy TTC commands into Phase II commands.

6.4 Data acquisition

The TilePPr prototype was installed in the control room and was the core of the back-end electronics during the testbeam campaigns of June 2016 and September 2016. The TilePPr prototype was fully integrated into the TDAQ architecture. It received the clock, commands and triggers from the legacy TTC system and also transmited the triggered data to the RODs. A block diagram describing the data flow and data acquisition architecture employed during the testbeam is shown in Figure 6.5.

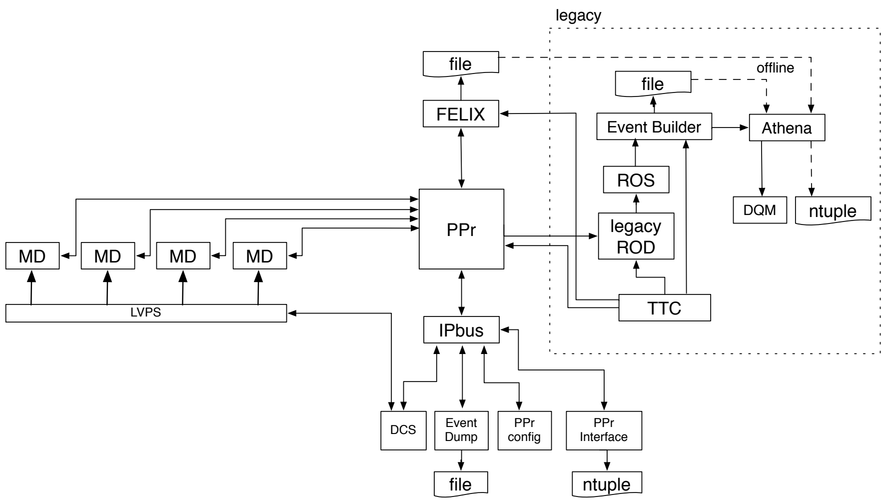


Figure 6.5: Complete data acquisition system and data flow for the testbeam setup.

The Demonstrator module transmitted to the TilePPr high and low gain samples every 25 ns through 16 GBT links (4 Tile GBT links per minidrawer). The TilePPr prototype extracted the samples from the GBT data and stamped them with the corresponding BCID before its storage in the circular pipelines. When a L1A was received, the TilePPr copied the data from the pipelines and created an event packet that was transmitted to the next level in the DAQ architecture.

The TilePPr prototype featured three different readout paths already introduced in Chapter 4: FELIX system, legacy ROD and Ethernet readout through IPbus. During the testbeam campaigns, the IPbus readout path was primarily used for the configuration of the TilePPr and front-end electronics, daily calibration runs, monitoring and readout of the integrator ADCs during the Cesium calibration scans.

In the case of the FELIX readout path, 16 samples with the corresponding BCID were formatted and sent to a FELIX prototype system through a Standard GBT link. The FELIX prototype used during the testbeams was a reduced custom version of the FELIX system capable of receiving GBT data at 4.8 Gbps and storing the received data in internal buffers. This system was implemented using a Xilinx KC705 evaluation board connected through PCIe to a computer. After the reception of a complete event in the FELIX prototype system, the binary data was extracted from the KC705 memories through the PCIe interface and stored in the computer for later offline analysis.

The legacy readout path is important because it allows the integration of the Demonstrator module into the legacy TDAQ architecture after its installation into the ATLAS detector. The TilePPr prototype emulated a legacy module by sending event packets to the RODs through a G-Link interface running at 800 Mbps. After the reception of a L1A, the TilePPr retrieved the data from the circular pipelines and packed the data into the legacy format for transmission to the RODs.

The PUs in the RODs used the Optimal Filtering 2 algorithm (OF2) [97] to reconstruct the amplitude and time of the shaped PMT signals using linear combinations of the digital samples with a set of weights.

Equations 6.1 and 6.2 represent the magnitudes reconstructed by OF2 algorithm.

$$A = \sum_{i=1}^{N} a_i S_i \tag{6.1}$$

$$\tau = \frac{1}{A} \sum_{i=1}^{N} b_i S_i \tag{6.2}$$

where a_i and b_i are OF2 weights, S_i are the digital samples, N is the number of digital samples (7 is the default number), A is the amplitude of the shaped signal in ADC counts, τ is the phase of the pulse peak with respect to the expected sampling time used in the calculation of the weights.

The OF2 algorithm also provides an estimation of the goodness of the reconstruction, called Quality Factor (QF) and expressed in Equation 6.3.

$$QF = \sqrt{\sum_{i=1}^{N}(S_i - (Ag_i + A\tau g_i' + p))^2} \tag{6.3}$$

where g_i and g_i' are the normalized amplitudes of the pulse shape function for the i_{th} sample and its derivative, and p is the pedestal which is usually estimated as the average of the first and last samples or, just as the value of the first sample [98].

Figure 6.6 shows a sketch of a reconstructed magnitudes superposed with the samples.

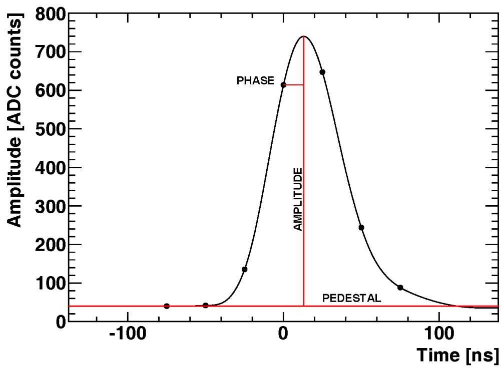


Figure 6.6: Picture of a typical pulse shape showing the 7 samples and the reconstructed pulse shape with the Optimal Filtering algorithm.

The Read Out System (ROS) received the reconstructed energy and time and the digital samples from the RODs and provided the data fragments to the Event Builder (EB). The EB reconstructed the energy and time per TileCal cell using the Athena software [99] of the ATLAS software framework and stored it in local disks together with the event trigger information provided by the TilePPr.

During the data taking, the Data Quality Monitoring application (DQM) accessed the stored events and displayed them in a Graphical User Interface

(GUI) to verify that the recorded data was useful. In addition, the DQM displays information regarding the beam line elements helping in the identification of problems during the data taking. Figure 6.7 shows a screenshot of the DQM used in the testbeam setup.

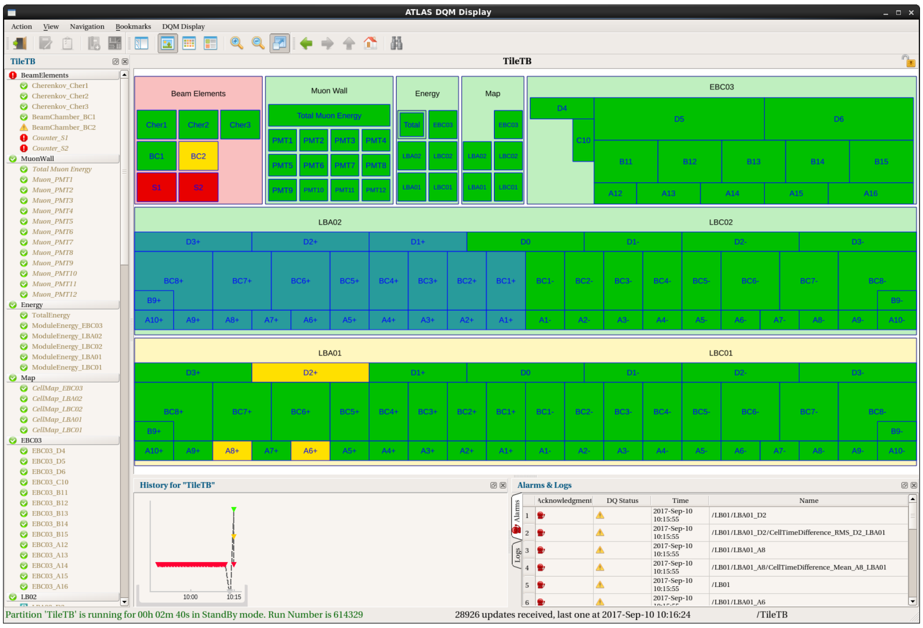


Figure 6.7: Screenshot of the DQM panel.

6.5 Calibration systems

The tests of the calibration systems are fundamental to verify the performance of the readout electronics before the data taking and to obtain calibration data to determine the electromagnetic energy scale and stability of the system. During the testbeam periods, daily pedestal and CIS runs were taken prior to the physics runs. Cesium scans to obtain the response of the detector were taken twice per testbeam period.

6.5.1 Pedestal and linearity runs

The first test performed during the calibration runs are the linearity tests. The linearity tests confirm that the front-end electronics receives correctly the configuration commands and the ADCs data is correctly deserialized.

In the linearity tests the DACs connected to the ADC inputs are configured to shift the pedestal value from 0 to the maximum ADC range in programmable steps. Then, pedestal samples are read out through the IPbus registers to verify the pedestal configuration. Any significant non-linearity of the results would indicate that commands did not reached the front-end electronics, the analog electronics is malfunctioning, or a problem with the deserialization in the DaughterBoard FPGAs. Figure 6.8 shows the linearity test results corresponding to the ADCs of one MainBoard section (3 channels).

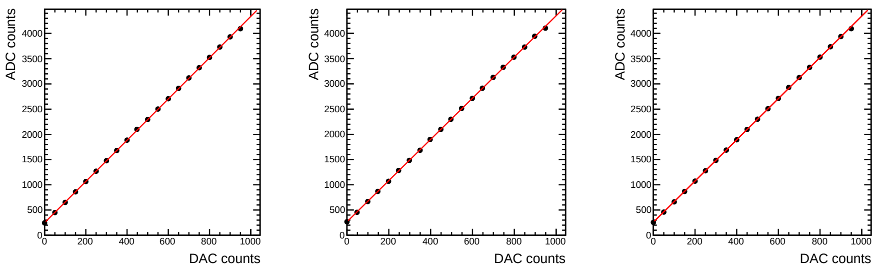


Figure 6.8: Result of the linearity test. The red line represents the fit result of a first-order polynomial function.

The pedestal runs were used to check that the digital path from the ADCs of the MainBoard to the TilePPr was working correctly. This test validates the digital path in both directions since the MainBoard is configured to set the DACs that move the baseline at the ADCs input and the samples are read out from the TilePPr through IPbus or the RODs. Normally, around 100,000 samples per ADC channel and gain were taken daily. When the readout path was the ROD, each measurement includes 7 samples while the IPbus read out 32 samples per measurement. Figure 6.9 shows the obtained histogram for a single channel with 100,000 samples, where a reduced noise with a value of 2.8 ADC counts RMS can be observed. This value is similar to the RMS noise measured in the current system [27].

In addition, this test permits detection of increased noise in the ADC channels or problems with the deserialization in DaughterBoard that would be seen as non-Gaussian distribution of the pedestal values.

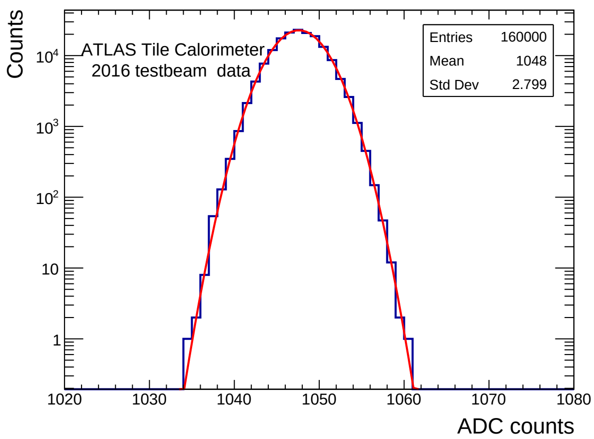


Figure 6.9: Result of a pedestal run taken with the TilePPr prototype through the IPbus readout path.

6.5.2 Charge Injection System

The Charge Injection System included in the 3-in-1 cards is used to obtain the gain factor of each individual ADC channel by injecting a known charge and measuring the ADC response. CIS runs were taken in two different operation modes: local and remote. In the local mode, a set of C++ and python scripts were used to configure the front-end electronics through the TilePPr. The 3-in-1 card configuration for the switches, charge and BCID execution were transmitted to the TilePPr through the IPbus interface, which encoded and transmitted the commands to the front-end electronics through the optical links.

In the remote mode, the front-end configuration was controlled by the TDAQ software which sent the configuration through the TTC system. The TilePPr decoded the legacy TTC commands, converted them into Phase II format and transmitted them to the front-end through the GBT links.

The two types of CIS tests were performed during the testbeam to obtain the gain factor of the 3-in-1 cards to convert amplitudes in ADC counts to pC.

CIS linearity

During the CIS linearity test a series of CIS runs are generated increasing the charge of the capacitors in discrete configurable steps. The CIS linearity test is done for high and low gains covering the full ADC range. The reconstructed pulses include a bipolar component introduced by the internal capacitance of the charge injector switches. This bipolar component can be measured configuring the DAC to provide 0 V, and then subtracted from the reconstructed pulses.

CIS stability

The CIS stability tests consist of repetitive CIS runs with the same charge and gain to track any variation of the reconstructed charge with time. During the CIS stability tests the TilePPr configured the front-end electronics to charge and discharge the selected CIS capacitor at a predefined BCID. It also stored the CIS pulses in the pipelines before transmitting them to a computer through the IPbus interface or through the legacy TDAQ infrastructure.

Figure 6.10 shows the result of a CIS linearity test for a single 3-in-1 card. The measured charge is presented as a function of the injected charge for a low gain channel showing good linearity. The bottom part of the figure indicates the difference between the injected and the reconstructed charge. These residuals are used to study the stability of the circuits with time.

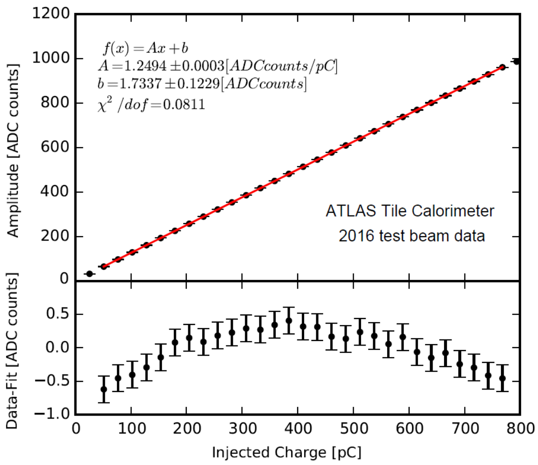


Figure 6.10: Results of a CIS linearity test of a low gain channel and its residuals.

6.5.3 Cesium scans

The Cesium system was designed to measure the PMT gain and optical response of the calorimeter cells. These measurements permit to obtain the correct high voltage settings for each channel to equalize the response of the cells. An insufficient strength of signal could also indicate broken fibers or a poor coupling between the fiber bundle and the PMT block.

An hydraulic system moves a ^{137}Cs γ source through a water-filled pipe that crosses all the scintillator cells in the module. The ^{137}Cs γ source is enclosed in a small metal capsule. The current from PMTs is integrated and then digitized by a 16-bit ADC. As explained earlier in Chapter 4, the integrator firmware block in the DaughterBoard reads out these ADCs and transmits the integrator samples to the TilePPr prototype.

The integrator samples can be read out at a configurable period in units of orbits (89 μs). Normally the integrator samples are read out at a rate between 90 Hz and 150 Hz to follow the movement of the ^{137}Cs γ source circulating through the cells. Figure 6.11 shows the result of a Cesium scan for the cell BC4. The maxima of the optical response correspond to the source crossing the scintillating tiles while the minimums correspond to the source crossing the absorber material.

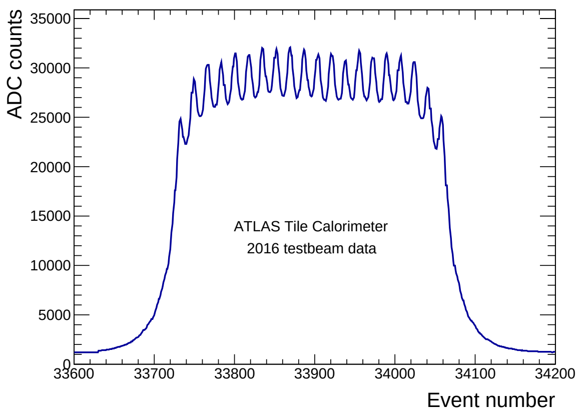


Figure 6.11: Response of the BC6 cells of the Demonstrator module during a Cesium scan. Each peak corresponds to the response of each individual scintillator tile when the Cesium source passes through the module.

6.6 Demonstrator physics program

The physics program for the testbeam included the evaluation of the Demonstrator and legacy modules with particle beams pointing at different cell positions and angles. One of the goals of the testbeam program is to characterize the response of the detector with the new readout electronics using different types of particle beams with known energy. The performance of the upgraded electronics is then compared with data obtained from the legacy modules also installed in the testbeam.

The measurement of the cell response to electron beams determines the average charge to energy conversion factor called electromagnetic scale (EM) constant. The measurement of electrons also evaluates the detector characteristics such as linearity, uniformity and energy resolution. In addition, the measurement of muon energy can be used for the calculation of the EM constant.

Other interesting measurements involve hadron beams where the hadron shower energies are measured. These tests characterize the pion response as a function of the energy and permits the evaluation of new energy reconstruction methods.

The SPS beam is not pure, it is a mixture of pions, electrons and muons. After the data is reconstructed, an offline analysis is needed to separate and identify single event-particles that will be the basis for the different studies and calculation of the EM constant

6.6.1 Data quality

During the data taking and prior to the offline data analysis for particle identification, the data collected from each PMT is analyzed for integrity. The maximum sample is positioned in the fourth position of the seven samples transmitted to the RODs in order to minimize the error deviation during the energy reconstruction. However, as indicated in Figure 6.12, the maximum sample could not always be contained in the fourth sample because the different time of arrival of particles depending on the beam interaction point. Also the timing precision of the testbeam trigger system when generating the L1A signals could produce a misplacement of the maximum sample.

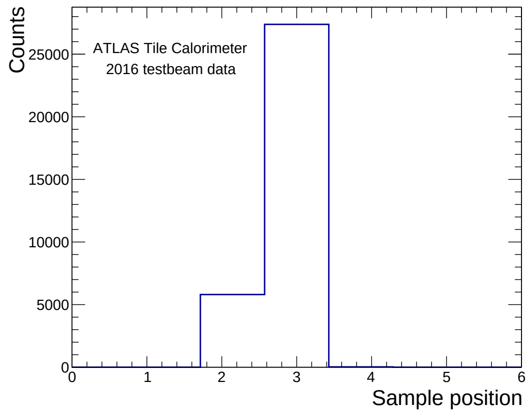


Figure 6.12: Histogram of the maximum sample position corresponding to PMT 42 during a run with 50 GeV electron beam.

A second data quality study includes the comparison of the energy collected by the two PMTs reading a cell. The correlation between the energy of the PMTs reading out a cell gives an insight of the PMT gain relation where the correlation coefficient is expected to be one or close to, if the beam is targeting the cell center. An energy response with a correlation coefficient different from one would indicate the malfunctioning of one PMTs or the application of non-optimal HV values. Figure 6.13 shows the correlation between the energy of the two PMTs reading the BC8 cell of the Demonstrator module in a run with 50 GeV electron beam.

Finally, the correlation between the reconstructed time of two pulse signals also provides information about the data quality. The reconstructed time of a pulse signal refers to the time difference between the reconstructed pulse peak and the sampling clock edge. However, since the testbeam trigger system is not synchronized with the beam, the reconstructed a peak varies uniformly in time between ± 25 ns. Figure 6.14 shows the correlation between the reconstructed time of two PMTs connected to cell BC6 (a) and the reconstructed time for only one PMT (b).

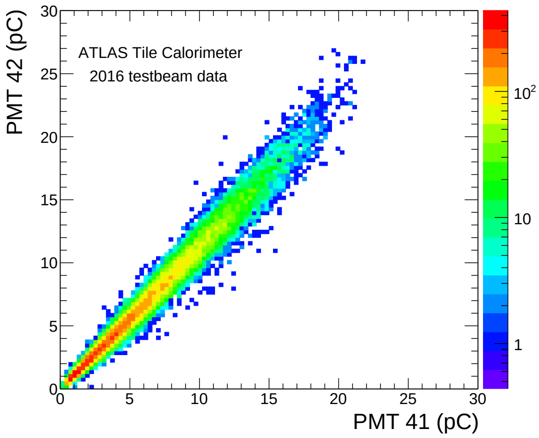
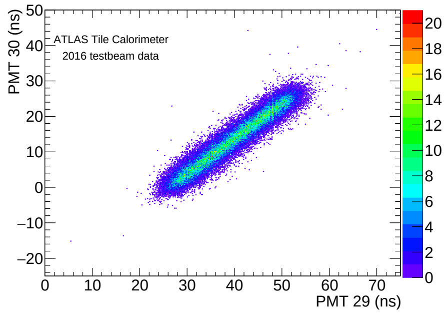
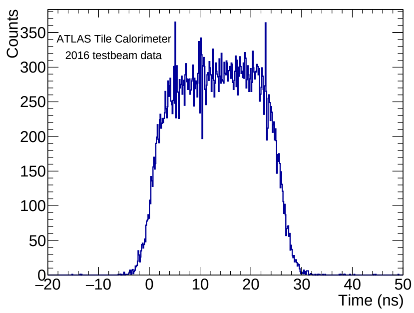


Figure 6.13: PMT energy correlation corresponding to cell BC8 during a run with 50 GeV electron beam. As can be observed, the correlation coefficient corresponds to a value close to one indicating a good equalization of the PMT gains.



(a) Correlation between the reconstructed time for PMTs 29 and 30 reading the BC6 cell. The timing correlation coefficient has a value close to one. The displacement of the maximum peak from the fourth sample produces an offset of 12.5 ns in the axis y and 40 ns in axis x.



(b) Reconstructed time for PMT 30. The phase difference between the peak pulse and the expected arrival takes random values in a 50 ns range centered in 12.5 ns.

Figure 6.14: Timing plots for BC6 cell taken during a run with 180 GeV muon beam.

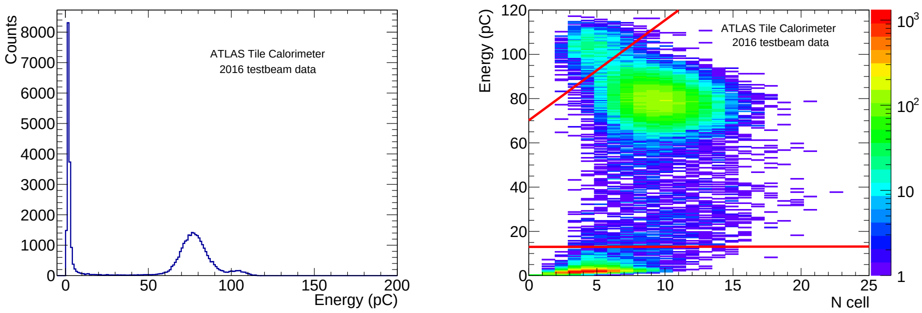
6.6.2 Offline data analysis

Different selections are applied to the reconstructed event data in order to select single-particle events and to perform the different studies for the detector characterization. The first selection requirement is implemented with the information collected with the beam elements during the run. The data from the beam chambers are used to reject events containing particles with tracks out of the beam axis or not parallel to it, since in this case the energy could not be deposited at the expected location in the module. In addition, selections are applied using the scintillator counters to remove events with particles generating undesired showers in the modules.

After the first selections, higher level methods are applied to effectively isolate specific types of particles for the different studies. For example, Figure 6.15 (a) shows the energy spectrum measured in the Demonstrator module with a 100 GeV electron beam where the pions and muons are clearly separated. Muons are mixed with pedestal and noise in the low energy side of the plot, while hadrons and electrons stay at higher energies.

The muon contamination can be easily removed for energies below 10 GeV by requiring the measured cell energy to be higher than 5 GeV. However, the pion-electron separation requires more sophisticated selections since electron beams are usually contaminated with a comparable population of hadrons and electrons. Most methods for electron-pion separation exploit the difference between electromagnetic and hadronic shower profiles. The electromagnetic showers produce a higher energy density in the impact region with respect to the hadronic showers, since the energy is deposited in a more concentrated region.

A method to separate pions and electrons, called Hot Cells [100], uses the measured energy of a single-particle event versus the number of cells that contains signal above the cell noise is also used. Figure 6.15 (b) shows the reconstructed energy of a run with 100 GeV electron beam versus the number of cells (N_{cells}) over an energy threshold of 0.05 pC [101]. For this analysis, the cells of the Demonstrator and the bottom legacy module are included for the calculation of the energy. The cluster on the top left side corresponds to electrons with higher energy which are concentrated in a lower cell count, the pions are at the center and the muons in the bottom part of the plot.



(a) Spectrum of the energy measured with the Demonstrator module during a run with 100 GeV electron beam.

(b) Event energy versus the number of cells over the threshold for a run with 100 GeV electron beam.

Figure 6.15: Energy spectrum of a run with 100 GeV electron beam and the representation of the energy versus the number of Hot Cells.

For electron beams with energies below 20 GeV the pion-electron separation can be improved by combining the data provided by the Cherenkov chambers with the Average Density (AvD) [100] expressed in Equation 6.4. The AvD is calculated as the sum of cell energies densities over the total number of cells with signal above a threshold.

$$AvD = \frac{1}{N_{cell}} \sum_{i=1}^{N_{cell}} = \frac{E_i}{V_i} \tag{6.4}$$

where E_i represents the deposited energy in cell i, V_i is the corresponding cell volume and N_{cell} is the number of cells with deposited cell energy greater than 0.06 pC.

Figure 6.16 shows a scatter plot of the second Cherenkov counter signal versus the AvD in the module for a 20 GeV run at $\eta = -0.25$. Electrons are separated in the right side where the AvD is higher in two main groups corresponding to the N_{cell} factor from Equation 6.4.

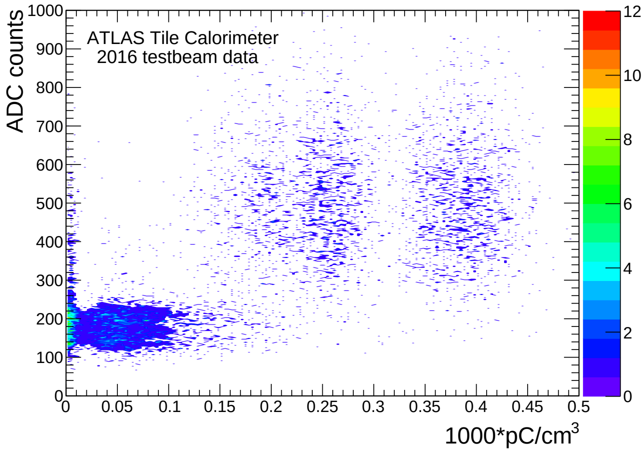


Figure 6.16: Scatter plot of the Cherenkov counter versus the AvD in the module for a run with 20 GeV electron beam. Pions are confined in the lower left quadrant and electrons in the right. The energy density for electrons is separated into two main regions corresponding to two or three cells above threshold.

These selection requirements allow identification of the different types of particles. As introduced before, the EM scale constant of the Tile Calorimeter cells is determined by measuring the energy of the single-event electrons. Figure 6.17 shows the relation between the electrons energy and the beam energy in a run with 100 GeV electron beam after applying a cut based on the AvD method. The EM calibration constant obtained is 1.031 pC/GeV with a σ of 0.045 pC/GeV, being close to the expected 1.05 pC/GeV already calculated in previous testbeams [101].

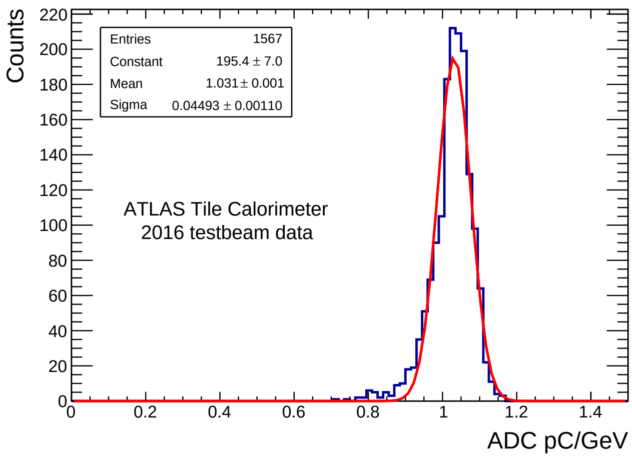


Figure 6.17: Energy in pC of the cell A8 normalized to the beam energy of 100 GeV electrons at 20 degrees after isolating the electrons.

The study of the muon signals permits the evaluation of the electronics performance since the TileCal response to muon are close to the pedestal values. Muons are isolated from the electronic noise applying energy cuts on all the cells that the beam crosses except in the cell under study. Figure 6.18 shows an example of muon signal isolation for a run with 180 GeV muon beam at $\theta = 0.15$. The pedestal shown in the plot corresponds to the reconstructed signal in cell D1 for a run with no beam on the Demonstrator module.

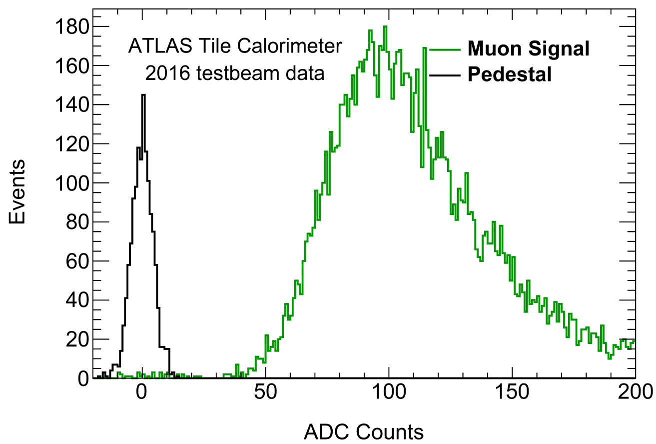


Figure 6.18: Isolated muon signal from the pedestal in cell D1 for a run with 180 GeV muon beam at 20 degrees.

Chapter 7

Conclusions

This PhD dissertation is focused on the design, production and integration tests of the first prototype of the TilePPr module for the ATLAS Tile Calorimeter in the HL-LHC.

Before the complete replacement of the readout electronics for the HL-LHC, the Demonstrator project aims to evaluate and qualify the upgraded electronics readout system with the installation of a Demonstrator module into the ATLAS experiment. The TilePPr prototype includes all the components required to read out and operate the Demonstrator module, implementing the trigger architecture envisaged for the HL-LHC, as well as, keeping backward compatibility with the current DAQ system.

A detailed description of the design and validation of the TilePPr prototype has been presented. Extensive signal integrity studies were performed to validate the PCB layout, where special attention was paid to the impedance discontinuities along the high-speed traces, that cause degradation of the signal integrity, such as the DC-blocking capacitors or the differential vias.

BER tests and eye diagrams were measured with a sampling oscilloscope as part of the validation tests of the prototype. The results presented in Chapter 4 show good performance of the prototype with a BER better than $5 \cdot 10^{-17}$ for a Confidence Level of 95%, as well as, low jitter values in the optical link signals with a $T_J(10^{-18})$ of 49.5 ps with a σ of 2.5 ps at 4.8 Gbps and 57 ps with a σ of 2.3 ps at 9.6 Gbps.

The limited number of clocking resources in the Readout FPGA forced a major modification of the GBT-FPGA IP core, where the MMCM of the GBT receivers was replaced by a BO-CDR implemented in logic. This modification permitted the implementation of a high number of GBT links in FPGAs. Moreover, the TileCal links required the modification of the IP core, where the data rate was increased from 4.8 Gbps to 9.6 Gbps in the uplink by tuning the configuration of the embedded transceivers and clocking resources. A special effort was made during the design of the GBT links and all the firmware blocks implemented in logic handling the readout samples, such as the data packers or deserialization blocks, to provide a fixed and deterministic latency.

The integration of the TilePPr prototype with the Demonstrator module was covered in detail, describing all the different firmware blocks implemented in the front-end and back-end electronics required for the operation of Demonstrator module.

Another important contribution is the implementation of a phase monitoring tool, called OSUS, which synchronizes the Demonstrator module with the LHC clock distributed by the TTC system and monitors the stability of the clock transmitted to the front-end electronics with a precision of about 30 $\mathrm{ps_{RMS}}$. Moreover, the OSUS circuit was used to study the latency variations of the GBT links produced after the reconfiguration of the front-end electronics. As it has been covered in this thesis, the glitches generated during the sampling of the clocks result in degradation of the system resolution. Different debouncing techniques were studied to estimate the time position of the positive edge. The studies allowed to improve the time resolution by about 15 $\mathrm{ps_{RMS}}$ when using the Average Position method instead the First Edge method.

Finally, the TilePPr prototype was integrated with the rest of the readout electronics during three testbeam campaigns and served as the main element of the back-end electronics system. Following the TDAQ architecture for the HL-LHC, the TilePPr prototype distributed the LHC clock and configuration commands to the front-end electronics through optical fibers and read out the digitized samples at the LHC frequency. Data was stored in pipeline memories up to the reception of L1A when the selected data was formatted and transmitted to the ROD and FELIX systems. Chapter 6 includes a detailed description of the testbeam setup, facilities, trigger and data acquisition architecture, accompanied by the physics analysis performed with the data collected from the testbeam campaigns. These important tests compared the performance of the legacy and upgraded readout electronics systems.

The future work derived from the TilePPr prototype includes the design of the TilePPr module for the HL-LHC, which will be based on the TilePPr prototype presented here. The final design will be capable to operate up to 8 complete modules and will be composed of an ATCA carrier with four AMC slots which will host the CPMs. The experience gained on high-speed data transmission techniques applied to the TilePPr prototype will be used for the future TilePPr module. In addition, many of the firmware pieces described in this document, such as the OSUS circuit or the Tile GBT-FPGA IP core, will be used in the final version of the TilePPr module.

Capítulo 8

Resumen

Esta tesis se desarrolla dentro del marco del proyecto *Tile Calorimeter* (TileCal) *Demonstrator*. Este proyecto tiene como objetivo la evaluación y cualificación de la electrónica de adquisición del detector TileCal para el *High Luminosity Large Hadron Collider* (HL-LHC). Los planes del proyecto *Demonstrator* incluyen la instalación de un módulo prototipo con los nuevos desarrollos electrónicos dentro del experimento *A Toroidal LHC ApparatuS* (ATLAS). Además, el módulo *Demonstrator* será testeado con haces de partículas en diferentes periodos de *testbeam* con el objetivo de estudiar el rendimiento de los prototipos.

En esta tesis se presenta el diseño, integración e instalación del primer prototipo *Tile PreProcessor* (TilePPr). Este prototipo ha sido diseñado para la operación y lectura del módulo *Demonstrator*, como primer y principal elemento de la electrónica de *back-end*. También se presenta el desarrollo de *firmware* que se ha realizado para los prototipos de la tarjeta *DaughterBoard* y TilePPr.

8.1 Introducción

El Gran Colisionador de Hadrones (LHC) es el más grande y potente acelerador de partículas del mundo. El LHC se encuentra en las instalaciones de la Organización Europea para la Investigación Nuclear (CERN) a 100 metros bajo tierra, dentro de un túnel circular de 27 kilómetros que cruza la frontera de Francia y Suiza. El LHC es el último acelerador de una serie de aceleradores utilizados para aumentar la energía de los haces de protones. La Figura 8.1 muestra el complejo de aceleradores del CERN. Los diferentes aceleradores aumentan la energía de los haces de protones hasta alcanzar una energía de 450 GeV y son inyectados en el acelerador LHC donde finalmente se aceleran hasta su máxima energía.

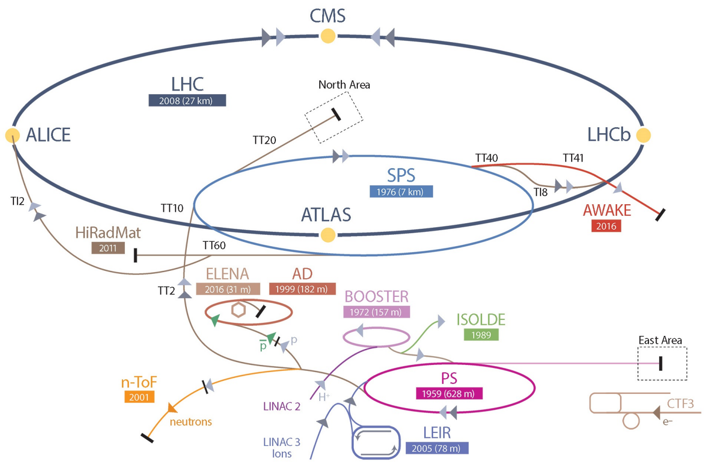


Figura 8.1: Complejo de aceleradores del CERN.

Situados alrededor del anillo del LHC, los 4 principales experimentos analizan las partículas producidas durante las colisiones de los haces de protones. Estos experimentos son: ATLAS, CMS, ALICE y LHCb. Los dos experimentos más grandes, ATLAS y CMS, son detectores de propósito general que están situados en lados opuestos del LHC. Ambos detectores han sido diseñados para medir con precisión las propiedades de las interacciones fuertes y electrodébiles de las partículas elementales , así como nueva física más alla del modelo estándar. Ambos experimentos anunciaron en 2012 el descubrimiento del bosón de Higgs con una masa alrededor de 125 GeV. Por otra parte, el LHCb estudia la violación de la simetría CP, y ALICE investiga el plasma quark-gluón mediante la colisión de iones pesados.

8.1.1 Experimento ATLAS

El experimento ATLAS (Figura 8.2) es un detector de propósito general diseñado para estudiar las partículas resultantes de las colisiones de los haces de protones en el LHC. ATLAS es el detector más grande del LHC con 45 metros de largo, más de 25 metros de altura, y con un peso total de aproximadamente 7,000 toneladas. El experimento ATLAS está compuesto por diferentes subdetectores que estudian las partículas generadas en las colisiones. Entre estos subdetectores se encuentran: el detector interno, los calorímetros electromagnético y hadrónico, y el espectrómetro de muones.

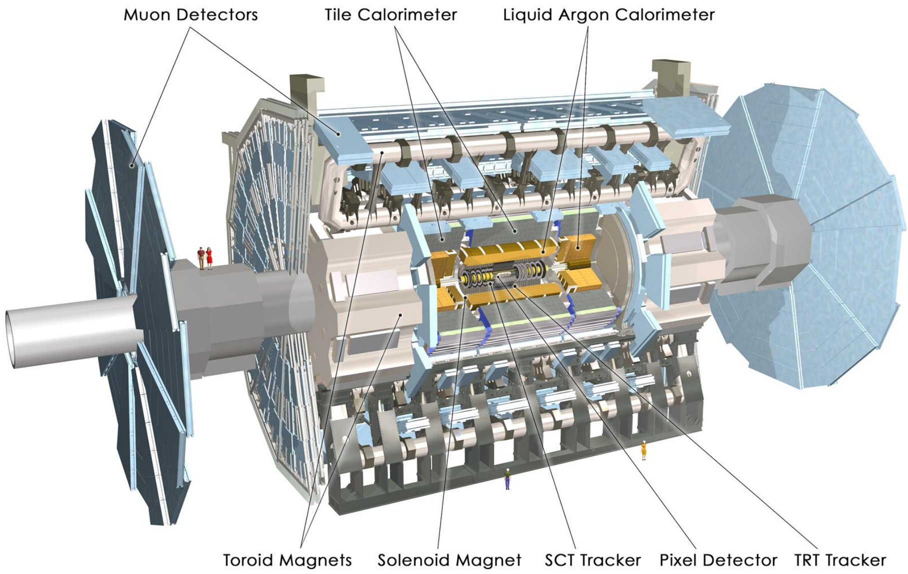


Figura 8.2: El experimento ATLAS.

El detector interno se sitúa en la parte más interna de ATLAS, alrededor del tubo donde circulan los haces. Este detector permite la reconstrucción de los vértices y de las trayectorias de las partículas cargadas que lo atraviesan. Rodeando a este detector se encuentran los calorímetros electromagnético y hadrónico que miden la energía depositada por las distintas partículas. En la capa más externa del ATLAS se encuentra el espectrómetro de muones calculando la trayectoria de las partículas cargadas que los calorímetros no han frenado. Finalmente, el detector ATLAS está rodeado por tres toroides magnéticos que generan un campo de 0.5 Teslas curvando la trayectoria de las partículas cargadas.

8.1.2 Calorímetro Hadrónico TileCal

El calorímetro hadronico de tejas es uno de los subdetectores que componen el experimento ATLAS situándose en la región $|\eta| < 1.7$. TileCal es un calorímetro de muestreo que utiliza acero como material absorbente y centelleador como medio activo. Este subdetector está dividido en un barril central (LBA, LBC) de 5.8 metros de longitud y dos barriles extendidos (EBA, EBC) de 2.6 metros de longitud cada uno. Cada barril está formado por 64 módulos (Figura 8.3), que se dividen a su vez en celdas. Cada una de las celdas del Tilecal se lee utilizando dos fotomultiplicadores (PMT) y fibras especiales que desplazan la longitud de onda de la luz. Un total de 9852 PMTs son necesarios para la lectura completa de TileCal.

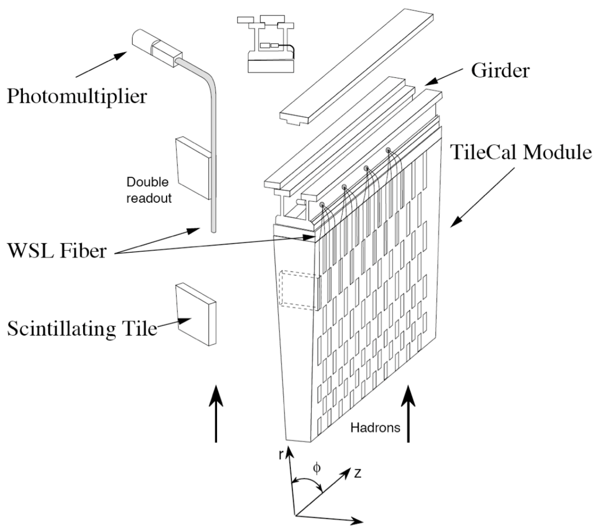


Figura 8.3: Estructura de los módulos de TileCal.

Durante las colisiones, las partículas producidas en el centro de ATLAS y que cruzan el TileCal, depositan su energía en las celdas del detector produciendo cierta cantidad de luz que es guiada hasta los PMTs. Estos PMTs generan un pulso eléctrico con una amplitud proporcional a la luz producida en la celda. La tarjeta 3-in-1 recibe este pulso y lo acondiciona generando dos pulsos analógicos con una relación de amplitud de 1:64. Los dos pulsos generados por la tarjeta 3-in-1 son digitalizados con un ADC de 10 bits utilizando un reloj de 40 MHz síncrono con las colisiones de haces en el LHC. Además, los pulsos son sumados analógicamente en grupos de hasta 5 señales correspondientes a las celdas de una misma η, y enviados al sistema de primer nivel de selección.

Las señales digitalizadas son almacenadas en las memorias de los chips *TileDMU* hasta la recepción de una señal de disparo (L1A), generada por el sistema de primer nivel de selección. Esta señal indica que los datos han sido seleccionados y deben procesarse. Esta selección de primer nivel se produce con una frecuencia máxima de 100 kHz en promedio. Una vez recibida dicha señal los datos son transmitidos a las tarjetas Read Out Drivers (ROD) donde se procesarán, transmitiendo al siguiente nivel de selección la energía y tiempo reconstruidos correspondiente a los pulsos recibidos.

8.1.3 Mejoras del experimento ATLAS y el *High Luminosity LHC*

Durante el año 2026 el acelerador LHC se actualizará dando paso al acelerador HL-LHC. Este nuevo acelerador permitirá aumentar la luminosidad instantánea en un factor 5, en comparación con el actual LHC, y hasta en un factor 10 la luminosidad integrada. El diseño del HL-LHC y la consecuente actualización de los experimentos instalados en él, representa un gran desafío tecnológico. El nuevo acelerador conlleva el desarrollo de nuevas tecnologías de aceleradores como imanes superconductores y cavidades, y sistemas electrónicos que permitan adquirir y procesar la extraordinaria cantidad de datos generada por los experimentos.

El proyecto de actualización del detector ATLAS, llamado *Phase II Upgrade*, está dividido en tres fases que corresponden a los tres periodos largos de mantenimiento (Figura 8.4). Después de la parada técnica LS3, los diferentes subdetectores habrán sido actualizados para operar con las nuevas condiciones de luminosidad HL-LHC. El número de eventos aumentará de 20 a 200 por interacción, requiriendo que los subdetectores proporcionen información con mayor precisión, además de un nuevo sistema de adquisición de datos capaz de manejar el volumen de datos generado.

Algunos de los subdetectores del ATLAS como el detector interno, el *Forward LAr Calorimeter* y las *Forward Muon Wheels* sufrirán más los efectos de la radiación requiriendo la sustitución tanto del detector como de la electrónica.

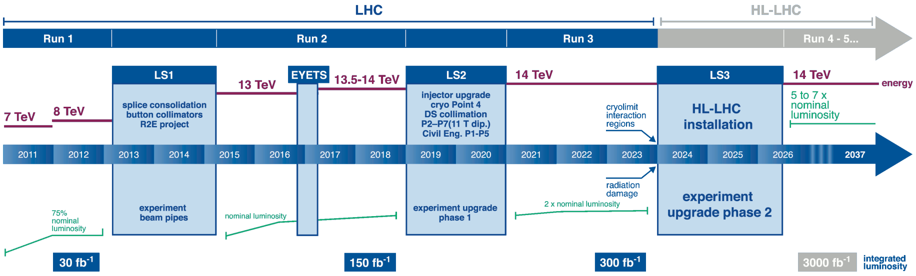


Figura 8.4: Plan del LHC para los próximos 10 años, incluyendo las paradas técnicas y actualizaciones para el aumento de la luminosidad.

Otros subdetectores como los calorímetros o el espectrómetro de muones, menos afectados por la radiación, tan solo necesitarán sustituir la electrónica de lectura y adquisición para hacer frente a los nuevos niveles de radiación y ancho de banda de datos.

8.1.4 Proyecto *Demonstrator*

El proyecto *Demonstrator* pretende la evaluación de la nueva electrónica de adquisición de datos antes de que ésta sea sustituida durante la actualización del experimento ATLAS para el HL-LHC. Dentro del marco de este proyecto se ha construído el módulo *Demonstrator*, el cual incluye prototipos de los nuevos sistemas electrónicos. El módulo *Demonstrator* está dividido en 4 partes iguales, donde cada parte está compuesta por una estructura mecánica de aluminio, llamada (*minidrawer*), sobre la que se distribuyen los siguientes sistemas electrónicos de lectura:

- Hasta 12 *PMT blocks*: cada *PMT block* contiene un fotomultiplicador (PMT, PhotoMultiplier Tube) y su correspondiente tarjeta 3-in-1 modificada para acondicionar las señales generadas. La tarjeta 3-in-1 modificada está diseñada con componentes discretos y proporciona dos pulsos analógicos con un ratio de 1:32 y una anchura a media altura (FWHM, *Full Width at Half Maximum*) de 50 ns. Esta tarjeta está basada en la tarjeta 3-in-1 utilizada actualmente en el TileCal.

- Tarjeta *3-in-1 MainBoard*: permite la operación de hasta 12 *PMT blocks*, además de incluir los ADCs necesarios para la digitalización de las señales de los PMTs. Esta tarjeta también es la encargada de transmitir las señales digitalizadas desde los ADCs a la tarjeta *DaughterBoard*.

- Tarjeta *Adder base*: da soporte físico y alimentación a las tarjetas *adder* que suman analógicamente las señales acondicionadas correspondientes a las celdas de una misma η. Estas tarjetas proporcionan la información analógica de los eventos al sistema de primer nivel de selección de ATLAS.

- Tarjeta *DaughterBoard*: esta tarjeta contiene dos dispositivos de lógica programable (FPGA, Field Programmable Gate Array) de altas prestaciones y conectores ópticos. La *DaughterBoard* es la interfaz con la electrónica de *back-end* transmitiendo, a través de enlaces de alta velocidad, las señales digitalizadas junto a información del detector y, además, recibiendo y distribuyendo las señales de sincronismo y los comandos de configuración.

- Tarjeta *HV board*: Esta tarjeta regula el voltaje de alta tensión aplicado a los PMTs. Existen dos opciones para la distribución de alto voltaje. En la primera opción, la tarjeta *HVOpto card* es alimentada con una tensión de alto voltaje y ésta regula de forma independiente el voltaje de cada canal, mientras en la segunda opción el voltaje de cada uno de los PMTs se proporciona de forma individual desde fuera del detector, y la *HV board* tan sólo distribuye las alimentaciones.

La Figura 8.5 muestra la estructura mecánica de un *minidrawer*, donde se indica las diferentes partes que componen la electrónica de *front-end*.

Además como parte de este proyecto también se evalúan otras dos alternativas más para la adquisición de los pulsos de los PMTs en el HL-LHC, (además de la tarjeta 3-in-1): el chip *Front-end ATlAs tiLe Integrated Circuit* (FATALIC) y el chip *Charge Integrator and Encoder* (QIE). El chip FATALIC es un Circuito Integrado de Aplicación Específica (ASIC) que incluye una etapa de acondicionamiento de la señal con tres ganancias (1, 8, 64) y un ADC de 12 bits integrado también dentro del mismo ASIC. Por otra parte, el ASIC QIE está formado un divisor de corriente con múltiples rangos y un ADC interno. A diferencia del resto de opciones, el QIE proporciona el valor integrado de la señal de corriente generada por el PMT.

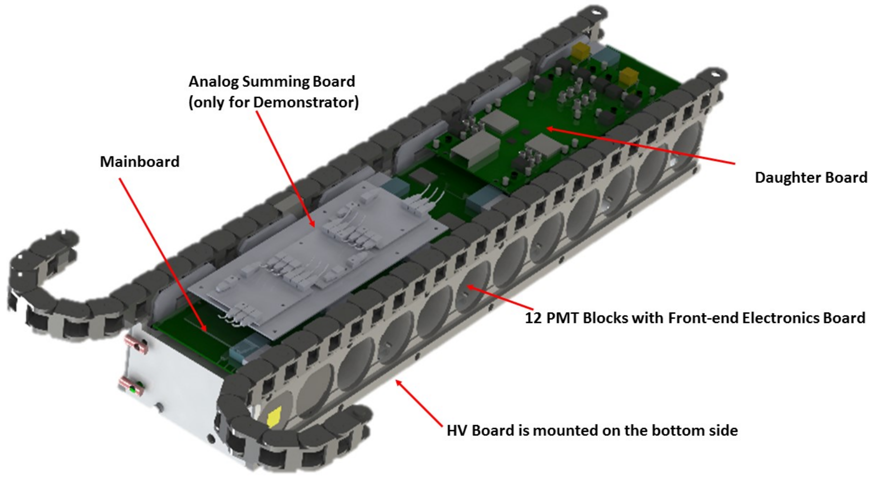


Figura 8.5: Figura detallada de un minidrawer y las diferentes tarjetas electrónicas de *front-end*.

8.2 Prototipo TilePPr

El prototipo Tile PreProcessor es el primer y más importante componente de la electrónica de *back-end* en el proyecto *Demonstrator*. Este prototipo tiene capacidad para leer y operar un módulo del TileCal, representando una octava parte del sistema TilePPr final que será diseñado para el HL-LHC.

El TilePPr recibe y procesa datos digitales del módulo TileCal, además de ser el encargado de la sincronización del detector y transmitir los comandos de configuración para operar la electrónica de *front-end*. El prototipo TilePPr, también se comunica con el Sistema de Control del Detector (DCS) configurando y supervisando el voltaje aplicado a los PMTs. Durante la operación del módulo *Demonstrator*, el prototipo TilePPr almacena cada 25 ns los datos transmitidos por la electrónica de *front-end* en memorias de tipo *pipeline*. Cuando el prototipo TilePPr recibe una señal L1A, éste transmite los datos seleccionados al sistema *Front-End LInk eXchange* (FELIX) y al ROD, integrando de esta forma el módulo *Demonstrator* dentro del sistema de adquisición actual.

Además, el prototipo TilePPr también incluye herramientas digitales para la monitorización de desfases entre señales periódicas. Estas herramientas han jugado un papel importante en la medida de la latencia de los enlaces ópticos con precisiones por debajo de 30 $\mathrm{ps_{RMS}}$, así como para sincronizar el módulo *Demonstrator* con el sistema de Timing, Trigger and Control (TTC), que proporciona el reloj y señales de sincronismo del LHC.

Como parte del proyecto *Demonstrator*, el prototipo TilePPr se ha utilizado para la lectura y operación de las tres opciones para las tarjetas de *front-end* (3-in-1, QIE y FATALIC) durante 3 periodos de pruebas donde se testeó la electrónica con haces de partículas. Además, también se prevé la instalación del módulo *Demonstrator* dentro del actual experimento ATLAS durante una de las paradas cortas del LHC durante el Run 2, donde el prototipo TilePPr se utilizará para su operación y lectura como bloque principal en el *back-end*.

Respecto al diseño del prototipo TilePPr (Figura 8.6), éste ha sido diseñado con un formato de tarjeta doble Advanced Mezzanine Card (AMC). Por tanto, esta placa se puede operar en una tarjeta madre Advanced Telecommunications Computing Architecture (ATCA) o directamente en un sistema Micro Telecommunications Computing Architecture (μTCA).

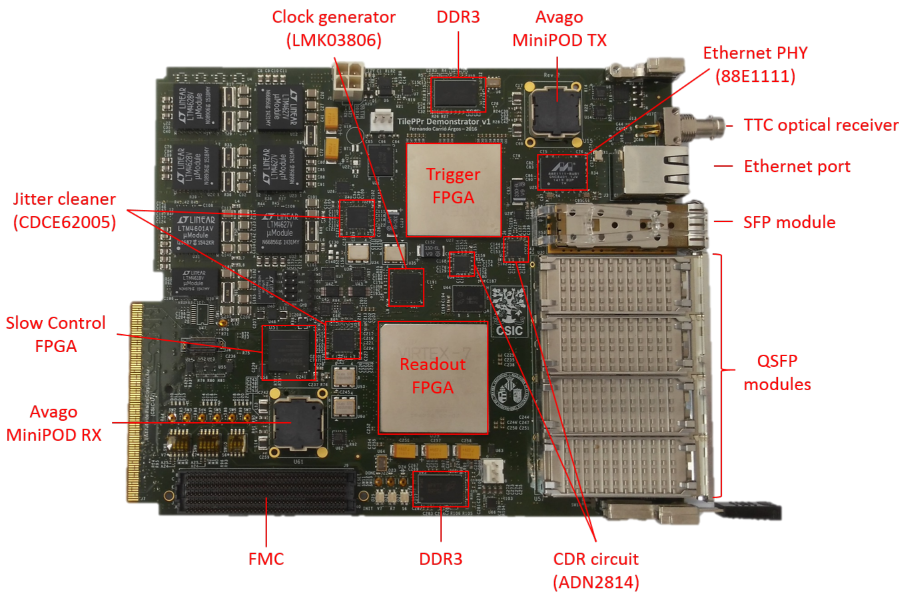
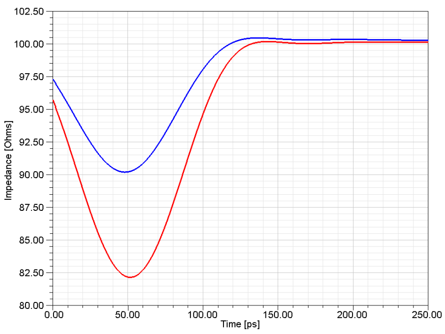


Figura 8.6: Imagen del prototipo TilePPr.

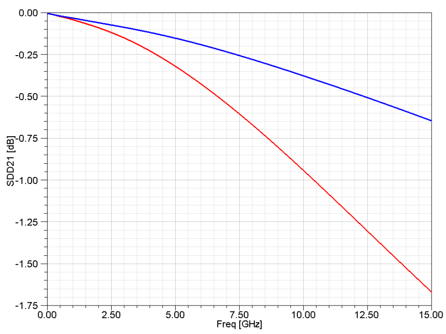
El núcleo principal de la tarjeta está formado por dos FPGAs de la serie 7 de Xilinx: una FPGA Virtex 7 (FPGA *Readout*), y una FPGA Kintex 7, (FPGA *Trigger*). Estas FPGAs contienen transceptores de alta velocidad, una alta densidad de recursos lógicos y un gran número de bloques de procesadores digitales de la señal (DSP). La tarjeta TilePPr integra 4 módulos ópticos Quad Small Form-factor Pluggable (QSFP) para la comunicación con la electrónica de *front-end*, así como otros módulos Avago MiniPOD con fines de evaluación.

Durante el proceso de diseño de la tarjeta PCB (*Printed Circuit Board*), se realizaron multitud de simulaciones de integridad de la señal, especialmente en aquellas líneas destinadas a operar a 10 Gbps. Estas simulaciones constituyeron una etapa crucial tanto en la definición de la geometría de las pistas de alta velocidad, como en la detección y optimización de las discontinuidades de impedancia producidas a lo largo de las pistas de alta velocidad.

Como método de análisis de la integridad de la señal se utilizaron los parámetros *Scattering* (S) extraídos a través de las herramientas ANSYS SIwave y HFSS, así como simulaciones de la técnica de Reflectrometría en el Dominio del Tiempo (TDR). La Figura 8.7 muestra un ejemplo de las simulaciones realizadas para la reducción de la discontinuidad de impedancia producida por condensadores de tamaño 0201 y 0402, donde se comprobó que los condensadores de tamaño 0201 producen una menor degradación de la integridad de la señal.



(a) Comparación de la respuesta TDR entre pistas diferenciales con condensadores *DC-blocking* con encapsulado 0201 (azul) y 0402 (rojo) utilizando una señal escalón con un tiempo de subida de 40 ps.



(b) Comparación de la pérdida por inserción (parámetro S_{DD21}) entre pistas diferenciales con condensadores *DC-blocking* con encapsulado 0201 (azul) y 0402 (rojo).

Figura 8.7: Comparación de los resultados de la simulación TDR y de pérdidas por inserción entre dos pistas con condensadores *DC-blocking* con encapsulado 0201 y 0402.

Una vez construidos los primeros prototipos, se realizaron tests para comprobar que cumplían con las especificaciones de diseño. Como parte de los tests de evaluación del prototipo TilePPr se midieron diagramas de ojo correspondientes a los enlaces ópticos operando a 4.8 Gbps y 9.6 Gbps. La Figura 8.8 muestra un diagrama de ojo obtenido de una de las salidas ópticas de un módulo QSFP conectado al prototipo TilePPr y operando a 9.6 Gbps.

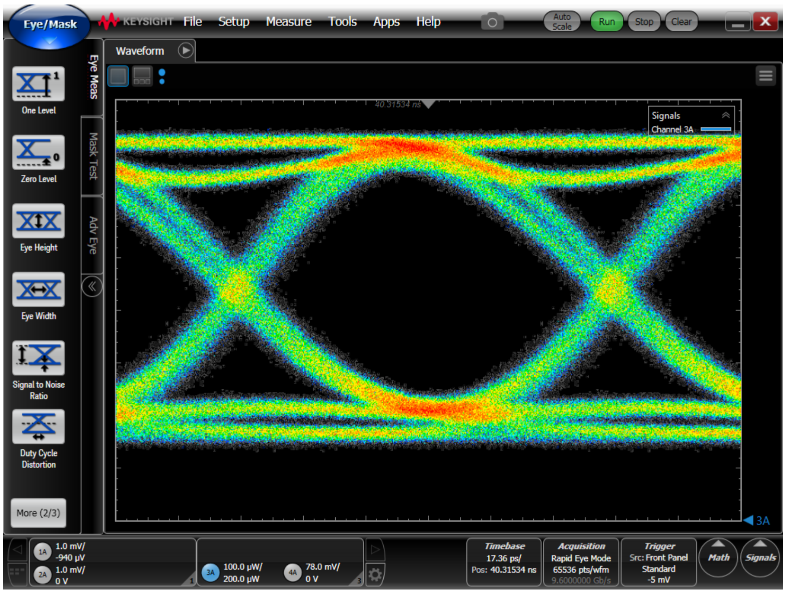


Figura 8.8: Diagrama de ojo correspondiente a la salida óptica de un módulo QSFP operando a 9.6 Gbps.

8.3 Objetivos

Los objetivos de la presente tesis incluyen el desarrollo e instalación de un primer prototipo electrónico para la adquisición de datos del módulo *Demonstrator* que demuestre la viabilidad de la nueva estrategia de adquisición de datos propuesta para el detector TileCal en el HL-LHC. Del mismo modo, este prototipo ha de servir como base para el futuro diseño de la versión final de la electrónica de *back-end* que operará en el HL-LHC. Los objetivos se han divido en diferentes puntos coincidiendo, en gran parte, con la estructura de la tesis:

- Desarrollo de un prototipo de electrónica de *back-end* que cumpla con los requisitos del sistema de adquisición de datos del TileCal para el HL-LHC. Este prototipo deberá ser capaz de operar y leer los datos del módulo *Demonstrator*, así como de transmitir información a los diferentes elementos que forman parte del sistema de adquisición en el HL-LHC. Además el prototipo debe permitir la integración del módulo *Demonstrator* dentro del sistema de adquisición del experimento ATLAS.

- Desarrollo de herramientas digitales basadas en FPGA para la medida de fase entre dos señales periódicas con una precisión inferior a 30 ps_{RMS}. Estas herramientas han de permitir la correcta sincronización del módulo *Demonstrator* con el LHC a través del TilePPr, así como servir de método para el estudio y detección de las variaciones de fase producidas en los relojes transmitidos por cambios de temperatura o de la tensión de alimentación de la electrónica y fibras.

- Integración el prototipo TilePPr con el módulo *Demonstrator* para el estudio del rendimiento de la electrónica diseñada para el HL-LHC. Este estudio, que incluirá pruebas con haces de partículas, permitirá comparar el rendimiento de la nueva electrónica con el de la electrónica actualmente utilizada en el detector TileCal. Estas pruebas se realizarán en las instalaciones del CERN, donde la electrónica será testeada en condiciones similares a la de operación.

8.4 Metodología

La metodología llevada a cabo para la realización de esta tesis doctoral consta de las siguientes fases:

Estudio de los sistemas de adquisición para experimentos de Física de Altas Energías

El trabajo se inició con el estudio del actual sistema de adquisición de datos del experimento ATLAS y, en concreto, de la electrónica del detector TileCal. Asimismo, también se realizó un profundo estudio de las necesidades del nuevo sistema de adquisición de datos para el detector TileCal en el HL-LHC, donde se identificó los requerimientos de la nueva electrónica.

Diseño conceptual del sistema de adquisición

Definidas las necesidades del sistema de adquisición de datos a construir, se propuso el diseño de un prototipo basado en FPGAs y conectores ópticos de alta velocidad. Para realizar dicha propuesta, primero se estudiaron diferentes arquitecturas de transceptores de alta velocidad embebidos en FPGA que permitieran un ancho de banda suficiente y que pudieran establecer comunicaciones de alta velocidad con latencia fija y determinista. Durante este estudio también se tuvo en cuenta que la cantidad de recursos lógicos y de memoria embebida de las FPGAs fuera suficiente para albergar los algoritmos y arquitecturas necesarias. Finalmente, se realizó un extenso estudio para definir qué otros componentes haría falta incluir en el diseño para poder implementar la comunicación a alta velocidad y el resto de funcionalidades requeridas.

Diseño físico y verificación del primer prototipo

Partiendo de los estudios realizados para la propuesta del diseño conceptual, se seleccionaron los componentes que formarían parte del primer prototipo, como son las FPGAs, memorias, dispositivos de reloj y conectores ópticos.

Durante el diseño físico de la tarjeta del TilePPr se realizaron amplios estudios de integridad de la señal con herramientas de simulación de campos electromagnéticos en 3D. Dichos estudios permiten el correcto diseño de la geometría de las pistas, así como la detección de discontinuidades de impedancia a lo largo de las líneas de alta velocidad, producidas por vías diferenciales o condensadores *DC-blocking*.

Como parte final de esta fase de la tesis, se procedió a la verificación de los prototipos fabricados. Para ello, se realizó un estudio de la calidad de las comunicaciones ópticas implementadas con la tarjeta TilePPr utilizando un osciloscopio de muestreo con entradas ópticas y un ancho de banda de 9 GHz.

Implementación de las diferentes funcionalidades en FPGA

Una vez validado el funcionamiento del prototipo TilePPr, se procedió a la programación de las FPGAs para implementar las distintas funcionalidades. La programación de las FPGAs se dividió en dos partes. La primera parte incluye todos los bloques necesarios para la comunicación con el detector TileCal y su integración en el sistema de adquisición del experimento ATLAS. Estos bloques incluyen las siguientes funcionalidades:

- Transmisión de comandos de configuración y señales de sincronismo hacia la electrónica *front-end*.
- Recepción de datos de la electrónica de *front-end* y almacenamiento en memorias de tipo pipeline.
- Transmisión de datos seleccionados a los sistemas ROD y FELIX.
- Recepción de comandos y señales de sincronismo con el sistema TTC.

En relación a los enlaces de alta velocidad, se realizó un amplio estudio del número de recursos necesarios para la implementación de múltiples enlaces ópticos en FPGA utilizando el protocolo GigaBit Transceiver (GBT). Además, también se identificaron las modificaciones que debeberían llevarse a cabo en dicho protocolo para cumplir con los requerimientos de ancho de banda del detector TileCal.

En una segunda parte de la programación de las FPGAs, se realizó un estudio de técnicas digitales en FPGA para la medida de fase entre señales periódicas con precisiones por debajo de los 30 $\mathrm{ps}_{\mathrm{RMS}}$. La implementación de este tipo de técnicas en el prototipo TilePPr es necesaria por dos razones fundamentales: conocer la diferencia de fase entre los relojes locales del TilePPr y el reloj del acelerador para poder sincronizar la electrónica de *front-end* con los cruces de haces en el ATLAS; y la continua monitorización de la fase del reloj transmitido a la electrónica de front-end para estudios sobre su estabilidad en el tiempo.

Como resultado de este estudio, se propuso un nuevo circuito, llamado *Over-Sampling to UnderSampling* (OSUS), basado en el circuito *Digital Dual Mixer Time Difference* (DDMTD). El circuito OSUS mejora las prestaciones del circuito DDMTD sobremuestreando las señales de entrada y descomponiendo las señales resultantes en señales submuestreadas. Además se analizaron diferentes métodos de *deglitching* para mejorar la precisión de la técnica de submuestreo, a través de la estimación temporal de los flancos de subida de las señales resultantes. Tras el análisis de los diferentes métodos de *deglitching*, se propone un nuevo método llamado *Average Position* que mejora la precisión del circuito.

Obtención y análisis de resultados obtenidos con el prototipo TilePPr

Por último, el objetivo final de esta tesis era comprobar la viabilidad del sistema de adquisición propuesto para su operación en el HL-LHC, siendo además capaz de integrar el módulo *Demonstrator* dentro del sistema de adquisición actual. Para ello, se instaló el prototipo TilePPr en las instalaciones de la línea H8 del acelerador SPS, junto al módulo *Demonstrator* que incluía la electrónica de *front-end* diseñada para el HL-LHC. Durante las pruebas con haces de partículas, el prototipo TilePPr fue utilizado para leer los datos digitalizados por el módulo *Demonstrator* donde distribuyó las señales de sincronización a la electrónica de *front-end* y transmitió los datos seleccionados al actual sistema de adquisición para su posterior análisis. Finalmente, los datos recogidos durante las pruebas fueron analizados y validaron el correcto funcionamiento del sistema de adquisición de datos diseñado para la actualización del detector TileCal.

8.5 Conclusiones

Esta tesis doctoral se centra en el diseño, producción e integración del primer prototipo TilePPr como parte del sistema de adquisición del detector TileCal en el HL-LHC. El proyecto *Demonstrator* tiene como objetivo la evaluación de la nueva electrónica del sistema de adquisición antes de su instalación en el HL-LHC. Como parte de este proyecto se ha construido el módulo *Demonstrator* equipado con la nueva electrónica de *front-end* diseñada para el HL-LHC.

El prototipo TilePPr ha sido diseñado para leer y operar el módulo *Demonstrator* implementando la nueva arquitectura del sistema de adquisición para el HL-LHC y, a la vez, permitiendo la integración del módulo *Demonstrator* en el sistema actual de adquisición de datos del ATLAS. Los planes del proyecto *Demonstrator* incluyen la instalación del módulo *Demonstrator* en el actual experimento ATLAS reemplazando uno de los actuales módulos.

En este documento se presenta una descripción detallada del diseño y validación del prototipo TilePPr. Durante su diseño se realizaron extensos estudios de integridad de señal, donde se ha prestado especial atención a la identificación y optimización de las discontinuidades de impedancia producidas a lo largo de las líneas de alta velocidad. Como parte de las pruebas de validación del prototipo, se realizaron test de BER (Bit Error Ratio) y diagramas de ojo de los enlaces ópticos. Los resultados presentados en el Capítulo 4 muestran un BER mejor que $5 \cdot 10^{-17}$ con un nivel de confianza del 95 %, y un *jitter* total para un BER de 10^{-18} de 49.5 ps con una σ de 2.5 ps a 4.8 Gbps y 57 ps con una σ de 2.3 ps a 9.6 Gbps.

Debido al limitado número de recursos de reloj en la FPGA *Readout* se modificó el módulo GBT-FPGA IP core, donde el *Phase-Locked Loop* (PLL) del receptor fue reemplazado por un circuito *Blind Oversampling Clock and Data Recovery* (BO-CDR) implementado con recursos lógicos dentro de la FPGA. Esta modificación permitió la implementación del número de enlaces GBT necesarios en la FPGA *Readout*. Por otra parte, a raíz de los requerimientos del nuevo sistema de adquisición, también fue necesario modificar dicho módulo para incrementar el ancho de banda de recepción de 4.8 Gbps a 9.6 Gbps. Además, los diferentes bloques *firmware* tanto en la electrónica de *front-end* como en la de *back-end* que intervienen en la adquisición y transmisión de los datos han sido diseñados para proporcionar una latencia fija y determinista.

Otra contribución importante de esta tesis es la implementación de un circuito digital en FPGA, llamado OSUS, para la medida de la diferencia de fase entre señales periódicas con una precisión de 30 $\mathrm{ps_{RMS}}$. Esta herramienta permite la sincronización del módulo *Demonstrator* con el sistema TTC y la monitorización del reloj transmitido a la electrónica de *front-end*. Además, a través del circuito OSUS se han realizado estudios de la estabilidad de latencia de la comunicación con el *front-end* en dos situaciones: después del reinicio de la electrónica de *front-end* y durante largos periodos de tiempo.

Se han estudiado diferentes técnicas de *deglitching* para la mejora de la resolución del circuito OSUS a través de la estimación temporal de los flancos de subida de las señales sobremuestreadas. Los estudios realizados concluyeron que el método de *Average Position* propuesto mejora la resolución del circuito en aproximadamente 15 $\mathrm{ps_{RMS}}$ respecto al método de *First Edge*.

Por último, durante los periodos de pruebas con haces de partículas, el prototipo TilePPr fue utilizado como elemento principal de la electrónica de *back-end*, donde proporcionó el reloj del LHC y los comandos de configuración al módulo

Demonstrator, recibiendo las señales digitalizadas de los PMTs cada 25 ns y transmitiendo los datos seleccionados a los sistemas ROD y FELIX. Los datos recogidos durante estas pruebas han permitido evaluar el rendimiento de la nueva electrónica de *front-end* diseñada para el HL-LHC comparándola con la electrónica actual.

El diseño del prototipo TilePPr será utilizado como base para el desarrollo de la versión final del TilePPr para el HL-LHC. El futuro TilePPr será capaz de operar hasta 8 módulos completos y estará compuesto por una tarjeta ATCA que albergará 4 módulos AMC. Gran parte de los bloques de *firmware* presentados en este documento, tales como el circuito OSUS o el Tile GBT-FPGA IP core, serán utilizados en la versión final del TilePPr.

List of Acronyms

ADC	Analog-to-Digital Converter.
AMC	Advanced Mezzanine Card.
ASIC	Application-Specific Integrated Circuit.
ATCA	Advanced Telecommunications Computing Architecture.
ATLAS	A Toroidal LHC ApparatuS.
BC	Bunch Crossing.
BCID	Bunch Crossing IDentifier.
BCR	Bunch Counter Reset.
BER	Bit Error Ratio.
BO-CDR	Blind Oversampling Clock and Data Recovery.
CDC	Clock Domain Crossing.
CDR	Clock and Data Recovery.
CERN	European Organization for Nuclear Research.
CIS	Charge Injection System.
CLB	Configurable Control Block.
CPU	Central Processing Unit.
CRC	Cyclic Redundancy Check.
CTP	Central Trigger Processor.
DAC	Digital-to-Analog Converter.
DAQ	Data AcQuisition.
DB	DaughterBoard.
DCS	Detector Control System.
DDMTD	Digital Dual Mixer Time Difference.
DMTD	Dual Mixer Time Difference.

DSP	Digital Signal Processor.
ECR	Event Counter Reset.
FEB	Front-End Board.
FEC	Forward Error Correction.
FELIX	Front-End LInk eXchange.
FEXT	Far-end crosstalk.
FF	Flip-Flop.
FIFO	First In, First Out.
FMC	FPGA Mezzanine Connector.
FPGA	Field Programmable Gate Array.
FSM	Finite State Machine.
GBT	GigaBit Transceiver.
HG	High Gain.
HL-LHC	High Luminosity LHC.
IPMI	Intelligent Platform Management Interface.
JTAG	Joint Test Action Group.
L0A	Level-0 trigger Accept.
L1A	Level-1 trigger Accept.
LFSR	Linear-Feedback Shift Register.
LG	Low Gain.
LHC	Large Hadron Collider.
LSB	Less Significant Bit.
LTP	Local Trigger Processor.
MB	MainBoard.
MMCM	Mixed-Mode Clock Manager.
MSB	Most Significant Bit.
MUX	MUltipleXer.
NEXT	Near-end crosstalk.
OSUS	OverSamling to UnderSampling.
PCB	Printed Circuit Board.
PLL	Phase Locked Loop.
PMT	PhotoMulTiplier.
PRBS	Pseudo-Random Binary Sequence.

PU	Processing Unit.
QSFP	Quad Small Form-factor Pluggable.
RAM	Random Access Memory.
ROD	Read Out Driver.
RTM	Rear Transition Module.
RTT	Round-Trip Time.
SFP	Small Form-factor Pluggable.
TDAQ	Trigger and Data AcQuisition.
TDAQi	Trigger and Data AcQuisition interface.
TDC	Time to Digital Converter.
TDR	Time Domain Reflectometry.
TileCal	Tile Calorimeter.
TilePPr	Tile PreProcessor.
TTC	Trigger, Timing and Control.
UI	Unit Interval.
VCO	Voltage-Controlled Oscillator.

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