Doctorado en Ingeniería Electrónica

Tesis Doctoral

Contributions to Phase Two of AGATA electronics

Autor:

Javier Primitivo Collado Ruiz

Directores:

Vicente González Millán

Andrés Gadea Raga

Valencia, noviembre 2019

Acknowledgements

I would like to start with a grateful thank to my supervisors Vicente Gonzalez and Andres Gadea, who first placed their trust in me to carry out this project, and supported in good and in the bad moments of its development. Only they have the best idea of the mountains we had to climb to carry out this thesis. I would like to thank also to the TEDRA team member Enrique Sanchis, who, together with Vicente accepted me to join them five years ago.

Furthermore, I would like to thank formally to the IFIC (Instituto de Fisica Corpuscular) CSIC and the University of Valencia for hosting me during my thesis period. The work of this thesis has been partially supported by the Ministerio de Ciencia, Innovación y Universidades Spain, under grants SEV-2014-0398, FPA2014-57196-C5 and FPA2017-84756-C4, by the European Commission FEDER funds and by the Generalitat Valenciana, Conselleria d'Educació, Investigació, Cultura i Esport under the grant PROMETEU/2019/005. Furthermore, I would like to thank to the Keysight Technologies Spain collaboration for the equipment for external board measurements on the Chapter 6.

I also like to thank to many members of the AGATA collaboration, in particular to the Phase 2 electronics development team, for the long discussions and joint hard work, without with this thesis would have never been feasible: Alberto Pullia, Amel Korichi, Erik Legay, Gustav Vinther-Jørgensen, Ian Lazarus, Laurent Charles, Nabil Karkour, Nicolas Dosme, Mos Kogimtzis and Xavier Lafay. Also I would like to thank to many others I meet from AGATA collaboration and worked together not mentioned before, especially with Diego Barrientos and Emmanuel Clement in Phase 1.

Me gustaría agradecer también a todos los con los que he compartido numerosas horas en el laboratorio TEDRA, ayudándonos los momentos más complicados: Xavi Egea, Jose María Blasco y Jose Manuel Deltoro. También añadir a aquellos con los que he compartido muchas horas en el IFIC y cuyas conversaciones han ayudado sin duda a avanzar en esta tesis: Fernando Carrió y David Calvo.

También agradecer al equipo de técnicos del IFIC y del departamento de Ing. Electrónica de la ETSE que me han ayudado en numerosas ocasiones. Sin olvidarse de aquellos a los que he codirigido trabajos fin de grado o han hecho sus prácticas con nosotros: Joel, con especial agradecimiento por la interfaz gráfica de test; Jorge y Agustin, por su inestimable ayuda en los test de la fuente de alimentación de la Fase 1, Miguel, Jose y Josep.

Ya a nivel más personal, me gustaría agradecer a mucha gente que me ha acompañado estos años y aportado en otros niveles. A los que conocí en Burjassot durante mi tiempo en la ETSE y el IFIC: Javi, Eva, Silvia, Gess, Ramón, Arnau, Carmen, Pablo, Delia, Manu, Jorge. A mi maestro, Toni Ruz y a toda la Escuela Nin Ruz Ryu: Raúl, Hector, Pablo, Alex, Raquel, Dani, Jose, Jorge…. Al grupo musical Oktopus, Guillem, Helder y Amparo, que me esperan pacientemente de mi descanso para terminar este texto. A los que me soportan todos los días: Víctor, Dimitri, Alex. Estefi, Iván, Jahna, Patri, Aarón, Carlotes, Roca, Andres, Alejandro y por supuesto todos los de LEDC que aún no he mencionado Juan, Dani, Mayte (y miniMay), Marco, Natalia, Paw, Natalia, Juanito, Lorena, Álvaro, Alvar, Iván, Víctor, Carlos, Marc. Sin olvidarse de los que están más lejos, pero siguen presentes y he visitado durante mis viajes en la tesis: Guillermo, Manu, Nieves, Pau, Mari Paz, Lucia, Jorge, Miguel Ángel. Con premio especial a quien más me ha sufrido últimamente con la tesis, Lorena. A mis compañeros de Recreación: Fernando, Vero, Elías y Ángela. A mis físicos dispersos por el mundo: Guillem, Alberto, Sara, María L., María G., Elena, Laura, Silva, Ana, Loli, Cristian, Carlos, Néstor.

Por último, a mi Familia, sobretodo mis padres, que nunca me han dejado ni dejarán de lado, a mi hermano Dani y a Hajni que me han apoyado en todo aun estando lejos y con especial atención a mi sobrina Luna, a quien dedico esta tesis.

Abstract

In the field of Nuclear Physics, high-resolution gamma ray spectroscopy is an accurate method to perform nuclear structure studies, retrieving the energy and angular distributions from gamma photons emitted in the transition between nuclear states. In order to obtain the nucleus in an excited state, such that will emit gamma-rays, we are forced to collide matter, doing nuclear reactions (in the in-beam spectroscopy) or resort to the radioactive decay (decay spectroscopy). The High Purity Germanium (HPGe) semiconductor detectors have shown to provide good response as gamma-ray detector. As other semiconductor detectors, HPGe produce, with high sensitiveness, a current proportional to gamma ray energies while there are subject to high voltage inverse polarization, in cryogenic conditions.

The AGATA (Advanced GAmma Tracking Array) HPGe detector array is a state-of-the-art detector array for the gamma ray spectroscopy technique in nuclear physics. In order to improve the sensitivity, AGATA HPGe detectors have the outer contact divided in 36 segments in order to determine photon position and energy deposited in each segment. With the interaction energy and position information is possible to reconstruct (Track) the gamma-ray interaction sequence using tracking algorithms. With such technique is possible to maximize the sensitivity of the detector array (energy resolution and P/T) without using part of the detection solid angle for the anti-Compton active shields. In addition to the segmented detectors, the positions sensitive HPGe arrays require sampling electronics with spectroscopic signal-to-noise ratios, which provides the traces to be processed by the Pulse Shape Analysis algorithms.

To provide maximum efficiency and sensitivity, the AGATA project aims to construct a 4π solid angle detector array. This geometry optimizes as well the information obtained, something that is especially important in experiments using expensive radioactive ion beams. Another goal in the construction of AGATA is the mobility of the array. AGATA is installed in different laboratories to take advantage of the variety of beams and complementary instrumentation existing in different European centres.

The AGATA project is currently in its Phase 1, using a second generation electronics, which aims at building a 1 π solid angle coverage. This requires 45 detectors, that today are partly instrumented with the previous Phase 0 electronics, mostly design and produced in the period from 2005 to 2007. Presently, the main goal for the AGATA collaboration, regarding electronics, is the development of the Phase 2 version, with the objective of instrumenting 180 detectors, which is partly done by the work described in this thesis. The main improvements for this Phase 2 electronics are: the integration of all the electronics from digitizers to readout, including Pre-processing, in one standalone system and the use of Ethernet as the readout protocol. The Ethernet technology will enable a multipoint connection and the possibility to distribute the data anywhere within the AGATA processing farm.

One of the main problems found in the integration of all the system is the optimization of the FPGA resources used in the Pre-processing. Despite of the increase in the high-speed transceiver data rates of the last FPGA developed in the industry, the number of transceivers on the devices is limited. Furthermore, the FPGA cost increases largely with the amount of transceivers, which is an issue for the AGATA detectors, with a need for a large number of transceivers but not at an especially high data rate. To reduce system complexity, cost and power, the number of high speed digital lines is optimized through data aggregation, increasing the speed data rate of each line but with a reduction of 4 to 1 in the total number of transceiver lines. The solution is carried out through the Input Data Mezzanine board, conceived and developed completely under this thesis work.

From a technological point of view, the main objective of the thesis is to prove the possibility of reading up to 40 optical or copper low rate inputs, using JESD204 or equivalent protocol, in the FPGA using only 10 transceivers through a time division multiplexing technique. The work is done with state-of-the-art in hardware-software FPGA design, high-speed digital design and digital communications, as well as with the knowhow of the AGATA current electronics. Although this device is designed for AGATA, we consider that this technology will be of interest for other instruments and applications.

Resumen

En el campo de la física nuclear, la espectroscopia de rayos gamma de alta resolución es un método preciso para estudiar la estructura del núcleo, extrayendo la energía y la distribución angular de los fotones gamma emitidos en las transiciones entre estados nucleares. Para obtener núcleos en un estado excitado y por tanto emitan rayos gamma, hemos de hacer chocar la materia, produciendo reacciones nucleares (espectroscopia de haz) o recurrir a desintegraciones radiactivas (espectroscopia de desintegración). Los detectores de semiconductor de germanio de alta pureza (HPGe) han demostrado tener una buena respuesta interaccionando con rayos gamma. Al igual que otros detectores de basados en semiconductores, cuando se los somete a alto voltaje, los detectores HPGe producen una alta corriente de medida proporcional a la energía de los rayos gamma incidentes.

El multi-detector HPGe AGATA (Advanced GAmma Tracking Array) es uno de los espectrómetros gamma de alta resolución más avanzados que existen dedicado al estudio de la física nuclear. Para maximizar la sensibilidad, los detectores HPGe de AGATA tienen los contactos exteriores divididos en 36 segmentos, de este modo se puede determinar la posición del fotón y la energía depositada en cada una de estas partes. Con la información sobre la posición y la energía de los fotones es posible reconstruir las interacciones de los rayos gamma a través de los algoritmos de tracking. Gracias a esta técnica, es posible maximizar la sensibilidad del detector (resolución energética y factor P/T) sin necesidad de utilizar parte del ángulo sólido de detección para otros detectores dedicados a la supresión del efecto Compton. Además de los detectores mismos, los detectores de HPGe sensibles al posicionamiento requieren una electrónica de muestreo con ratios señal a ruido de calidad espectroscópica, que capturen y digitalicen las trazas para ser procesadas por los algoritmos de análisis de forma de pulso (Pulse Shape Analysis).

Para conseguir la máxima sensibilidad y eficiencia, el proyecto AGATA busca construir el multi-detector cubriendo una superficie total con 4π de ángulo sólido, optimizando la información obtenida, algo especialmente crítico en experimentos que usan

costosos haces de iones radiactivos. Otro objetivo en la construcción de AGATA es su movilidad. El multi-detector AGATA se instala en diferentes laboratorios para aprovechar la variedad de haces e instrumentación complementaria que existen en los diferentes centros europeos.

El proyecto AGATA se encuentra actualmente en su Fase 1, que busca cubrir hasta 1π de ángulo sólido y se encuentra funcionando con la segunda generación de electrónica. Los 45 detectores instalados actualmente utilizan en parte la anterior generación o Fase 0 de electrónica, que fue diseñada y producida entre 2005 y 2007. El principal objetivo a nivel de electrónica en la colaboración AGATA es el desarrollo de la nueva generación para la Fase 2, que busca instrumentar 180 detectores y la cual se ha desarrollado parcialmente en esta tesis. Los principales objetivos de la electrónica para la Fase 2 son la integración de en un solo dispositivo, desde la digitalización hasta la salida de datos y el protocolo Ethernet como comunicación para dicha salida. La tecnología Ethernet permitirá una conexión multipunto y la posibilidad de leer los datos desde cualquier sitio de la granja de procesado de AGATA. También se han tenido en cuenta, en el diseño, facilitar el mantenimiento y evitar la obsolescencia de los componentes utilizados.

Uno de los grandes problemas que se encuentran en la integración del sistema electrónico de AGATA es la optimización de los recursos en la FPGA por parte del Pre-procesado. Con el avance de la tecnología, a pesar del aumento de la tasa de datos por transceptores de alta velocidad en estos dispositivos (entre 16 y 32 Gbps), el número de transceptores en las FPGAs no se ha incrementado sustancialmente. Además, el coste de los dispositivos FPGA aumenta considerablemente con el número de transceptores. Esto es un problema crítico en AGATA, ya que requiere un gran número de canales digitalizados por dispositivo, pero no a una velocidad especialmente alta (sobre 2 Gbps). Para reducir la complejidad del sistema, el coste y la potencia total, el número de líneas de alta velocidad se ha optimizado mediante agregación de datos por multiplexado en tiempo, incrementando la velocidad de tasa de datos, pero con una reducción en el número total de éstas de 4 a 1. Esta solución se ha llevado a cabo a través de la tarjeta Input Data Mezzanine, concebida y desarrollada enteramente en esta tesis.

El objetivo principal desde el punto de vista científico es demostrar la posibilidad de leer 40 canales bajo el protocolo JESD204 o uno equivalente, vía fibra óptica o por cable físico, únicamente con 10 transceptores de alta velocidad de una FPGA, gracias a la técnica de multiplexado por división en el tiempo. La base de la que se parte es la electrónica actual de AGATA y se apoya en tecnología del estado del arte sobre diseño hardware y software para FPGA, diseño digital de alta velocidad y comunicaciones digitales. A pesar de que este diseño se ha realizado principalmente para el proyecto AGATA, consideramos que esta tecnología será de interés para otros instrumentos y aplicaciones.

Contents

Abstract III

Resumen V

Chapter 1: Technology in Nuclear Gamma-Ray Spectroscopy 1

1.1 Nuclear Gamma Ray Spectroscopy 1

1.1.1 Brief introduction to the Atomic Nucleus. 2

1.1.2 Gamma radiation Interaction with matter 5

1.1.3 Detectors for gamma-ray detection in Nuclear Science 6

1.1.4 High-Resolution Gamma-Ray spectroscopy and Germanium detectors 9

1.1.5 In-Beam Spectroscopy 11

1.1.6 Gamma Ray Detector Arrays and Tracking 15

1.1.7 The Gamma-ray Tracking Concept 19

1.1.8 AGATA The Advanced Gamma Tracking Array 20

1.2 Technology on the Edge 23

1.2.1 High speed links. 23

1.2.2 Instrumentation technology. 27

1.2.3 Parallel processing and FPGA. 28

Chapter 2: AGATA spectrometer electronics and Read Out 31

2.1 General description 33

2.2 Detector preamplifier 34

2.3 Digitalization 35

2.3.1 First generation (Phase 0) digitizer 35

2.3.2 Second generation (Phase 1) digitizer 36

2.4 Pre-processing 42
2.4.1 Triggering system 42
2.4.2 Energy processing 43
2.4.3 Comparison of the Phase 0 and Phase 1 Pre-processing 46
2.5 Trigger and Synchronization system 49
2.6 Data acquisition system 52
2.7 Phase 2 electronics requirements 53
Chapter 3: AGATA Phase 1 Electronics Test System 55
3.1 Motivation and testbench 57
3.2 Performed Tests 58
3.3 Software 60
3.3.1 Stage I: Automation Code 60
3.3.2 Stage II: Graphical User Interface 62
3.3.3 Stage III: Standalone test upgrade 64
3.4 PSU analysis. 65
Chapter 4: AGATA Phase 2 electronics 67
4.1 Goals for the Phase 2 Electronics of AGATA 69
4.2 Design of the AGATA Phase 2 Electronics 71
4.2.1 Preliminary PACE design. 71
4.2.2 The Phase 2 electronic collaboration. 72
4.2.3 IDM prototype and PACE design 73
4.2.4 Description of the AGATA Phase 2 electronics 74
4.3 Production PACE design 79
Chapter 5: Input Data Mezzanine Design 81

5.1 Design requirements 83
5.2 The IDM design 84
5.2.1 Input Area. 85
5.2.2 Link Aggregator Area. 86
5.2.3 FMC Output Area. 90
5.2.4 Control Area 91
5.2.5 Clock Network. 98
5.2.6 Power Supply. 100
5.3 Timing and High Speed considerations 103
5.3.1 Design, Stack-up and materials. 103
5.3.2 Differential line design 106
5.3.3 Synchronous clock networks 108
5.4 Mechanical, Power and High Speed analysis. 108
5.4.1 Power analysis. 108
5.4.2 Mechanical simulation 110
5.4.3 High speed analysis 111
5.5 Layout and prototype production 113
5.5.1 Layout 113
5.5.2 Manufacture and prototype productions 114
Chapter 6: Test and validation. 117
6.1 Preliminary tests 119
6.1.1 Test for IDM v1.2 119
6.1.2 Test for IDM v1.3 119
6.2 The data receiver firmware system for CAP-PACE 120

6.2.1 The CAP Pre-processing firmware description. 120
6.2.2 The receiver module 122
6.2.3 Other Firmware modules 127
6.3 The IDM testbench 128
6.3.1 Testbench description 128
6.3.2 Verification of the data path. 131
6.4 The AGATA Phase 2.0 Electronics proof-of-concept. 139
Chapter 7: Conclusions. 143
List of figures XIII
List of tables XIX
References XXI
Appendix A XXIX
Appendix B XXXI
Appendix C XXXV
Appendix D XLIII

Chapter 1:
Technology in Nuclear Gamma-Ray Spectroscopy

1.1 Nuclear Gamma Ray Spectroscopy

The first experiment identifying high energy photons was carried out on November 1895, when Roentgen discovered the X-Rays with his experiments using cathode ray tubes [1]. Furthermore, the following year Becquerel demonstrated the existence of radiation with a photographic plate becoming darkened just with uranium salt and no sun exposure, being in this way the first radiation detector. Curie improved the detection with the piezoelectric effect of quartz and discovered radiation as general effect on matter in radioactive substances. [2]

Those discoveries lead to the idea of the nucleus in 1911 as the origin of the radiation, opening a new chapter of science thanks to the ideas about the structure of the nucleus from Rutherford and the experiments of Geiger and Marsden. Further experiments in 1940s and 1950s would reveal that nuclei are no longer the fundamental units of the universe as it was thought. [3]

The nuclear gamma-ray spectroscopy is the quantitative analysis of the photon spectra emitted by a nucleus. These gamma-ray photons, occurring during the transitions of the nucleons (protons and/or neutrons) between two quantal states in the nucleus, are on the very high energy side of electromagnetic spectrum. With gamma-ray spectroscopy techniques it is possible to measure basic nuclear properties of excited nuclear states such as excitation energy, angular momentum (spin) and parity using conservation laws and electromagnetic selection rules. In addition, the determination of decay probabilities of nuclear states (with lifetime measurements) gives direct information on the relationship between the initial and final states within the nucleus.

The many-body nature and the fact that it is formed by two types of fermions, characterizes the atomic nucleus as one of the most complex systems in nature. The advancement in the study of the nucleus and its complexity requires each time more accurate and complete information from the detectors that become our eyes into the tiny world of matter.

1.1.1 Brief introduction to the Atomic Nucleus.

Presently, the science vision of the matter is that it's compound of several fundamental particles, including the ones that were earlier thought to be and conformed the nucleus. Each element in nature, in whatever state, is compound by a central core called nucleus, with positive electric charge, and several electrons in quantized atomic shells with negative charge. These shells define many of its electrochemical or atomic properties.

The nucleus is responsible for the radiation saw by those early researchers and is composed itself by a certain number of particles, i.e. protons and neutrons. The number of particle in the nucleus is called mass number A, and, due to the fact that both particles have a similar mass, gives an approximate value of the total mass per nucleus. Protons have positive charge, and neutrons, with no electrical charge, are needed to stabilize the nuclei.

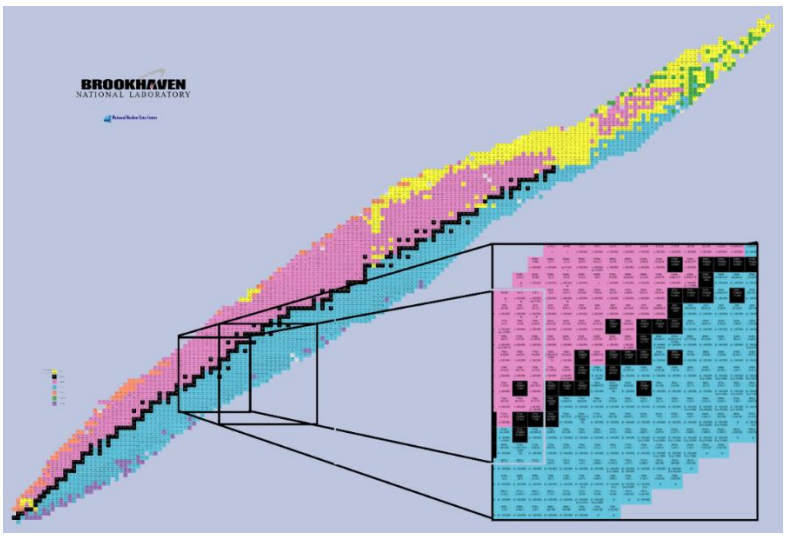

Fig. 1.1. Table of nuclides with the stable elements in black and for the other nuclides the colour indicates the type of decay (or radiation) happening in the unstable nuclei, i.e. red: β+, blue:β-, orange: proton-decay, yellow: α-decay, purple: neutron-emitters

The number of protons Z or atomic number, define the true name of the element because of its chemical importance. The number of neutrons N defines a series of isotopes, elements with identical chemical properties and name but with different amount of neutrons, with different nuclear properties, lifetimes and levels. This extends the periodic table set by chemical or atomic definitions to the table of nuclides, found on Fig. 1.1.

There are around 3000 nuclei discovered, although only about 300 hundred are stable. They respond to particular characteristics like proton-neutron relation, magical numbers and presence of drip-lines, as well as other aspects as geometrical distribution (deformation) or the presence of collective rotational and vibrational states at the Fermi level [4].

Each non stable element will decay by emitting a Beta, Alfa, heavier particles or even, in extreme cases, neutrons or protons, transforming the nuclei into another element. The Alfa decay is an emission of the equivalent of a Helium nucleus (2 protons and 2 neutrons) from a heavier nucleus; the Beta decay is the emission of an electron (β-) plus and antineutrino or a positron (β+) and a neutrino. The positron (anti-matter partner of the electron) usually annihilates with another electron in the matter into two photons with the energy corresponding to the electron mass, i.e. 0.511 Mev [5].

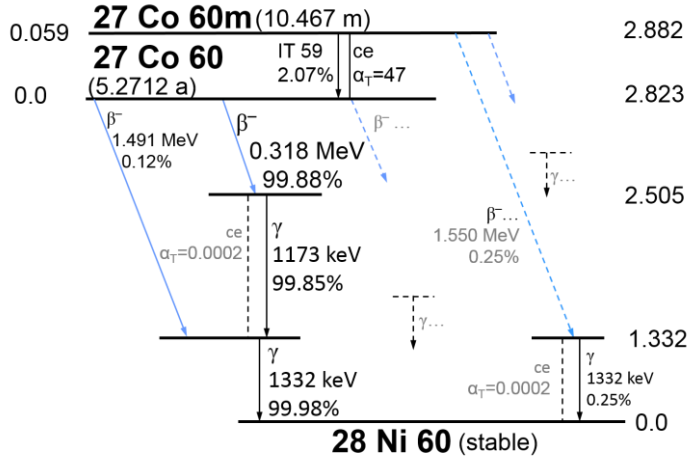

Fig. 1.2. Level-Scheme of Ni60 populated in the β-decay of Co60. [6]

In the decay of a nucleus, several excited nuclear levels can be populated on the daughter nucleus. This nuclear levels mostly de-excite to lower or fundamental energy levels emitting the energy difference as electromagnetic radiation, i.e. gamma-ray photons. Taking into account the nuclear shell structure, the transition energies are related to the nuclear shells (following the Pauli exclusion principle since protons and neutrons are Fermions) and give valuable information to understand the internal structure. The energy

of these photons gives direct information of the excited levels and their de-excitation, revealing themselves as specific energy peaks on the gamma ray spectra [3]. With energy levels and data from each nuclide, the decay (or de-excitation) level-scheme is elaborated as for example in the case of Co60 decay, shown in Fig. 1.2, representing the probability of decay for each level (the branching ratio) and type of radiation emitted in each decay.

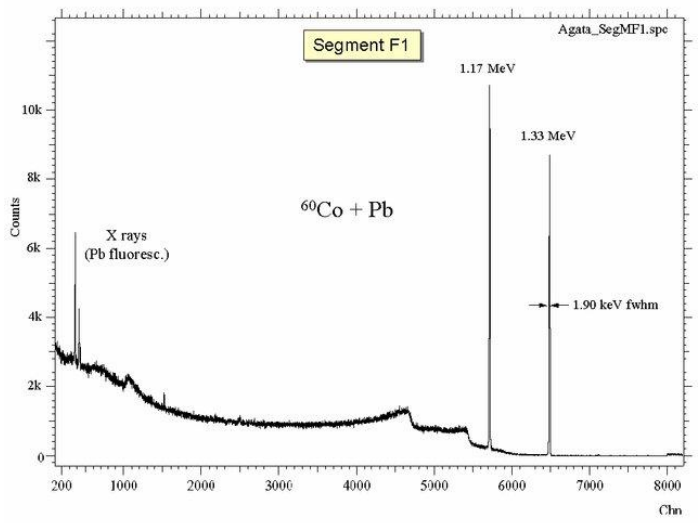

Fig. 1.3. AGATA calibration: Co60 β-decay radioactive source measured Spectra, with the 1.17 MeV gamma emitted in the de-excitation of the state 4+ to 2+ and 1.33 MeV emitted in the de-excitation of the state 2+ to 0+ of Ni60. ©2004 IEEE.[7]

In order to extract this structural data and other possible information related to the excited level in the state of the nucleus, a proper detector is required. Furthermore, not only emission following radioactive decay of the nucleus, but also the emission of gamma-radiation by the products of a nuclear reaction or following excitation of a nuclear beam colliding to a proper target could give even more information about the nuclear structure. The development of detectors has been evolving in the last 50 years towards better energy resolution and analysis capabilities, as the ability to produce new reactions with the use of heavy-ion and radioactive-ion beam accelerator facilities, to fulfil a wide spectrum of nuclear states to study.

1.1.2 Gamma radiation Interaction with matter

To understand how to extract the maximum possible amount of information from the gamma rays emitted in an experiment, the knowledge of the interaction of gamma-rays with matter is of paramount importance. It is relevant not only to evaluate the detected radiation of interest, but also to recognize the unwanted sources of radiation that could degrade our measurements.

A photon of high energy which approaches matter, releases energy through three possible interactions. It could be fully absorbed by the atom and this will free an electron through Photoelectric Absorption, it can collide to an electron and share its energy in a Compton Scattering process, or, providing it has enough energy, create a positron electron pair in a Pair Production event. The probability of each one of these interactions to occur depends on the energy of the gamma-ray but also on the atomic number of the material the photon is interacting with. Let's describe briefly these three mechanisms.

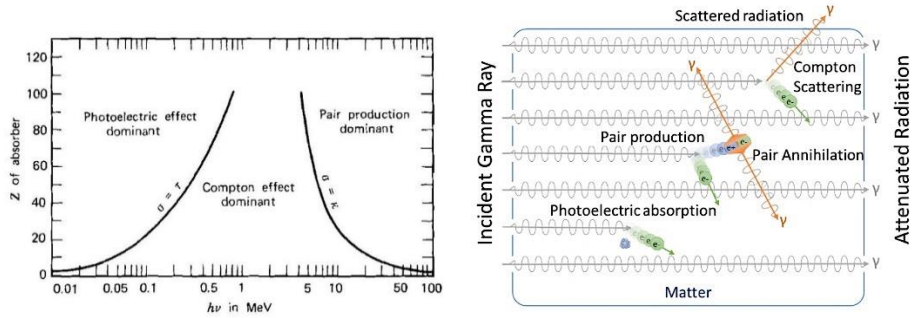

Fig. 1.4. ***Left:*** *Attenuation coefficients for gamma ray in relation with atomic number Z of absorber material.* ***Right:*** *Image representing the different interactions of gamma ray with matter.*

Photoelectric Absorption: The photoelectric effect is dominant at low-energies of the gamma spectrum, and the energy is related to the incoming photon energy and the electron binding energy. The electron is ejected with the remaining kinetic energy from the unbind one. This secondary electron will release its energy by electromagnetic interaction with the medium.

Compton Scattering: This effect is dominant in the mid-energy range of the gamma spectrum (1-few MeV). The gamma ray transfers part of its energy to an electron as kinetic energy and a new photon with the difference of energies is generated.

Pair Production: the pair production effect is dominant at high energy levels of the gamma spectrum (>10MeV). The photons with energies above the mass of two electrons, and in presence of the nucleus electric field, can transform into a pair of electron and positron. The energy above the 1022 KeV, required for the pair production, is directly translated into their kinetic energy.

In Fig. 1.4 the interaction areas are depicted and from them we can understand their influence in our spectra. The low energy area has a decreasing Photoelectric Absorption, on the central part the Compton is the main mechanism and for the highest energies the pair production is dominant.

1.1.3 Detectors for gamma-ray detection in Nuclear Science

The detectors in Nuclear Science profit from the properties of the interaction of the radiation with matter and sets-up specific conditions in an enclosed environment in order to generate a readable signal proportional to the energy of the incoming radiation. The detection is achieved in a vast amount of manners, depending of the kind of event or radiation, the sources and the energy range under study. Also different kind of detection systems can provide different information, from just decay rates to energies, position of the interaction or even characterization of the radiation received.

In the present section I will mainly concentrate in the detectors used for the detection of gamma radiation.

One of the early developed detectors was based on the effects of charged particles crossing a gas. The charged particles can be the entering radiation into the detector or can be produced within the detector material by, for example, an interacting gamma-ray.

This gas is ionized along the track of the particle and this ionization is collected thanks to a charged field. Depending on the charge collecting method, several types of detector have been developed. An Ionization Chamber collects charge through the electrodes generating the electromagnetic field in the gas. A second method is the proportional counter based on the fact that increasing the field in the gas generates a multiplication avalanche effect that increases the reaction effect compared to a single track. Another type of ionization chamber is the Geiger-Mueller Counter. In this case, higher electric fields are applied and a huge avalanche is triggered in the gas at each particle crossing. However, this method is only able to retrieve a value corresponding to the number of interactions but not to the energy of the particle due to the avalanche mechanism.

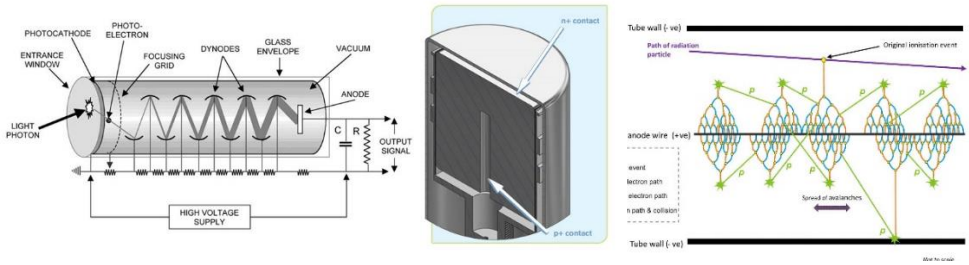

Fig. 1.5. ***Left****: Scintillator and PMT diagram*[8]. *Center: Example diagram of a Camberra SEGe Coaxial Ge Detector.* ***Right****: Geiger Muller Counter diagram*[9].

Another traditional technique to obtain information about the energy of a particle is the scintillation effect. The main function of scintillation materials is to transform the energy deposited by the radiation into detectable light. This light is collected and converted into electronic signals using photomultiplier tubes or photodiodes. The photomultiplier tubes generate electrons in a photocathode when photons hit it and the electrons colliding to the dynodes, placed sequentially increasing the positive potential, produce a multiplying cascade of electrons along the photomultiplier structure, generating a proportional current measured at the anode. In the case of the photodiode, the photons affect a semiconductor material taking advantage of the junction light absorption effect. As the output signal is proportional to the received radiation energy, scintillators are widely used in spectra analysis. The main disadvantage of scintillators materials for spectroscopy applications, as for example sodium iodide, is their poor energy resolution.

The last technology that allows to detect gamma radiation is based on semiconductor diodes. When a semiconductor P-I-N doped structure (p+ doped-intrinsic-n+ doped) is reverse polarized, a fixed electromagnetic field is generated in the material. Any photon reaching the semiconductor will transfer its energy to electrons and positrons using one of the interactions described before. If the secondary electrons and positrons have enough energy, they will create electron-hole pairs in the intrinsic zone and the field forces them to move to the P and N electrodes. The bigger the energy the larger the amount of pairs created, being the charge proportional to the gamma ray energy. Due to the larger atomic number, Germanium is preferred to Silicon as semiconductor material.

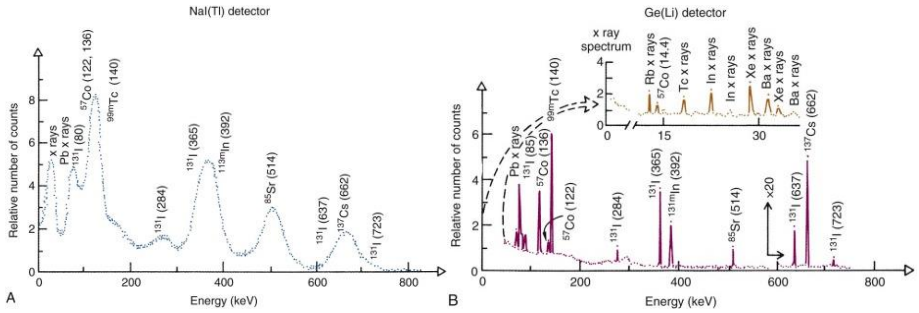

Fig. 1.6. NaI(Tl) scintillator spectra (A) and Ge(Li) Semiconductor spectra (B) comparison. Greater energy resolutions on the gamma ray peaks are observed on semiconductor device.[10]

The big disadvantage of Ge semiconductor detectors is related to the working temperature. At room temperature a noticeable amount of background noise is present due to thermal induced electrical currents. This problem is solved lowering the detectors temperature in cryostats, normally at liquid nitrogen temperatures (77K or -196 °C) [11].

Among the benefits of using Ge semiconductors, we have the size required for the same amount of retrieved energy because of their higher densities and their excellent energy resolution, due to the high amount of charge carriers (electron-hole pair) per incoming energy particle compared to gas or scintillators [12]. Approximately one ionization is produced per 3 to 5 eV of radiation in semiconductors (depending on the material) and about ~30eV for gases [10]. This leads to better energy resolutions and therefore higher sensitivity, still an order of magnitude better than scintillators. Among the semiconductor detectors, the excellent energy resolution of germanium (better than 0.2 % at 1.333 MeV) makes it the best gamma detector for high resolution gamma-ray spectroscopy studies.

1.1.4 High-Resolution Gamma-Ray spectroscopy and Germanium detectors

In the field of the Gamma-Ray spectroscopy the aim of the detector is to have an accurate map of the number of photons according to their energy. There are three main parameters that contribute to the detection sensitivity namely the detector efficiency, the peak-to-total ratio (equivalent to the signal-to-noise ratio) and the energy resolution.

The detector efficiency is related to the properties of the detectors used. Not all photons from an event interact in the active sensor material, and not all the photons interacting inside the active material are depositing their full energy. The first component of the efficiency is related to geometrical characteristics of the detector, in particular the solid angle Ω from the gamma source subtended by the detector. The second component of the efficiency, the intrinsic one, is independent of the source to detector distance and it is related to the detector depth, the technology and active material [5]. The total efficiency ε can be measured as the number of events recorded divided by the number of radiation particles emitted by the source. The intrinsic efficiency is defined as the number of pulses recorded divided by number of radiation particles incident on detector.

The second important parameter on spectroscopy is the Peak-to-Total (P/T) ratio, that is, the relation between the energy of the peaks in the active material and the total energy. This is a useful parameter to have an objective and independent measure and comparison of the efficiency regardless the laboratory and event conditions. It can be extracted through a measurement of the high-end peak of the differential pulse height spectrum, where all the information of high peak energies is stored [5].

The last element to take into account is energy resolution, i.e. the capability of detectors to define a single energy value peak. In the spectra, each monoenergetic pulse will be represented as a Gaussian peak added to the background and the rest of the spectrum. This pulse width at half height or FWHM will define the energy resolution of the detector and its standard deviation (σ) is extracted from it. In the energy resolution is where semiconductor detectors, and Germanium in particular, have their best benefits.

In germanium detectors PIN structures, as in Silicon detectors, there is a limit on the volume of active material detector because of the impurities. These impurities create "electron traps" and capture electrons released from ionization. To limit this effect, the thickness of the semiconductor must be restrained to values below 1cm. There are two known solutions to overcome this limitation. The first one is to induce new forced impurities to generate enough electrons to be captured, compensating this way the effect of the intrinsic impurities. A second solution, only available after several years of technology improvements, is to refine the material to purify enough the semiconductor.

The first solution, developed in the early 60's, is carried out doping the Si or Ge with lithium by controlled diffusion [13], the resulting detectors being named as Si(Li) and Ge(Li) detectors. The main issue of the Lithium doped detectors is that, at room temperature, the diffusion of Li ions destroys the delicate compensation profile of the impurities, so the storage of the detectors has to be at low temperatures [14] .

The second solution was first possible to manufacture in the early 70's and only for the Ge and this detector are called HPGe detectors (High Purity Germanium detectors) [15][16]. It's an expensive process and allows to grow up detectors of about 10-12 cm diameter [9]. Unlike the Ge(Li), the HPGe can be stored at room temperature, they have a faster and versatile production and less neutron-induced radiation damage [14].

The already mentioned ionization per eV takes the main part in this better resolution. Regarding the difference between Germanium and Silicon, Germanium is usually preferred due to the higher densities (Si: 2.33 g/cm^3; Ge: 5.32 g/cm^3), higher electron mobility (Si: $2.1 \cdot 10^4$ $cm^2V^{-1}s^{-1}$, Ge: $3.6 \cdot 10^4$ $cm^2V^{-1}s^{-1}$) and hole mobility (Si: $1.1 \cdot 10^4$ $cm^2V^{-1}s^{-1}$, Ge: $4.2 \cdot 10^4$ $cm^2V^{-1}s^{-1}$), and lower energy per electron-hole due to the smaller band gap (Si: 3.76 eV, Ge: 2.96 eV) [17] resulting in a larger amount of charge per incident gamma ray. Additionally, the interaction cross sections for the relevant mechanisms, in our energy range of interest, depend on the atomic number (Z) of the detector material (photoelectric as $Z^{4.5}$, Compton as Z, Pair Production as Z^2) so the larger atomic number of Ge (Z=32) compared with Si (Z=14) is relevant for the intrinsic efficiency of the detectors.

1.1.5 In-Beam Spectroscopy

The In-Beam Spectroscopy is the technique to obtain the gamma emission energy spectra for a nucleus produced or excited in a reaction resulting from colliding nuclei. An ion beam colliding to a target is the main instrument to obtain excited states of the nucleus far from stability or with high spin states. The necessity to study nuclei further from stability has triggered the construction of Radioactive Ion Beam facilities, where the ion beam impinging into the target is composed of unstable nuclei.

A discussion of the characteristic of the reactions in necessary to understand the capabilities of the technique.

The atomic nucleus has tiny dimensions, in the order of several fm of radius. Therefore, most of the beam particles miss the target, which implies a small cross-section for the impact, in the other of 1 barn (10^{-28} m^{-2}). There are two main parameters that will define the possible outcome of the collision: the impact parameter b, as the distance between the two colliding nucleons centres in relation to the collision trajectory, and the kinetic energy of the incident beam of ionized atoms.

If the impact parameter b is too large in relation to the atomic radius, the two nucleus have a kinetic energy transfer mainly through the electromagnetic interaction, i.e. an elastic scattering with no nuclear excitation or nucleon exchange.

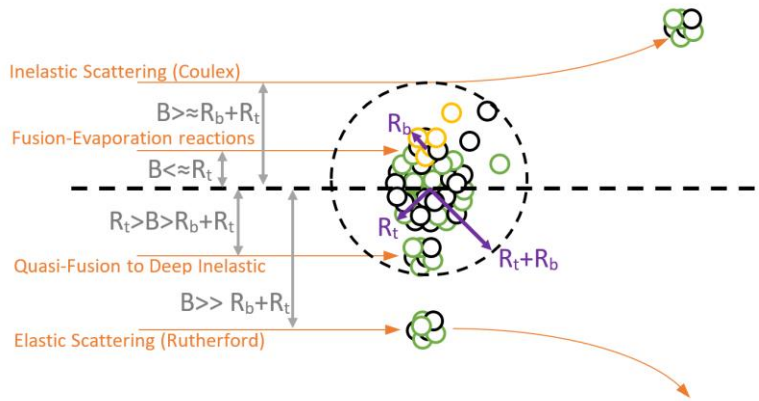

Fig. 1.7. A conceptual view of the possible results related to impact parameter B between beam and target nuclei.

With an impact parameter b approaching the sum of nuclear radius, reactions of interest for the in-beam spectroscopy start to happen. With low incident beam kinetic energy, and in case the parameter b is close enough to the sum of target and beam nuclear radius, there is an excitation without matter exchange in the collision, i.e. an inelastic scattering. The inelastic scattering can happen through the Coulomb interaction (Coulomb excitation), or, at smaller impact parameter it plays a role in the inelastic excitation. With slightly higher energies and smaller impact parameters b, transfer of nucleons is on-set, starting from the quasi-elastic, where few nucleons are transferred, until the Deep Inelastic regime is reached. In this transfer reactions the nucleons are moved between the two nuclei, resulting in new excited elements near both original A and N configurations of the projectile and target. [18]

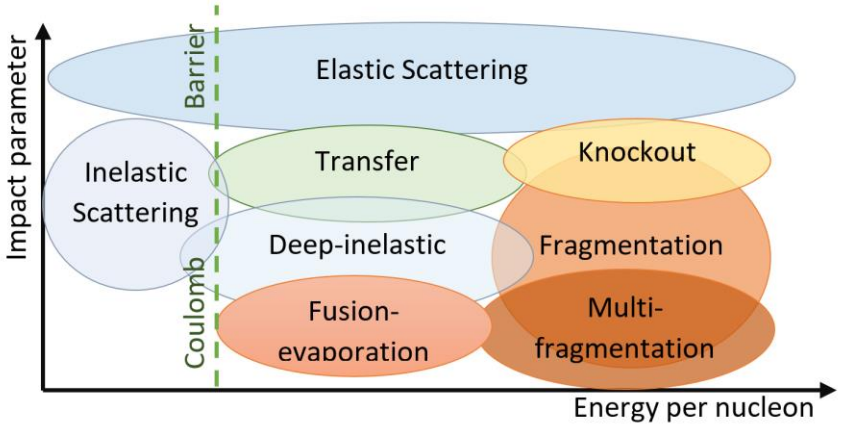

Fig. 1.8. Representation of possible reactions in relation to energy beam and impact parameter.

At smaller impact parameters b, the nuclear fusion becomes possible, starting with the quasi fusion reactions to smaller impact parameters with Fusion-Evaporation reactions. In the case of fusion-evaporation reactions, both nucleons merge combining their masses, losing the memory of the original fused nuclei and some nucleons are usually evaporated in the process, since the compound nucleus is created at relatively high excitation energy. [19]

The fusion-evaporation reaction is used to obtain excited high spins in neutron deficient nuclei of interest. To produce the fusion, the kinetic energy of the beam must overcome the Coulomb repulsion. As mentioned before, after the fusion, few nucleons are emitted by evaporation. Due to the availability of stable projectiles and targets for the nuclear reactions, in general, after evaporation, a neutron deficient metastable excited nucleus is created after 10^{-20} seconds.

In general, the evaporation of neutrons and charged particle is followed by the emission of gamma-rays de-exciting the entry states of the reaction products through the complex excited level scheme. The de-excitation sequence reaches finally the so-called Yrast line, that represent the lower state energy level for each angular momentum, thus the de-excitation follows the Yrast line until the nucleus reaches the ground state. In limited occasions fusion evaporation or quasi-fusion can be used to study neutron-rich nuclei close to the stability line. In this case the detection of the evaporated or out-coming light charged particles is fundamental to select the reaction channel.

To study neutron rich nuclei, the multi-nucleon transfers and deep inelastic reactions can be used. Spectroscopy techniques using these reactions profit from the nucleon transference and the equilibration of the N:Z ratio happening on the reaction. Therefore, light to medium mass nuclei beam, against very heavy stable targets, gain neutrons after such reactions.

Reactions with sizeable higher kinetic energy beams than the ones studied before are dominated by fragmentation. With beam energies above 30 MeV/A (energy per nucleon) colliding to a target results in a loss of a number of protons and neutrons, with almost all momentum conservation on the beam nuclei. A whole family of possible nuclei are produced with different yields. There is a particular case of fragmentation when the b parameter is in the order of the nuclei radius called knockout, capable of stripping only one nucleon from the nucleus of interest.

Reactions with high energy beams combined with Fragment separator facilities are used in relativistic Radioactive ion beam facilities to obtain the secondary radioactive beam. In such facilities the in-flight Fragment Separator is used to select the desired nucleus and use it on a secondary reaction on a target placed at the separator focal plane position. The other use of projectile fragmentation is to directly study long lived excited states, with detectors at the end of the separator. These type of Radioactive Ion Beam facilities are called In-Flight facilities.[20]

Another reaction at relativistic energies, used in in-flight Radioactive Ion facilities, is the induced projectile fission. It is performed with heavy beams, for example ^{238}U, impinging, in general, on light target, causing the fission of the heavy nuclei. The resulting fragments beams are mass separated and selected, like in the fragmentation production method, to be used for secondary reactions. The secondary reactions in In-Flight facilities are exclusively in inverse kinematics and with large β (~ 50%), like relativistic coulomb excitation, knock-out reactions, fragmentation, etc.

The fragmentation is not the only production method used in the facilities for the production of radioactive ion beams, the Isotope Separation On-Line (ISOL) method is as well widely used. The ISOL method consists in generating the radioactive ions from whatever reaction, in general at lower energies, to have them reaccelerated after selection using magnetic separators or Laser Ionization techniques.

The drawback of the ISOL technique is that the time necessary for the ion selection, charge breading and acceleration, places a lower limit on the lifetimes of the radioactive nuclei to be used. The ISOL facilities provides beams to be used in direct and inverse kinematics reactions, with β ~ 10%, as coulomb excitation, transfer reactions, deep inelastic, etc.

1.1.6 Gamma Ray Detector Arrays and Tracking

The experimental investigation of the nuclear structure, using gamma-ray spectroscopy techniques, requires as a first step to obtain a nucleus in an excited state, such that in the de-excitation process electromagnetic radiation is emitted. This can be realized in two ways: first using nuclear reactions that obtain a reaction product in an excited state or excites the beam o target nuclei. The second option is to obtain an unstable nucleus in the ground or isomeric state that will later decay to excited states in the daughter nucleus.

The selection of the experimental set-up and the laboratory to perform the experiment is strongly dependent on the kind of measurement and the nucleus to be investigated.

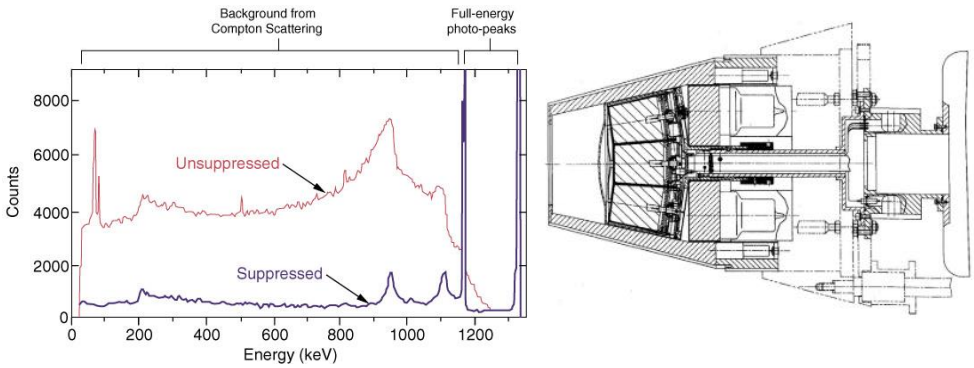

Fig. 1.9. ***Left****: image representing the effect of suppression on Germanium arrays.*[21]. ***Right****: Euroball cluster detector.*

State-of-the-art nuclear structure studies are dealing with nuclei very far from the stability line (many of them of relevance for the nucleosynthesis processes) or with very exotic states in nuclei closer to the stability, that might reveal new symmetries in the effective nuclear Hamiltonian. Gamma-ray spectroscopy in such cases requires advanced instrumentation as the Ge Detector Arrays, frequently coupled with complementary instrumentation in order to reveal the reactions channel, to track the trajectories of the moving nuclei or even to help performing measurements that can't be done only with the Ge detectors.

The second important aspect about these measurements is the laboratory, able to produce the nucleus in the state of interest. Presently the most interesting laboratories are the ones providing accelerated high-intensity beams of stable ions as well as Radioactive ion-beams (RIBs) produced with the ISOL or in-flight techniques. Europe provides, or will provide, some of these world-class laboratories as the in-flight facility FAIR (GSI, Darmstadt, Germany) [19] providing RIBs at relativistic energies, the ISOL Laboratories HIE-ISOLDE (CERN, Geneva, Switzerland) [20], SPIRAL2 (GANIL, Caen, France) [21], SPES (INFN-LNL, Legnaro, Italy) [22], that are providing or will provide RIBs beams at the Coulomb barrier energies or slightly above. There are other such facilities all over the world: FRIB (NSCL/MSU, Michigan, US) [23], ISAC-II (TRIUMF, Vancouver, Canada) [24] and RIBF (RIKEN/Nishina Center, Saitama, Japan) [25], etc.

In this section we will discuss the HPGe detector arrays, their history and finally the development of the advanced Tracking arrays of HPGe detectors.

Regarding the energy resolution for the gamma-ray measurements, we have already discussed that the best capabilities are on the HPGe detectors, due to near 0,2 % energy resolutions achieved at around 1 MeV gamma-ray energy. Therefore, the next parameters to optimize are the efficiency and the Peak-to-Total ratio (P/T). For this purpose, the germanium arrays were developed.

First, the large angular coverage by including in a set-up a large number of HPGe detectors, results in a larger efficiency. Moreover, the Compton scattering highly dominates the energy region of interest in Ge detectors and many of the scattered gamma ray scape from germanium active detector volume, with a low peak-to-Compton ratio. The first solution is to grow larger Ge crystal with HPGe to include the scattered photons, but this is limited by the semiconductor growing technologies, and the second one is to incorporate the Compton suppression shield to the bare Ge detector. With such a shield, initially build of NaI(Tl) scintillator, the scattered gamma ray from Ge are detected on the surrounding a NaI(Tl) scintillators. In the early small volume Ge detectors, improvements of a factor of 10 where achieved on the P/T values for Compton. [14]

The first gamma array with suppression was built in 1980 and it was called TESSA. The detector achieved a P/T of 60% with 5 Ge(Li) detectors and NaI detectors tubes for suppression. The amount of detectors in the array was strongly limited because of the solid angle used by the Compton suppression shield. Later, the HERA spectrometer was built with major improvements including the use of HPGe as an advance for germanium detector and BGO ($Bi_4Ge_3O_{12}$) scintillator as improvement for shielding. This detector was built with 21 HPGe + 44 BGO detectors deployed around the reaction target and reaching a 1.5% full-energy absorption (peak) efficiency for 1 MeV gamma-rays. After this achievement, several arrays were built with the same techniques with around 12-40 Ge detectors and reaching about 3% of peak efficiency at 1 MeV gamma-ray energy.

After the explosion in the number of detectors, the scientific community, by the end of 1980s, proposed to build a full sphere detector with 4π solid angle covering. This resulted in the construction of EUROBALL [22] detector in Europe and GAMMASPHERE detector [23] in USA, thanks to the work of big collaborations with multiple institutes involved. The GAMMASPHERE was developed in only one phase and was built with 110 hexagon detectors with BGO shielding covering 95% of 4π. Nevertheless, the HPGe peak efficiency of the GAMMASPHERE was 10% and the P/T was about 50%.

The European project had a several step approach, GASP (Legnaro, Italy) and EUROGAM II (Dalesbury, UK + France) with 40 Ge covering 80% of 4π resulting in 3% full-energy efficiency and 54 Ge resulting in a peak efficiency of 3% or 5.8% in its two configurations. These detectors were the preliminaries to EUROBALL, introducing its encapsulated cluster detector, a 7 packed germanium detectors in the same cryostat merged in a hexagonal form to fit the sphere (see Fig. 1.9). The EUROBALL detector was built in steps upgrading EUROGAM II to EUROBALL III and later to EUROBAL IV. The final configuration had similar capabilities as GAMMASPHERE with 253 detectors and a peak efficiency between 7 and 10%, depending on the experimental conditions.

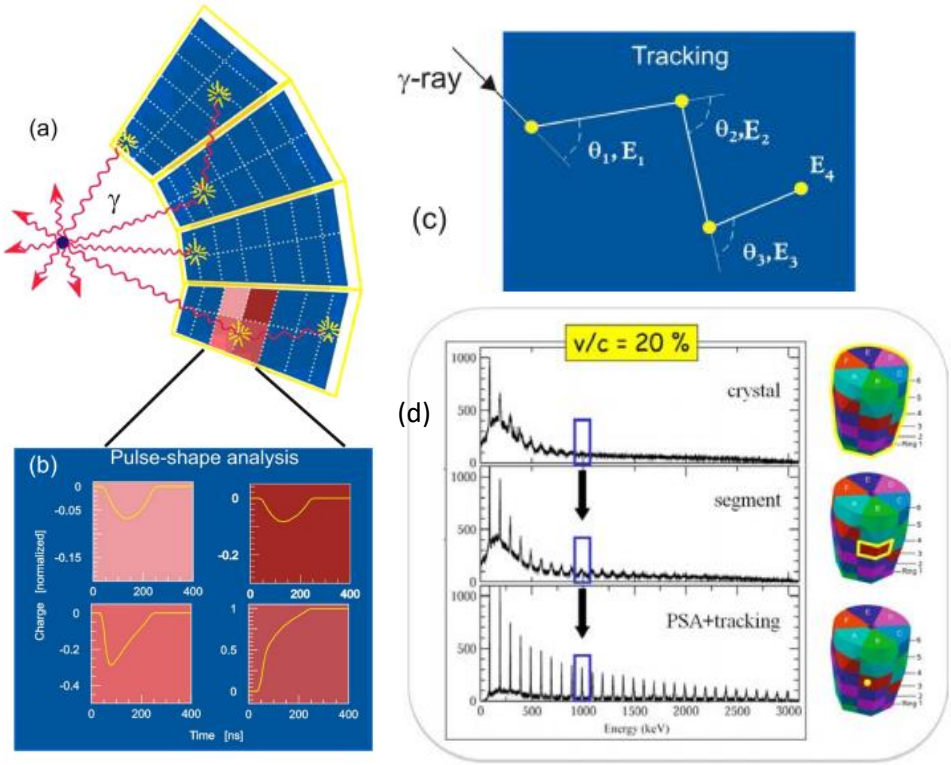

Fig. 1.10. a: Example of a gamma ray impact on several segmented sectors of HPGe. b: representation of the signals on each of the segments. c: gamma tray path for tracking techniques. [21] *d: AGATA P/T signal demonstration for each part of the tracking algorithm.*

Nevertheless, EUROBALL and GAMMASPHERE were not the end of the journey and a new idea came up and was developed at the turn of the millennium. The Compton suppression technique provided excellent peak-to-total (signal to background) ratios but reduced the solid angle covered by the Ge detectors, thus limiting the sensitivity of the arrays.

An European Commission financed initiative, the TMR network 'Development of gamma-ray tracking detectors' [24], taking place during the period 1996 to 2001 encouraged the development of the highly segmented position sensitive Germanium detector technology. This technique applies the so-called Pulse Shape Analysis (PSA) that uses the shape of the charged and induced (in neighbouring segments) signal, in highly segmented Ge contacts, to locate the position where the gamma deposited its energy [25].

The inception of the Ge position sensitive detectors technology has opened the possibility to build arrays of detectors based on the γ-ray tracking technique [26], providing an unprecedented level of sensitivity and efficiency.

Fig. 1.10 represents the path of the photons over a position sensitive Ge detector and the corresponding signals from the segments. Only two arrays with such technology are being built in the world, the European implementation of the tracking array is realized in the AGATA project. The second one, also under construction in the U.S.A., is the GRETA array [27].

1.1.7 The Gamma-ray Tracking Concept

The gamma-ray tracking process requires position sensitive semiconductor Germanium detectors. The technology of the position sensitivity, that requires segmented contacts in the detector and was developed in the mid 90's, is based on the early works on the E. Gatti, et al. [28] on the signal evaluation of multi-electrode detectors. This position sensitivity is achieved applying the Pulse Shape Analysis technique to the charge as well as to the induced signals in the segmented contacts of the Ge detector.

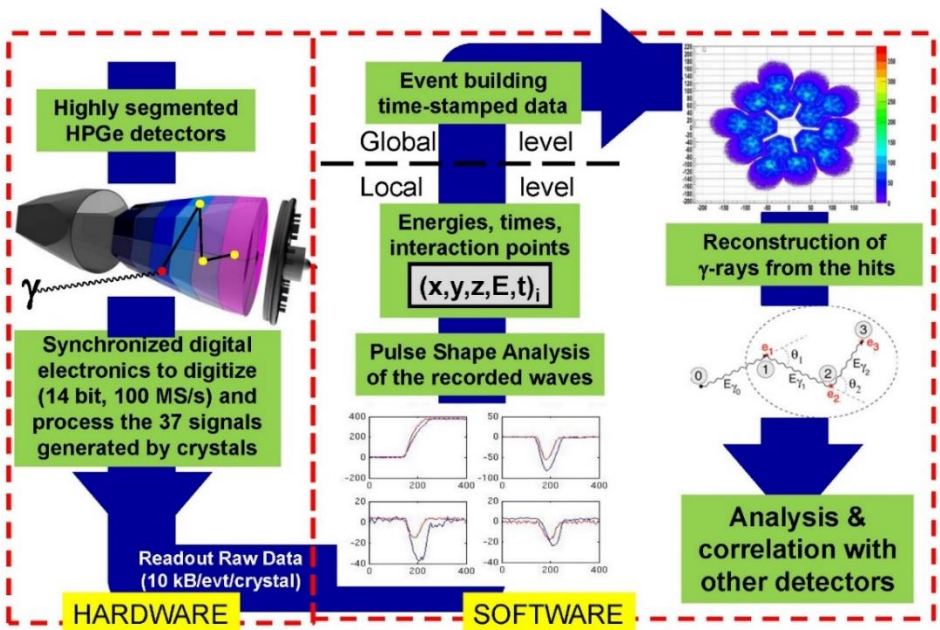

Fig. 1.11. Scheme showing the gamma-ray tracking concept differentiating between the hardware and software parts.

The position resolution depends strongly on the capability to understand the charge and image (induced) pulses for the detectors [29]. The complex Pulse Shape Analysis that is required can only be done using the sampled pulses of the detector, therefore the digital sampling electronics is playing a major role in the design and construction of such Tracking arrays. The digital hardware and software paths are depicted in Fig. 1.11.

As mentioned before, the digital sampling electronics is a fundamental part of the tracking arrays. Nevertheless, the signal processing starts with the low-noise spectroscopic charge amplifier. On Chapter 2 a more advanced overview of electronics for tracking arrays is explained in the context of AGATA spectrometer.

1.1.8 AGATA The Advanced Gamma Tracking Array

The Advanced Gamma Tracking Array is a spectrometer array developed by a huge European collaboration from 12 countries and more than 40 institutions and Universities [30]. The detector is an array of position sensitive HPGe crystals. Each piece is segmented in 6 layers in depth and 6 pieces per depth layer (for a total of 36 segments). To increase the overall geometrical efficiency, it is designed as 180 detectors over a whole sphere covering 4π srrad of solid angle. Several studies were done in the initial phase in order to optimize the geometry using the technique of tiling the sphere Fig. 1.12 [31].

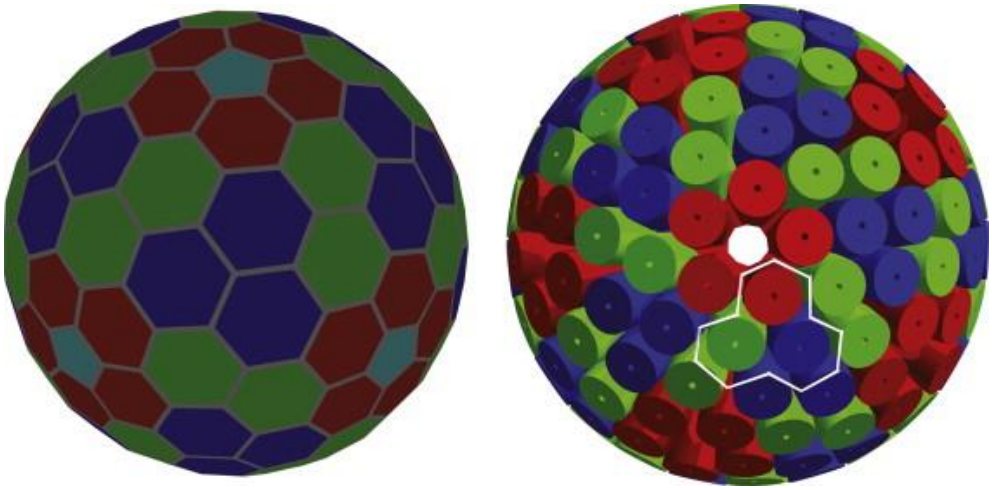

Fig. 1.12. The AGATA 180 detectors tiling of the Sphere and construction of the triple cluster. [32]

The final form is composed of a series of triple clusters and of asymmetric detectors in a particular geometry. This geometry maximizes the solid angle and lets only one hole for the accelerator beam pipe. Each triple cluster is built with a cryostat for cooling and preamplifiers placed between the cold and warm part [33], an example can be found in Fig. 1.13. The AGATA detector is designed to be built progressively in several phases. For the present one, Phase 1, the agreement in the collaboration was to build up to 4/3π or, equivalently, 60 encapsulated detectors (20 triplets) until 2020. Phase 2, with the MoU under preparation, is aiming to complete the array.

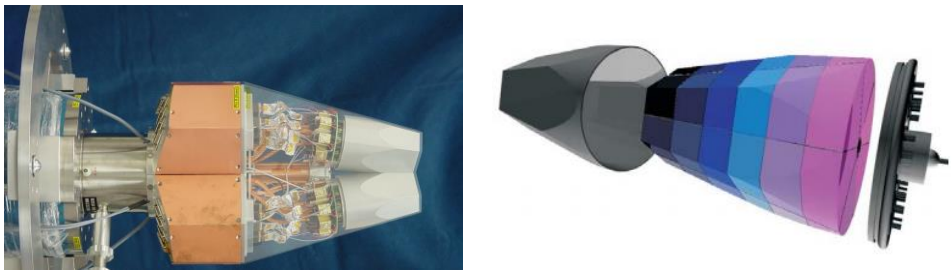

Fig. 1.13. Left: The AGATA detector cryostat. ***Right****: The AGATA detector segment distribution.*[34]

AGATA is being built with the expectation, obtained with Monte-Carlo techniques and simulating the PSA and Tracking processing, to gain about 2 orders of magnitude in sensitivity with respect to the previous European array EUROBALL (see Fig. 1.14).

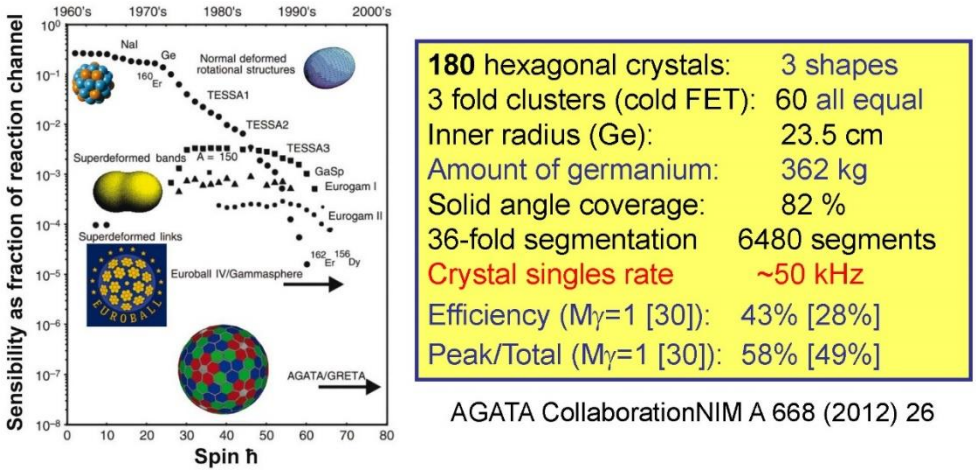

Fig. 1.14. AGATA sensitivity compared with previous arrays and AGATA design specifications.

The development is carried out taking into account the possibility to move the array to several laboratories around Europe to take advantage of the different beams and experimental possibilities in high-intensity stable beams and RIB facilities. For this reason, the newest technologies are used to integrate as much as possible and shrink the detector size on all of its areas: electronic, power supplies, processing, etc.

Since the collaboration started the construction of AGATA, the existing detectors have been used to perform experimental campaigns with smaller sub-arrays. On its last experimental campaign in 2019 at GANIL (Caen, France) AGATA used up to 45 detectors and until now it has been working together with many ancillary detectors such as NEDA, NWALL, DIAMANT, MuGAST and VAMOS [35] (see Fig. 1.15). Before going to GANIL, AGATA was placed in GSI (Darmstadt, Germany) [36] coupled to FRS in 2012-2014 and years before, the first place where it was assembled and tested was LNL (Legnaro, Italy) [37] in 2010.

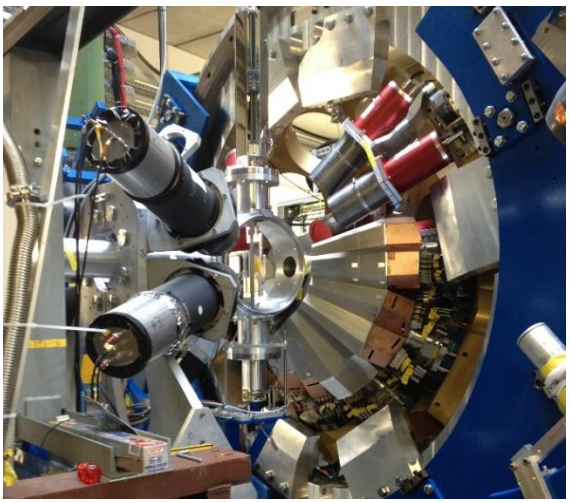

Fig. 1.15. AGATA with 35 detectors coupled to NEDA, DIAMANT and NWall [30]

Until now, the AGATA spectrometer and its collaboration have produced more than 50 scientific publications in nuclear science and related areas and more than 80 publications in technical areas. Nevertheless, the detector is not already completed, and the next phase of development is creating expectations for the opening of possibilities with such instrument.

The final approach to 4π needs great efforts in the technical side due to the amount of channels to be processed and computing capability required for PSA, tracking and global synchronization. This is leading the collaboration to its Phase 2 of development relying in the new developments on the edge of technology.

1.2 Technology on the Edge

The electronic technology advances and the Nuclear Science take advantage of new elements to increase performance maximizing the scientific outcome. On the digital age, every information read from Nature has to be digitalized and codified and the main objective required by modern nuclear instrumentation is to acquire the maximum amount of information of an experiment with the current technology.

The detection of a full event demands high speed data and bandwidth throughputs before, or even after, the triggering system data reduction. The other relevant element for communication technology is the number of those high speed channels for detector arrays, even more demanding in the case of position sensitive highly-segmented detectors arrays.

In any detection system an information of paramount importance is related to the time in which the detection occurs, so a timing system is required to synchronize all the elements of the detector array.

Another area where technology improves the performance is on the processing capabilities and system control. Such a complex detector with a high number of electronics channels and several steps of parallel high speed processing, require an automation and control system able to cope with all the actions required to configure, start and stop the detection process and control each part from a user friendly point of view.

1.2.1 High speed links.

On the field of high speed electronics, the technology has evolved into multi-Gbps links in the last decades [38]. The Ethernet 40G-100G [39] and Interlaken 400Gbps [40] became a standard in use in the computing and communications industries. Each of the single links of these high speed lines work at speeds between 10 and 40 Gbps. In order to

reach these data speed rates over long distances, optical lines and transceivers are used, moreover, the techniques of high speed PCB manufacture procedures and components for integrated circuits construction are fundamental.[41]

Optical Lines

The optical lines are one of the main development area in the communication industry. There are several possibilities to transmit data through a controlled index wave guideline, as well as several methods to generate the optical light signal and retrieving it.[42]

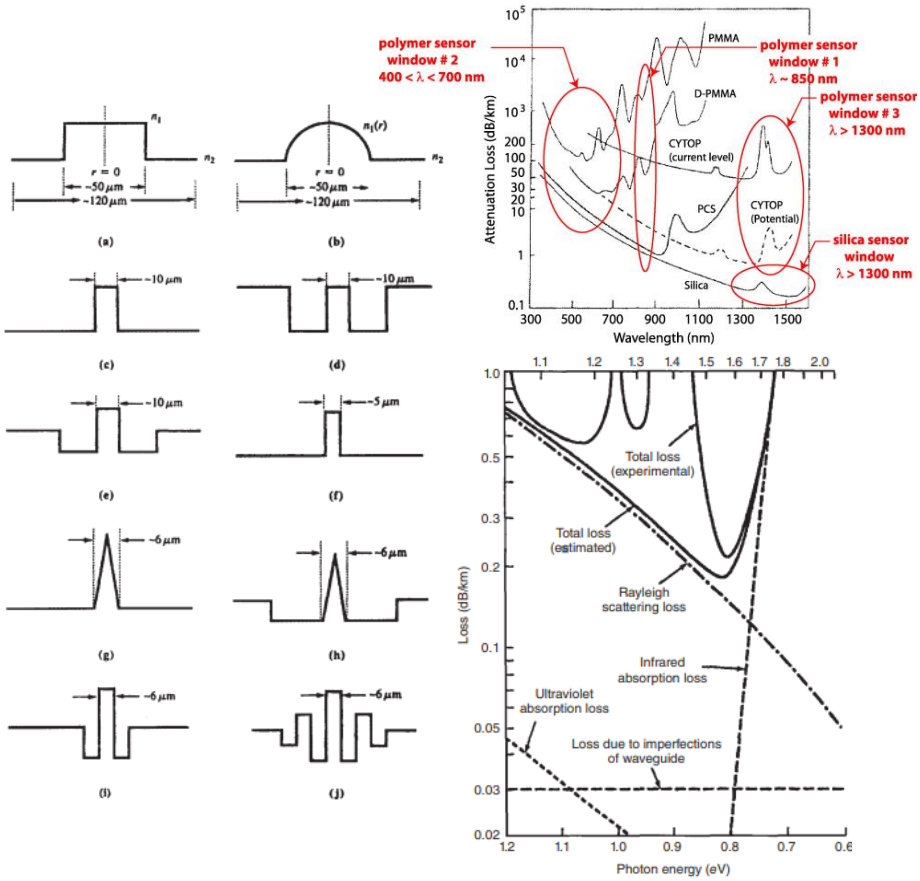

Fig. 1.16. ***Left****: Refractive index profiles of (a) step-index multimode fibers, (b) graded-index multimode fibers, (c) match-cladding single-mode fibers, (d, e) depressed-cladding single-mode fibers, (f–h) dispersion-shifted fibers, and (i, j) dispersion-flattened fibers.*[42] ***Right Up:*** *Optical line attenuations loss comparison on spectra between polymer and silica.*[43] ***Right Down:*** *Silica SiO2 loss in relation to Wavelength.*

Inside an optical transmission line signal can propagate in several conditions, or modes, which relate to its dimensions and refractive index profile. These electromagnetic modes are used to propagate information in form of light of a given wavelength. In the one hand, we can select only one mode and we set up a Single Mode Fiber (OS), with core diameter less than ten times the selected wavelength. In the other hand, if we select several modes we are on a Multi Mode Fiber (OM), and we are working with bigger diameters for the active core of the fibre. This characteristics are achieved modifying the refractive index profiles as is represented in Fig. 1.16.

A second element in optical fibres is the material for the fibre itself, with impact on signal attenuation, wavelength dispersion and limitations on the length of the fibres (See Fig. 1.16 right). Common materials used are fused silica (SiO2)[42], fluoride glass [44], phosphate glasses [45], or specific polymers [43].

The third interesting element of fibres as communication technology is integrating a bunch of fibres in a single cable. This is directly related to technology material, modes and industry capabilities. The technology of Multi-core fibers (MCF) allows to merge several active cores of controlled refraction index to implement multiple transmission lines on the same section of cable [46][47]. Once the core is manufactured, the rest of the material for the cable is filled with Polydimethyl siloxane, Silicon oils or Acrylates.

About the sensor at reception transceiver side, we normally expect a PIN photodiode optimized for the used wavelength. The most commonly used are silicon, germanium, InGaAsP[48] or GaAlAsSb. Nevertheless, other elements can be found as receptors like Avalanche Photodiodes [49], photodiode arrays, Schottky barrier photodiodes [50] or Metal-Semiconductor detectors (MSM) [51]. On the transmission side, the usual elements are LEDs, edge-emitting lasers diodes (EELD) and vertical cavity surface-emitting laser (VCSELs).

For the fiber interconnection, industries have set a series of standards. On the passive side of the optical line, the optical cables have a label to specify the mode and performance, as in OM1 to OM5 for multimode or OS1-2 for monomode. There is a wide variety of connectors for the physical connection of the optical line as depicted on Fig. 1.17.

On the active side of optical lines, the transceiver main standard widely used is Ethernet Small Form-factor Pluggable transceiver (SFP) and its evolutions SFP+ [52] or SFP28, a full-duplex line up to 10Gbit/s and 25Gbit/s, or the quad full-duplex version QSFP+ and QSFP28 up to 40Gbit/s and 100Gbit/s aggregated bandwidth respectively [53]. Manufacturers also develop their own connectors and standards as PPOD [54], MiniPod [55] and MicroPod from Broadcom Avago, SNAP12 modules, FireFly optical versions from Samtec [56] or the CXP [57] version of SFP, all of them with 12 optical lines.

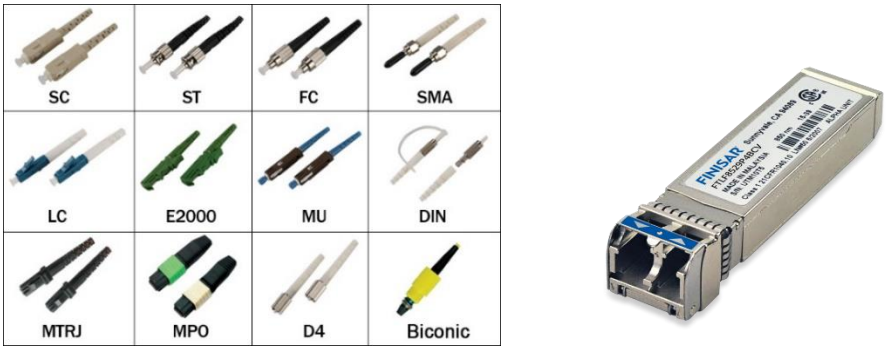

Fig. 1.17. ***Right****: types of optical mechanical connectors.* ***Left****: Example of an active transceiver part SFP+ connector from Finisar Corporation with a LC mechanical connector socket.*

High speed PCB.

The high speed communication technology and optical lines require from the electronic elements an appropriate response of the copper connections from the printed circuit boards (PCB) side. Common speeds nowadays for this systems could reach over 10-30Gbps in most critical cases, and the electronic integration increase requires less space and more connections for the same PCB area.

Many tools and techniques had been developed in the last years to cope with these requirements. There is a special need for high speed materials as Nelco [58], Rogers [59] or FR408 [60], usually designed for RF applications, with low loss tangent and low dielectric constant at 10GHz frequencies. These materials allow to ensure a controlled impedance for the differential lines in the designed PCB (see Fig. 1.18), in addition to proper design techniques as trace line matching, constant impedance matching, via optimization, return lines analysis, crosstalk corrections [61][62][63].

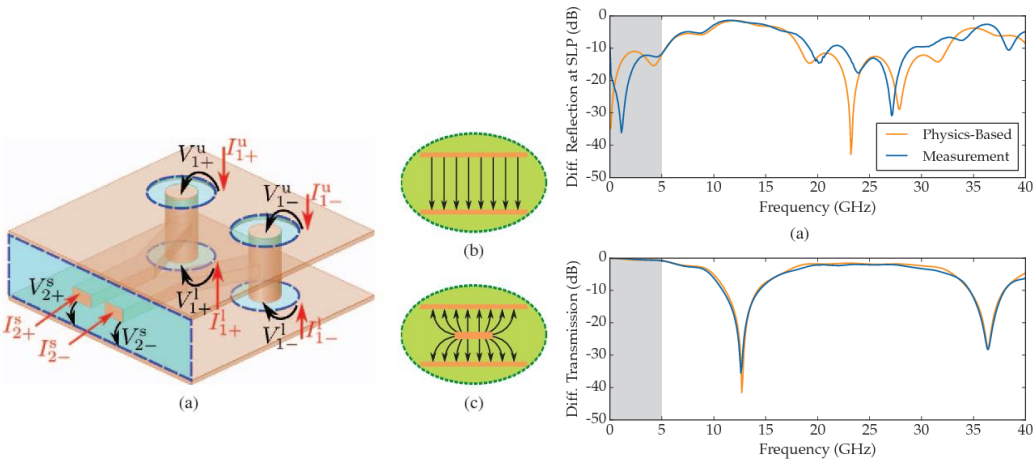

Fig. 1.18. Example of a differential strip line and the high speed transmission and reflexion analysis.[64]

On the integration side, industry has developed a new methodology to generate smaller PCBs interconnection called High Density Interconnect (HDI) [65]. With this technology it's possible to use laser vias down to 50µm, vias in pads and via pitch below 0.4 mm [66].

1.2.2 Instrumentation technology.

Reading signal data from a detector is not trivial since the signal has usually a low amplitude or can be a current measurement. In the last case, it has to be converted to a voltage signal with an RC element. So the first step reading the signal is to deliver and adapt it to the proper condition, amplification and shape for the next step in the electronic chain.

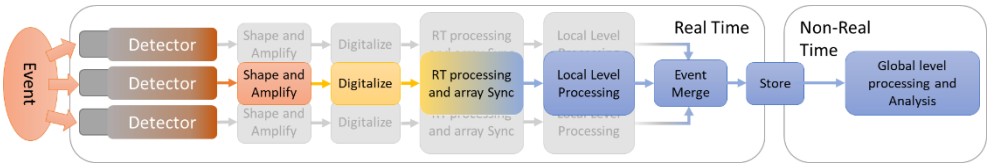

Fig. 1.19. Diagram of an Array detector instrumentation.

The world of storage, processing and communications nowadays is digital, so after a proper signal adaptation it has to be digitized.

The digitalized signal is sent to the real time processing and the triggering trees to verify whether the data is valid or not. This is a critical point due to fact that the full array and different complementary detectors have to contain the elements that make valid the event for our purpose or, at least, should be synchronized to identify the data that are of the same event. Once the data is valid, it's digitally sent to the storage systems for further processing and extraction of physical information. An example of an array detector instrumentation diagram can be found on Fig. 1.19.

1.2.3 Parallel processing and FPGA.

The amount of channels to process in real time on nuclear spectrometry before sending the signals and spectra for processing requires a very high degree of parallelization. In the field of real time processing, one can perform the calculations required with a relative fast sequential processor in such a way that the time to process is less than the real time scale timing unit. Nevertheless, when the number of channels in parallel to process increases, we have to move to a faster processor or increase the number of processors. The speed limits of electronic devices processing cycles are due to the power and thermal requirements so the real solution is parallel computing [67].

The real time parallel computing can be done in any of the big devices for computing as multicore processors or DSPs, parallel devices or Graphic Processing Units (GPU), Field Programmable Gate Arrays (FPGA) or Application-Specific Integrated Circuit. For our application, the multicore processor is excluded due to the high amount of parallelism required on the real time side. Nevertheless, they play an important role in non-real time processing stages in computing grids or data centres where the data from detectors is stored. GPU multiprocessor units are an option valid for the high amount of channels but not at the level of the electronics to perform the real time processing. However, these devices could be an aid to the processing centres with the stored data.

The specific integrated ASICs are valid for processing and even for other tasks if they are including more specific analogic or digitalizing parts. The main problems of ASICs are the design costs and time of production. While this solution fits on many experimental set-ups, the complexity and flexibility required for our Pre-processing makes another solution more appealing.

FPGA devices give a mixed solution between an ASIC and a fixed parallel processing system, with the benefits of customization compared to the general processors or GPU, but with an increase on the production time and design. FPGAs are devices formed by a matrix of basic electronic cells. These cells have a logical part, a register part and the capability to interconnect between them. Over the years more modules in addition to the basic cells were added, such as memory cells, digital signal processor (DSP) cells, high speed transceivers cells and, in the last years, full microcontrollers and microprocessors.

The last FPGAs have capabilities up to millions of cells as in the biggest Kintex and Virtex Ultrascale+ in Xilinx [68] or in Stratix X from Intel [69], transceivers capable of differential full-duplex lines of 32 Gbps, more than 100 Mb of distributed memory, thousands of DSP blocks and some of them incorporate ARM processors like Zynq in Xilinx and SX SoC in Intel. In the high performance devices, the aggregated bandwidth is large because of the High Speed transceivers (up to 32 Gbps) implemented, but the number of transceivers itself is low and decreases drastically in low-end devices (from 80 to 8).

In some scenarios, like ours, we would need a big number of not-so-high data rate transceivers but a reasonable big amount of resources to implement the data processing. This seems a no-win situation because devices with a lot of resources have a lot of high data rate transceivers that will be underused and, moreover, at a high price. On the opposite, devices with lower data rates, appropriate for our application, provide fewer logical resource so Pre-processing algorithms would use several of them. As it will be

shown, the use of auxiliary circuitry will provide the best of the two options: full use of data bandwidth and logical resources at a reasonable cost.

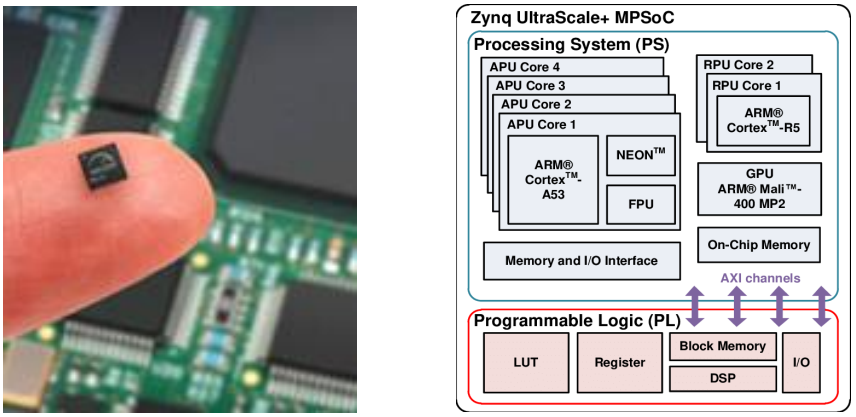

Fig. 1.20. ***Left****: IGLOO FPGA size reference.* ***Right****: Zynq Ultrascale+ MPSO processor multicore ARM + GPU + Cortex ARM Microcontroller + Xilinx FPGA fabric*

On the other edge of the FPGA state-of-the-art we can find the low power low consumption and usually low cost FPGAs for electronics with high integration. With no transceivers and lower capabilities (40k-100k cells at much), these devices reach power consumptions in the order of µW or even less in standby mode and sizes below $1cm^2$ (see Fig. 1.20). Examples of this devices are the ICE family of Lattice Semiconductors [70] or the IGLOO from Microsemi [71].

Chapter 2:
AGATA spectrometer electronics and Read Out

2.1 General description

In Chapter 1, Fig. 1.19 showed the basic scheme of the electronics for a Germanium detector array. For the AGATA case, there have been two generations of electronics up to present with similar configurations described both in Fig. 2.1. The first one was developed for the demonstrator or Phase 0 of AGATA and was also used at the beginning of the next phase to instrument 10 more detectors. The second one was designed in the Phase 1 of AGATA and used along with the precedent electronics in the array for an equivalent number of detector channels. In the rest of the document the early generation of electronics will be called Phase 0 and the second, Phase 1.

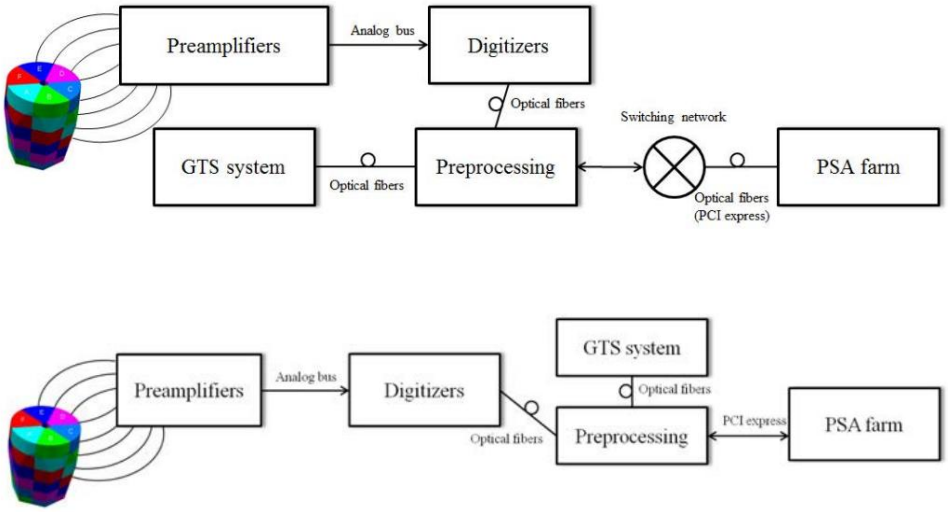

*Fig. 2.1. **Up**: First generation of AGATA electronics and Read-Out. Down: Second generation of AGATA electronics, design in the Phase 1 of the array.*

Both electronics are composed by the same functional elements: the detector electronics part or preamplifier, the digitizer, the Pre-processing, the Global Trigger System (GTS) leaf and are followed in the data stream by the data acquisition system. However, they differ in the way of implementing these functionalities for some parts.

2.2 Detector preamplifier

The detector preamplifier is the only part that stays the same along the AGATA generations (Phase 0, Phase 1 and in the future Phase 2). The deep study carried out in due time and the simplicity of their elements makes it unnecessary to upgrade it [33]. This electronic is side by side to the detector and it's implemented in two parts: one on the cold part inside the cryostat area and one on the warm part outside the cryostat. The reason for this structure is that, as mentioned in Chapter 1, germanium only collects the charges created during the ionization process, thus, in order to maintain a low-noise environment, the first stage of the electronics should remain as close as possible to the detector. The detector is cooled to 90K for normal operation and preamplifier has to be operated at temperatures near 130 K ±20 K, where their noise contribution is minimal.

On the cold part we have a low-noise silicon Field-Effect Transistor (model BF862), a 0.8 pF feedback capacitance and 1GΩ feedback resistance as a first low-noise charge amplifier stage [72]. The warm part implements the low noise transimpedance amplifier to transform current to voltage, a pole-zero stage, the fast reset system and a differential output buffer to feed the MDR (Mini D Ribbon) cables with the analogue signal to reach digitizers (Fig. 2.2).

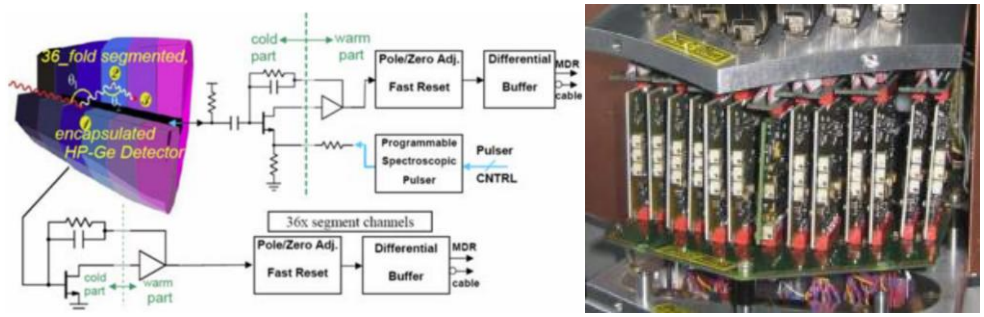

Fig. 2.2. ***Left****: Preamplifier cold and warm part conceptual design on the AGATA cryostat.* ***Right****: Images of the AGATA preamplifiers.*

In order to keep noise at minimum, both parts are carefully connected with several individual thin wires with low thermal conductivity and by a specific grounding. The preamplifier is perfectly characterized in order to ensure signal shaping and proper input for the digitizing step following the specifications.

The fast-reset circuitry avoids the effect of the saturation in the pre-amplifier stages in case of non-wanted high energy events, like cosmic rays, quickly discharging the capacitance in the pole-zero stage. This same circuit is also used for the measurement of Time over Threshold to correct overflowed signals. [73]

There are two types of preamplifier boards, the core and the segment. Each core card has two preamplifier signals for two different gains of the same core. The segment ones amplify three segment signals per board. The last key element added to the preamplifiers is the high precision pulser for the core boards. Introduction of calibration pulses into the detector bulk capacitance allows to perform tests and calibrations for the detectors.

2.3 Digitalization

The differential output from the detector preamplifier is connected through 6-channel copper MDR mini ribbon cables [74] of 10 m length each to the digitalization stage, in the same room of the detector. The digitizers have been improved in the different generations.

2.3.1 First generation (Phase 0) digitizer

In the first version of digitizers, corresponding to the design during the Phase 0, the ADCs boards were based on the AD6645 (high speed, high performance, monolithic 14-bit analog-to-digital converter) chip from Analog Devices. This integrated circuit (IC) is capable of digitalizing differential signals at 100Msps with 14-bit resolution. Once the data is digitalized, it is serialized on a Xilinx Virtex-II FPGA and sent through optical fibers to the Pre-processing stage via SFP optical connectors. The FPGA also performs a constant fraction discriminator (CFD) for fast trigger output and the Time-over-Threshold calculations of the preamplifiers. The output signals from the FPGA consist of 16-bits per channel corresponding to the digitalized data plus 2 bits for the trigger information. While the AD6645 IC has 14-bit resolution, the effective number of bits (ENOB) reached by the digitizer is about 12-bit, in very good agreement with the noise specifications of the ADC IC.

The digitizers are distributed in segment boards with 6 FADC, the Virtex-II to serialize the 6 channels and the optical output. Another specific board is available for the core with only 2 FADC instead and some extra features like a pulser and a fast trigger output. There is also another type of board on the digitizer system, a Control Card with a Xilinx Spartan II E and Ethernet connection for the slow control. All the mentioned boards have a mezzanine board to board connection for the motherboard.

As there are two type of modules (segment and core) there are also two types of motherboard. The first one houses four segment boards and the Spartan Control Card, the second one has two Segment Cards a Core Card and a Control Card. Both motherboards take care of the power supply of all the boards and interconnection for the monitoring and slow control. A total of 6 segment card, one core card, two control card and two motherboards are required to digitalize one whole crystal. This makes a total of 7 Virtex 2, 2 Spartan II, 38 AD6645, 7 optical transceivers and 2 Ethernet connectors.

The digitizing system for a complete AGATA crystal together with the inspection lines and the fast trigger for ancillary detectors is installed on a water-cooled box. The data for the Pre-processing is sent in groups of 6 through 12 channel fiber connectors for the segments and an extra QSFP per box for the core in both gains, 2 and 7 MeV. This QSFP also includes the global input clock signal for all the digitizer system. The power consumption is about 400 W and the box dimensions are 500 mm x 350 mm x 160 mm. As already mentioned the system has water cooling plates to ensure thermal stability and the power from the AGATA low power voltage system is feed by a XLR connector serving 48 V.

2.3.2 Second generation (Phase 1) digitizer

The new digitizers for Phase 1 have major improvements on integration and reduction of optical lines. The optical connection lines are reduced from 7 to 5 per crystal, the overall size is reduced to a third and power consumption is about 40-60W.

The Phase 1 digitizer system enclosure is a 5 stack compact Digitizer Box (DB). The DB includes 4 Digi-Opt12 [75] to digitalize 12 channels each, where one is used only for the 2 core signal and the other three for the 36 resting segments, and one Control Card. Besides the control tasks, the Control Card is responsible of clock conditioning/distribution and synchronization of the Digi-Opt12 cards [76].

Fig. 2.3. ***Left****: Phase 0 digitizer crate for one crystal digitalizing with 38 channels.* ***Right****: Phase 1 digitizer crate, for a triple cluster detector digitalizing with 114 channels.*

The power from the 48V of the general AGATA low voltage power supplies is transformed into the required power for each board within the Phase 1 power supply unit (Phase 1-PSU).

Digitizers

The Digi-Opt12 digitizer boards are based on the ADC1413 IC from IDT [77]. These devices digitalize 2 channels, serialize data with the JESD204 protocol [78] and output them using differential lines. Each Digi-Opt12 has 6 ADCs with all their outputs connected to a 12 line PPOD AFBR-776 [54] optical transmitter module from Broadcom Avago or equivalent.

There are two possible configurations for the Digi-Opt12: core version and segment version. The configuration can be selected by changing an interconnecting mezzanine on the boards. Besides, the Digi-Opt12 implements an analogue control system for each one of its inputs from the MDR cable. With this system it's possible to change the voltage offset of each channel by means of digital potentiometers and select each gain; the circuitry also provides a fast output trigger accessible on the front panel for the core card version. This features and many other related to the ADC, as voltage reference or the JESD204 configuration and the optical transceivers, are controlled through an internal backplane from the Control Card board.

The ADCs have similar sampling characteristics as the older digitizers, 100Msps and 14-bit width. Nevertheless, they introduce a power consumption reduction, improved capabilities and the integrated serialization. The main drawback of the integrated serialization is the intrinsic stochastic latency, with a different latency between digitalized channels. To solve this problem, all the ADC data has to be aligned on the Pre-processing side with elastic buffers; more details about this effect can be found on Chapter 6.

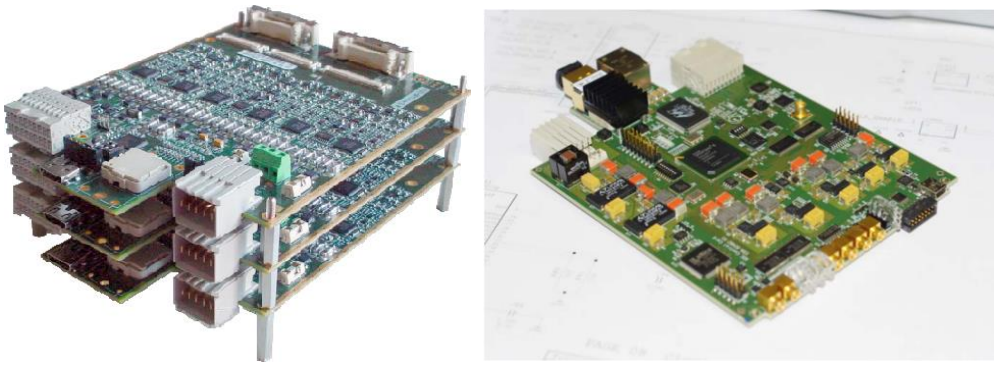

Fig. 2.4. ***Left****: AGATA Digi-Opt 12 Digitizer boards from the Phase 1 staked.* ***Right****: AGATA LP1 Control Card.*

Control Card

The Control Card takes care of providing the clock system, synchronizing all the Digi-Opt12 cards and performing the slow control. The board is implemented with a Spartan 6 FPGA and has several registers synchronized to the Pre-processing system [79]. This synchronized registers are used for slow control and configuration through an optical fibre full duplex connection, using a PPOD connector from Avago Broadcom with 4 full duplex signals.

One of the optical transceiver lines is used for the register sync, the others are for the clock system. On the Pre-processing board, the clock is synchronized to the full tree and the synchronized clock is sent through this optical fiber to the Control Card. This clock is then cleaned in a zero delay PLL (Phase Locked Loop), copied through a fan-out and sent to the digitizers.

The JESD204 protocol requires a sync signal to send synchronization information to the ADC to stablish the link. Normally, this is performed using with a high or low level in a synchronization signal. This is impossible to send through an optical link that needs a switching signal to work. The solution thought up for this system was to send through the optical link a pattern clock stealing a cycle and set it as input on the ADC. This pattern is read on the Pre-processing JESD204 custom core again to set synchronous alignment on the elastic buffers. [80]. The Control Card also controls this synchronization mechanism.

This board also can be managed standalone without a Pre-processing card through a USB connector and provides many MCX connector to customize the clock inputs and the Sync signals.

Power supply

The power input of the system is a 400 W 48V connection from the general AGATA Low voltage power supply inherited from the first generation electronics. The power supply needed by the system is 60 W at voltages of 2 V, 3.3 V and 5 V, with a high current consumption on the 3.3 V voltage. The Phase 1-PSU performs the conversion from the 48 V AGATA Low Voltage power supply to the required voltages.

On its last version, v4, the device has two isolated DC-DC converters from 48 V to 5 V and 48 V to 3.3 V and a non-isolated DC-DC from 5 V to 2 V. The output voltage is trimmed up to stablish a proper voltage value on the digitizers on a working state taking into account the conductor losses. The power supply is enclosed separately in its own aluminium case, with the XLR connector to the 48 V input and a Tyco specific connector for the digitizer power connector.

To ensure the thermal stability, it includes a small fan. Furthermore, it counts with automatic thermal and overcurrent shutdown systems and with active power LED indicators outside of the box. The design of this element will be described in the next chapter.

Digitizer box and mechanics.

All the digitizer system becomes a complex dense electronic system, with 4 levels of electronics for digitizers and one for the Control Card. The Control Card is placed on the middle level to ensure a star connection for the clock. Each of the levels or boards are screwed to an aluminium plate shaped using CNC to make contact to the critical thermal points, using thermal paste. The aluminium plates are screwed and thermally coupled to a lateral aluminium heat exchanger This lateral aluminium heat exchanger has an isolated water serpentine with an input and output connection for cold water.

The five levels of electronics are connected through two backplanes. The first one for clock distribution and slow control, the second one for power. This last backplane is connected to the outside of the box using a specific Tyco connector. The enclosure is made of aluminium and is ground connected to the crate.

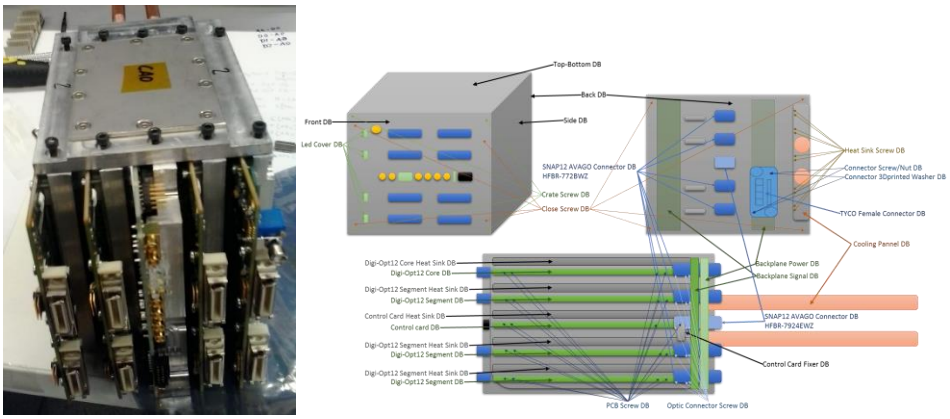

Fig. 2.5. Digitizer box disassembly image and mounting schematics.

Improvements.

Table 2.1 is a summary of the resources for the digitizer of both electronic generations, representing the technological evolution and improvement. From the point of view of the ADC characteristics there is a loss in the Equivalent Number Of Bits (ENOB) from 12 to 11.6 but this is an accepted reduction for the sake of the simplification and reduction of the system.

Phase 1 electronics has no FPGA on the digitizer side because the serializing is already done on the ADC, in addition there is a reduction in power consumption. The Control Card FPGA are reduced as well to one and the optical transceivers to 5, with no Ethernet connection needed.

The comparative also presents the power consumption reduction, the pricing, the optical fiber connection reduction and the complexity.

Digitizers Phase 0			
ADC boards: Digitizer Phase 0			
FADC	AD6645 Analog Devices	Number	6
		Channels	1
		Serialization	None
		Resolution	14 bits
		Sampling Frecuency	100 MS/s
		SNR (100MHz)	72 dB
		SFNR (70 MHz)	89 dBc
		ENOB (30MHz)	12 bits
		Power	1,75 W
		Year	2002-2008
		Obsolescence	Obsolete
Jitter Cleaner	SY89295+CS-300+Traf	jitter	<7ps
Optical Transceiver	VCSEL Zarlink ZL60101 (Segment)	Connector	MPO
		Lines	12
	QSFP - MPO (Core)	Lines	4Rx+4Tx
FPGA	Virtex 2 Pro 2VP30FF896	Number	1
		CLBs	30,8 k
		Memory	136*18kbit
		Year	2002
		Transceivers	8 MGT
		Cost	--
Offset	PCM56 + AD8138	Range	16 bits
Gain		Ranges (Mev)	0-5 / 0-20
Inspection Lines		DAC	14 bits
Control Card			
FPGA	Spartan II E	Number	1
		CLBs	
		Memory	
		Year	2002
		Obsolescence	Obsolete
		Cost	
Ethernet	RJ45 10/100BASE-T	Xport Pro	1
Jitter Cleaner	Not Needed		
Digitizer Box - Electronic per detector Crystal			
Assembly			
Digitizer Boards	Core		1
	Segment		6
Control Card			2
Motherboard			2
Backplane			0
Power Supply			0
Power			
PS Voltage	48V		
Total Power	300W		
Connections			
Optical Fibres	ZL60101 /QSFP	MPO 12 line OM3	7
Ethernet	RJ45	Ethernet	2
Diferential Input	MDR 26	MDR mini Ribbon	7
Production			
Production 1	Phase 0		16
Production 2	Phase 1		11
Cost			
Last Producction	30k€		
Nowadays	Impossible		

Digitizers Phase 1			
ADC boards: Digi-Opt12			
FADC	AD1413D IDT	Number	6
		Channels	2
		Serialization	JESD204A
		Resolution	14 bits
		Sampling Frecuency	125 MS/s
		SNR (100MHz)	72 dBFs
		SFNR (70 MHz)	86 dBc
		ENOB (30MHz)	11,6 Bits
		Power	1 W
		Year	2009-2012
		Obsolescence	Obsolete
Jitter Cleaner	Not Needed		
Optical Transceiver	Avago HFBR 772 / Reflex Fotonics SN-T12-C00601 (PPOD)	Connector	MPO
		Lines	12 Tx
		Obsolescence	Obsolete
FPGA	Not Needed		
Offset	AD5254B (8 bit pot)	Range	+-30%swing
Gain		Ranges (Mev)	0-5 / 0-20
Inspection Lines	Analog + Fast Output (Core)		
Control Card			
FPGA	Spartan 6 XC6SLX45T	Number	1
		CLBs	43,661
		Memory	401 Kb
		Year	2011
		Obsolescence	75
		Cost	Active
Optical Transceiver	PPOD QSFP - AFBR 7924	Connector	MPO
		Lines	4 Rx + 4 Tx
		Obsolescence	Obsolete
Jitter Cleaner	LMK 3200	Jitter	0,8ps
Digitizer Box - Electronic per detector crystal			
Assembly			
Digitizer Boards	Core		1
	Segment		3
Control Card			1
Motherboard			0
Backplane			2
Power Supply			1
Power			
PS Voltage	48V		
Total Power	60W		
Connections			
Optical Fibres	ZL60101 /QSFP	MPO 12 line OM3	5
Ethernet	None		
Diferential Input	MDR 26	MDR mini Ribbon	7
Production			
Production 1	Phase 1		13
Production 2	Phase 1		18
Cost			
First Production	10k€		
Second Production	9,9k€		

Table 2.1. Comparative of the Phase 0 and Phase 1 digitizer electronics.

2.4 Pre-processing

The Pre-processing provides the data bandwidth reduction and extracting of valid information to be sent to the PSA farm and written to disk. The first of its main tasks is to perform the triggering on the dataflow to reduce data bandwidth. There is a local trigger level for each crystal and the global trigger level with the GTS tree. Another important task is to extract the information to be sent: Energy for each event, Time Over Threshold, Timestamp, etc. The final task is to read data from the digitizers and communicate valid extracted features to the readout system.

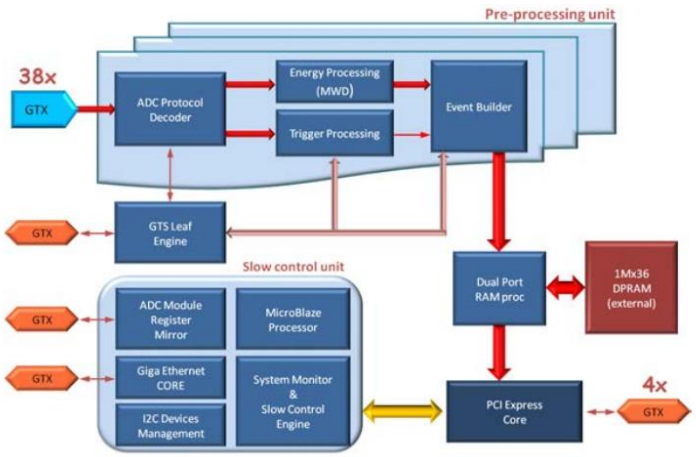

Fig. 2.6. The conceptual block design of AGATA Pre-processing system.

Both generations of Pre-processing electronics systems are situated on the PSA farm room, 50-100 m far from the detector room, and connect with the digitizers using long optical fibres.

2.4.1 Triggering system

The ADC IC in AGATA are continuously converting at 100 MHz and thus are providing data with a rate of 200 MB/s for each of the core or segment channels. As a consequence, before moving data to the processing computer farm or to the storage, data has to be prepared and reduced. The input data at the level of the Pre-processing for each crystal is 38 channels at 2Gbps, that is a total aggregated bandwidth of 76 Gbps. For this reason, the data is filtered through the triggering system and only meaningful information is transferred, providing a data reduction of approximately 90%.

AGATA specifications request a maximum event detection rate of 50 kHz. A digital Constant Fraction Discriminator (dCFD) triggers a local trigger event when a pulse appears on the core signal and exceeds a specified threshold. When a local event is identified, a trigger request signal is sent to the global trigger system together with the timestamp provided locally by the GTS system. Meanwhile, 100 samples of the rising edge of the local event are stored for further processing on the PSA for all the channels. In parallel, all the needed values extracted from the data are calculated.

When the trigger is Validated (Rejected) through the GTS for all detectors, a global trigger Validation (or Rejection) along with the corresponding timestamp and event number, is received at the GTS leaves. If validated, it triggers the Pre-processing system to send the corresponding buffered data, along with the information extracted during the Pre-processing, to the PSA farm as a valid event.

2.4.2 Energy processing

One of the most important quantities extracted from the data, at the level of the Pre-processing, is the energy. We are dealing with a high-resolution spectroscopic system and, therefore, to preserve the energy performance of the detectors is the highest priority. While the bandwidth of an AGATA detector after the pre-amplifier is about 30 MHz, the falling edge of the signal usually extends beyond 100 µs. With conventional analogue electronics, "shaping times" up to 10 µs are used to obtain the best performance, in term of resolution of the detector. With the digital processing, also large sampled pulses are required and, thus, the energy evaluation is done at the level of Pre-processing.

This is performed through a Moving Window Deconvolution algorithm (MWD) [81][82], although other methods were also studied on the early stages of AGATA design back on the earlies 2000s, like Moving Average and Continuous Average. As mentioned before, the output signal from the preamplifier of the germanium detectors has a fast rising edge from the charge collection and a slow exponential decay of the RC discharge. To retrieve the pulse energy, the preamplifier effect has to be extracted. An ideal representation of the Pulse (at initial time $t_0 = 0$) would be:

$$P(t) = \begin{cases} A \cdot e^{-\frac{t}{\tau}} & t \geq 0 \\ 0 & t < 0 \end{cases} \tag{2.1}$$

Where t is time, τ is the decay constant and A the initial amplitude, related to energy. The next pulse received from detector will be added to the tail of the exponential, if they are too close and detector is not able to separate peaks, generating a pile-up event. No matter how, the baseline level is changing each time so the first step is to hold a baseline restorer to calculate the energy pulse in relation to the baseline at pulse start.

After the baseline restorer, the MWD is applied. This is a filter to extract the exponential effect and retrieve the amplitude value, A value on equation 2.1. To do so, the exponential curve has to be compensated. First, we declare the signal read from the detector U(t) as a convolution:

$$U(t) = \int_{-\infty}^{+\infty} g(t) f(t-\tau) d\tau \tag{2.2}$$

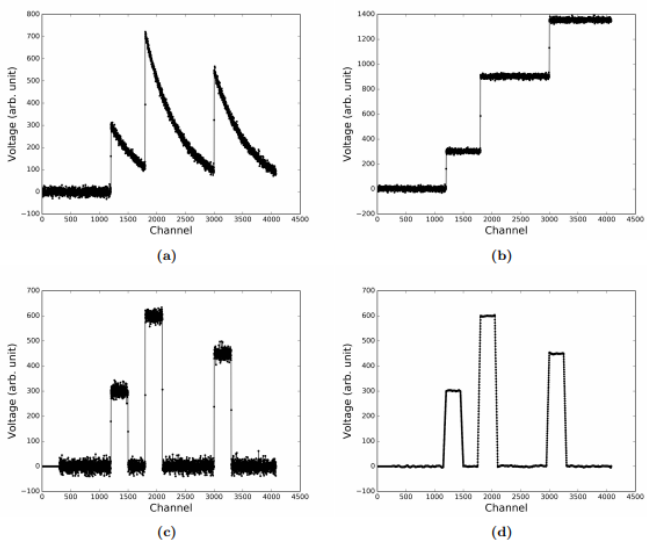

Fig. 2.7. The moving window deconvolution steps. a) The original input detector pulses. b) Deconvolution signal from pulses. c) The m-step differentiation. d) The average applied to m-step pulses.

Let's now define an auxiliary function $U(t_n)$ for a time $t_n > 0$ as:

$$U(t_n) = P(t_n) + A - P(t_n) \tag{2.3}$$

Applying the definition from 2.1:

$$U(t_n) = P(t_n) + A\ (\ 1 - e^{-\frac{t_n}{\tau}}\ ) \tag{2.4}$$

Integration of P(t) from 0 to t_n gives $\left[\int_{t=0}^{t_n} e^{-\frac{t}{\tau}}\, dt = \tau\left(1 - e^{-\frac{t_n}{\tau}}\right)\right]$. Substituting in equation 2.4 we have:

$$U(t_n) = P(t_n) + \frac{1}{\tau}\int_{t=0}^{t_n} A \cdot e^{-\frac{t}{\tau}}\, dt = P(t_n) + \frac{1}{\tau}\int_{t=0}^{t_n} P(t)dt \tag{2.5}$$

This expression can be extended to -∞ provided the P(t) function is 0 for t<0. This converts the auxiliary function U(t) in A in case of equation 2.3 and 0 for t<0, with N being the energy of the pulse. In discrete time the function transforms into:

$$U(t_n) = P(t_n) + \frac{1}{\tau}\int_{-\infty}^{t_n} P(t)dt \rightarrow U(t_n) = P(t_n) + \frac{1}{\tau}\sum_{-\infty}^{n-1} P(t_i) \tag{2.6}$$

The next step is differentiation (equation 2.7), to separate the signal into finite pulses. Selecting the discrete time, m, large enough (several times the rise time), the signal will become a square pulse for each event and the pulse height will be proportional to the energy. The selected value of m will determine the time interval with piled up pulses in which they will be separate into different square steps, if the value of m is larger than separation of two pile-up pulse, the energy will be added at some point of the step. Nevertheless, the value of m has to be large enough to proceed with the average and leave enough samples to reduce noise.

$$MWD(t_n) = U(t_n) - U(t_{n-m}) = P(t_n) - P(t_{n-m}) + \frac{1}{\tau}\sum_{k-m}^{n-1} P(t_i) \tag{2.7}$$

The last step is the average of the signal. Once the pulse train with amplitudes proportional to the energy is extracted, the averaging cleans the signal to reduce noise and each square box is shaped into a trapezoid. The mean value is compute with the moving average method of w samples (equation 2.8).

$$M_{avg} = \frac{MWD(t_n)+MWD(t_n)+MWD(t_n)+\cdots+MWD(t_{n+w})}{w} \tag{2.8}$$

After the average, the energy value of each trapezoid is extracted from the high level of the pulse, in a stable area of the plateau. The key parameters to select in the MWD algorithm are: the value of m, the number of samples to take for the differentiation; the exponential constant τ, related to the pulse decay and, in AGATA, to the RC from preamplifier and w, the weight of the final average step.

2.4.3 Comparison of the Phase 0 and Phase 1 Pre-processing

In the electronics design of the phase 0 of AGATA, the Pre-processing was located in carriers based on Advance Telecommunication Computing Architecture (ATCA) boards [83]. Each of them contained four slots for mezzanines in CMC format. To complete a full crystal electronics, two carriers were needed, one with four mezzanines dedicated to segments and the other one with two more mezzanines for segments, one for the core and one for the GTS system leaf. These mezzanines were populated with a Virtex-4 from Xilinx for processing the input data from the optical SFP connectors. The segment and core mezzanines kept the samples of the traces and calculated the energy in a Direct Memory Access (DMA) memory, sending the trigger request from the core to the GTS system leaf mezzanine. On the condition of a valid trigger, this memory was collected and read by the PSA farm [72].

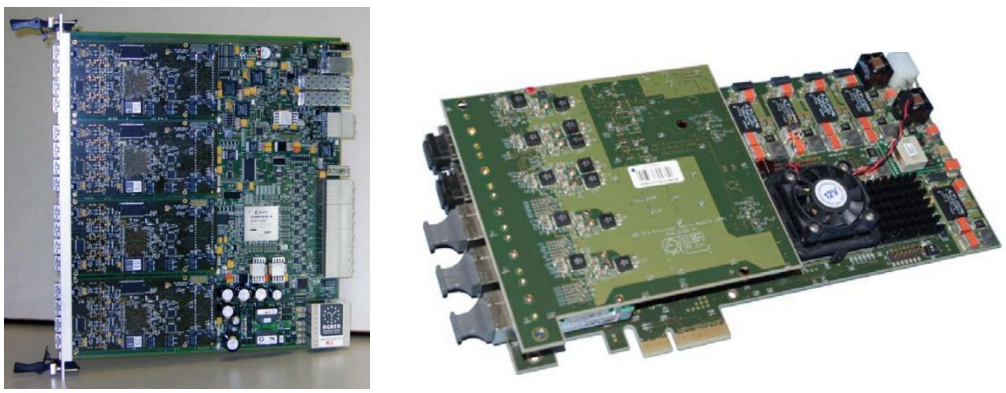

Fig. 2.8. ***Left****: The Phase 0 first generation Pre-processing ATCA carrier and Mezzanines.* ***Right****: the second generation Phase 1 GGP board for Pre-processing and readout.*

The link to the PSA farm was performed by optical connection. There were specific boards installed on the PSA farm computers that translated a PCI express (PCI-E) protocol connection from the machine through an optical fibre, the LINCO2 boards [84]. The optical fibre was connected to an FPGA on the ATCA carrier boards and it was capable to read the DMA memory. This turned the DMA stored memory data into an addressable data from the PSA farm machines side. On a valid trigger, the data could be transferred to start the PSA.

The big improvement of the second generation of electronics, Phase 1, is on the integration and optical link reduction aspects. The Gigabit General Processor (GGP) board is a PCI-E card installed in a PSA farm machine. Therefore, in this new generation the PCI-E interface board is not required. This board receives directly the 12 optical links from the Phase 1 Digi-Opt12 digitizers. The board populates a Virtex 6 FPGA from Xilinx and implements all the processing and the GTS leaf.

All the optical connectors from the GGP are on a separated mezzanine, with 3 12-line input PPOD from Avago Broadcom, the GTS link and a 6-line full duplex PPOD from Avago Broadcom for the Control Card communication. This last connector sends the slow control register synchronisation, the digitizer JESD204 sync data and the digitizing clock which can be selected either from a local one for stand-alone mode operation or from the GTS tree clock. The GTS link uses the same transceiver as the Control Card but is externally adapted to the optical fibre in order to match an SFP standard LC cable of the GTS FIFOs.[80]

The evolution of the Pre-processing is presented in Table 2.2. The amount of resources needed to process all the system are similar for each generation, but on Phase 0 the technology available forced to split the processing capability into 7 FPGA of 57.000 CLBs each. The GGP combined all in one device, but the resources available on the FPGA were on the limit of its possibilities.

Pre processing Phase 0			
Preprocesing Board: Core and Segment.			
FPGA	Xilinx Virtex 4 XC4VFX60-11FF1152 Preprocessing 6 channel	Channels Processed	6
		CLBs	56,880
		Memory	395 kb
		Transceivers	16
		Year	2004
		Obsolescence	Obsolete
		Cost	1.300 €
Input from digitizer	VCSEL Zarlink ZL60102(Segment)	Connector	MPO
		Lines	12
Con. Mezzanines. Core, Segment, GTS	Mictor - Tyco	Pinout	114
		Data Rate	8x100 Mb/s
		Slow Control, Clock, Trigger, Eth	
Carrier			
FPGA	Xilinx Virtex 4 XC4VFX60-11FF1152 Alignment, GTS connetion and tarnsmission to DAQ	Channels Processed	38
		CLBs	56,880
		Memory	395 kb
		Transceivers	16
		Year	2004
		Obsolescence	Obsolete
		Cost	1.300 €
Output to DAQ	Optical Transceiver + Linco2 PCI-E	Links	1xSFP
		Total DataRate	2,5 Gbps
Con. Slow Control	RJ45 10/100BASE-T	Ethernet	1
Power Supply	ATCA	Voltage	
		Voltage	
GTS: GTS mezzanine			
FPGA	Spartan II E	CLBs	56,880
		Memory	395 kb
		Transceivers	16
		Year	2004
		Obsolescence	Obsolete
		Cost	2.004 €
Optical Transceiver	PPOD QSFP - AFBR	Connector	MPO
		Lines	4 Rx + 4 Tx
		Obsolescence	Obsolete
Readout - Electronic per detector crystal			
Assembly			
Pre Processin	Core	1	
Mezzanine	Segment	6	
VME carrier		2	
GTS leaf		1	
Linco 2		1	
VME Crate		1	
Power			
PS Voltage	48V		
Total Power	300W		
Production			
Production 1	Phase 0	15	
Production 2	Phase 1	10	
Cost			
Original	30k€		
Nowadays	Impossible		

Pre processing Phase 1			
Preprocessing Board: GGP			
FPGA	Xilinx Virtex 6 XC6VHX250T-FF1154	Channels processed	38
		CLBs	251,904
		Memory	18,14 Mb
		Transceivers	48 x6,6Gb/s
		Year	2009
		Obsolescence	End of Life
		Cost	4824
Input from digitizer	Avago HFBR 782BZ / Reflex Fotonics (PPOD)	Connector	MPO
		Lines	12 Rx
		Power	
Conection DAQ	PCI-E v2 x4		16 Gbps
Power Supply	PCI-E Power Adaptor	DC-DC and Fuse	12V to 12V
		DC-DC and Fuse	12V to 5V
GTS: GGP			
Software	GTS Leaf Firmware in FPGA		
Optical Transceiver	PPOD QSFP - AFBR7924 + Spliter to TxRx SFP	Connector	MPO
		Lines	4 Rx + 4 Tx
		Obsolescence	Obsolete
Readout - Electronic per detector crystal			
Assembly			
GGP			1
Power			
PS Voltage	12V and 5V		
Total Power	70W		
Production			
Production 1	Phase 1	14	
Production 2	Phase 1	17	
Cost			
Production 1	9,5k€		
Production 2	6,5k€		

Table 2.2. Comparative of the Phase 0 and Phase 1 Pre-processing electronics.

2.5 Trigger and Synchronization system

The goal of the trigger system is to ensure the time coherence of the event arriving at the detector understood in a wide sense, that is, including the full AGATA detector array plus complementary detectors (charge particle or neutron detectors, spectrometers etc…), in order to accept or reject an event using information with similar timestamps. The first duty of the trigger system is that every element connected to its network has to receive a synchronous clock and respond to the detection on the basis of a common timestamp, the second is that all the local triggers have to be transferred to a common processor to validate and return an answer. These goals are achieved using a synchronization network and on AGATA this is the Global Trigger and Synchronization (GTS) system.

In the GTS, all elements of the network connected in a tree form depicted in the right hand side of Fig. 2.9. The element associated to the top of the tree is where the validation process takes place for all the local triggers and is called Trigger Processor. This element receives all validations and it's directly and only connected to the root GTS board in charge of providing a common clock and of being the starting point of the tree.

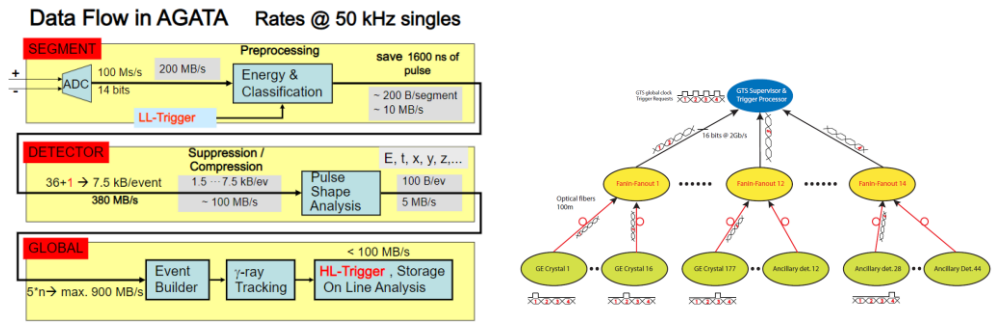

Fig. 2.9. ***Left****: Incoming data bit rate reduction effect and triggering scheme of AGATA.* ***Right****: A generic GTS tree representation.*

The connection to the rest of the tree is done using optical fibres in a SFP and LC connectors at 2 Gbps. There are FanIn-FanOut (FIFO) nodes that extent the tree from 1 connection up in the tree to 3 new elements. The final end node element of the tree is called a Leaf and represents the destination node in the clocking network. This element could be as simple as a single AGATA crystal or as complex as a whole ancillary detector. In any case, it would be treated as a trigger generator for merging the whole event.

To ensure a proper synchronous clock, each element of the network counts on jitter filters and clock delays to synchronize all clocks to central one. A 48-bit global clock counter is common for all the network elements and it's used to merge all the information from the same clock counter value as a unique event for future PSA algorithms and event builder processing. When a trigger request is fired on one of the detectors, the value of the 48-bit global clock at the trigger time is sent to the trigger processor through the GTS. When a valid global event is triggered, a new label is assigned through a global event counter (24-bit) to tag all the triggered elements and the selected timestamp 48-bit global clock counter.

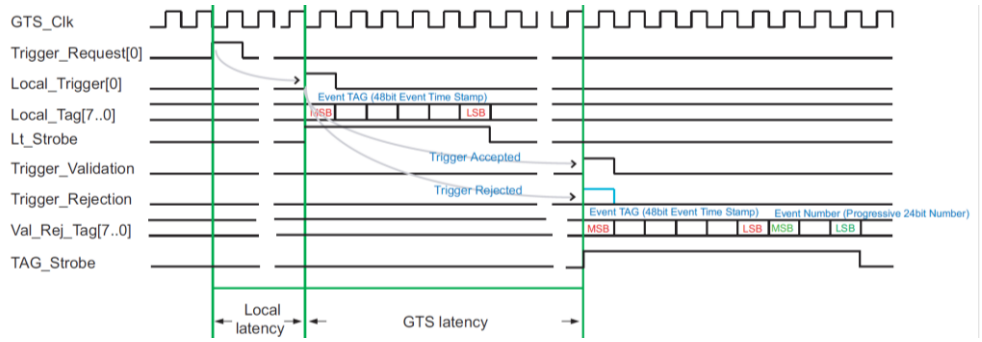

Fig. 2.10. The AGATA GTS dataflow after a trigger request from the leaf and the response of the trigger processor.

The GTS Trigger Processors is the center of the system validating or rejecting the trigger request from all detector leaves. It works only with the topological and the multiplicity information. The topological information is given by the leaf identifier (Detector Identifier) and the multiplicity information is built on the basis of the timestamps provided in the Trigger Request information. The detectors are organized in partitions and the multiplicities are evaluated within the detectors in one partition. A logical equation evaluates the trigger involving several partitions.

The current trigger processor is capable of processing up to 256 nodes and is programmable to set the desired multiplicity conditions or more complex coincidences involving several elements.

The GTS network is sending data continuously even with no triggers to ensure the system is on and synchronized, sending IDLE commands each 1 microsecond that are received on the trigger processor. There are also especial reports from the trigger processor on buffer overflows, missed trigger signals or warning signals.

The electronic implementation of the system is done in several parts. The end node leaves are implemented depending on the detector and electronic generation utilized. For complementary detectors based on analogue (conventional) electronics not fully compatible with GTS and not implementing its own leaf, the AGATA VME Adapter (AGAVA) system provides the trigger translation.

In the AGATA electronics, the first generation places the leaf on a mezzanine at the ATCA Pre-processing carrier while in the Phase 1 electronics it's on the GGP board itself, inside the FPGA in charge of the Pre-processing.

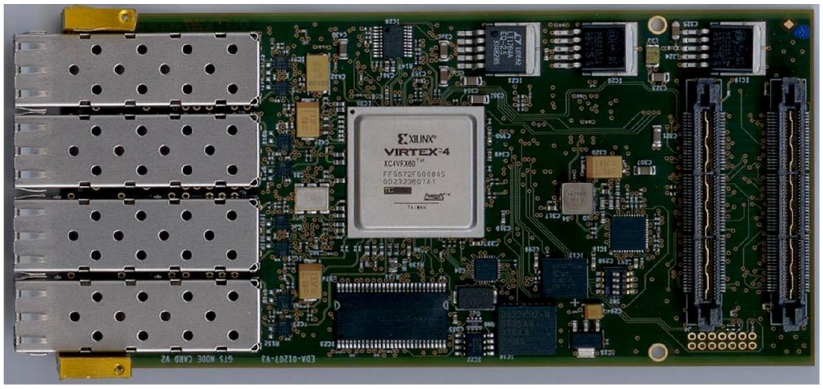

Fig. 2.11. Image of a GTS version 2 mezzanine for ATCA, it can be configured as FIFO, root or leaf.

The rest of elements of the GTS tree are the FIFOs and the root node, implemented on the same hardware mezzanines as the leaves on the ATCA carrier, populated, on its last version, with up to four SFP transceiver and a Virtex 4 FPGA for processing (Fig. 2.11). On the leaves for digitizers, only one SFP is implemented and the leaf firmware is installed while, on the FIFO, all four transceivers are used, one for up-tree connection and three for down-tree. On the root node the down-tree outputs are setup as on a FIFO node but the up-tree is sent to the trigger processor and the firmware implements the tree communication. All of them are housed on VME motherboard carriers.

2.6 Data acquisition system

For the Phase 0 and Phase 1 electronics, the data from the Pre-processing is received, through the PCI-E, on the memories of the PSA farm machines in a specific format. At present, each machine is receiving a full crystal data and it performs the Pulse Shape Analysis of the signal to calculate the gamma ray positioning. Fig. 2.12 shows the scheme of the data processing. The system is based on the Nouvelle Acquisitions temps-Reel Version Avec Linux NARVAL[85], a distribution system based on ADA for real time processing with a producer-consumer paradigm.

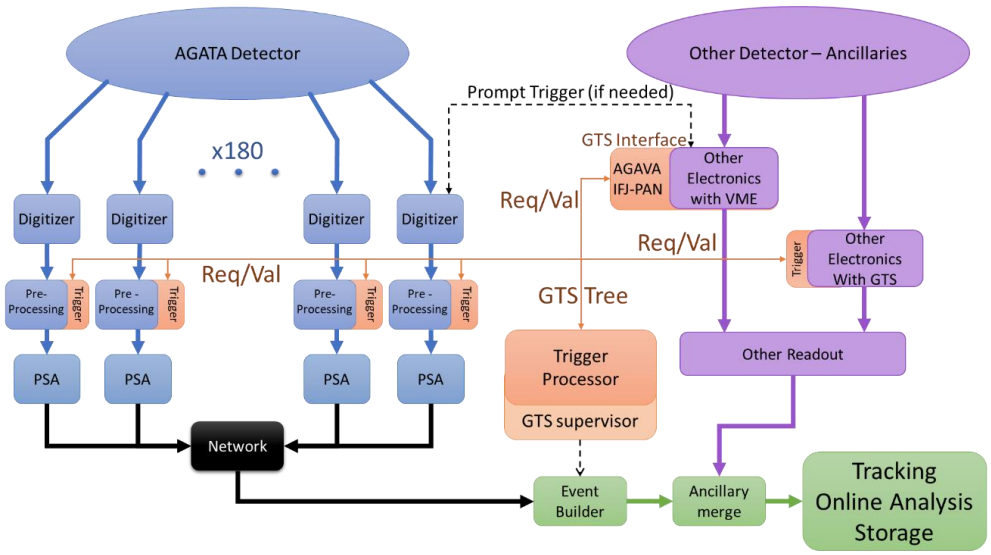

Fig. 2.12. Scheme of the NARVAL AGATA Acquisition and processing system Data Flow

This system has been recently updated to DCOD (Distributed Caen-Orsay DAQ), a software layer above NARVAL. It includes a Posix Memory Handler (PMH) to work as memory pool, a Common Transport Layer (CTL) in control of the network flow, the NARVAL system itself and ENX to control the devices in the network. The last element is the communication with the system, done by SOAP, REST or web servers.

The PSA is done for each crystal and the results from all the detector are merged on the Event Builder. The merged information is sent to the Tracking Farm where the Tracking Algorithms are applied to the data, obtaining the sequence of interactions and defining if the event is a full absorption one or not. Finally, all the processed information is stored in disks.

2.7 Phase 2 electronics requirements

The AGATA project underwent already two phases, the first of them (Phase 0) was a proof-of-concept, the AGATA Demonstrator. The AGATA project started around 2003 and most of the Phase 0 electronics was designed in 2005 (Digitizer) and 2007 (ATCA Pre-processing). The Phase 1 electronics was designed between 2010 and 2012, largely on the same philosophy of splitting the locations of digitizers and Pre-processing electronics over large distances, using optical fiber connections.

The Phase 2 of AGATA, as we mentioned before, aims to the completion of the detector array. To start the research and development for the Phase 2 electronics, there has been a study on the requirements from a technological and physical point of view to improve the performance. Based on the previous versions issues, experiences and technological improvements, the collaboration stablished several requirements on the new electronics. Several of the main statements proposed were related to further integration, getting rid of the PCI-E point to point custom connection and read-out update with the Ethernet standard, increase readout bandwidth capability, increase modularity to easy further improvements, stablish an external company for maintenance and implement testing and monitoring systems.

In addition, in an ideal detector, the preamplifier would be integrated in a standalone device inside the cryostat and the signal digitalized side by side. This concept reduces noise to the minimum and is called Digital-Preamplifier. The idea of the integrated preamplifier requires a specific ASIC development and increases the amount of heat dissipated on the cryostat. Moreover, the ADC has also too much power consumption and

heat dissipation to stablish them side by side. Nevertheless, the new Pre-processing electronics should be compatible with a future possible version of this front end and Phase 2 must study the possibility to reach this objective if the proper technology becomes available.

The first step to approach to the Phase 2 electronics is a deep study of the previous electronics and, in particular, of Phase 1. In parallel to the deployment of last productions of the Phase 1 electronics, a test system has been developed for the collaboration and is fully described on Chapter 3 as part of the work. This system is called PACE and it sets the start of Phase 2 as Phase 2.0 version which would evolve as part of Phase 2.1 and 2.2. The different versions of Phase 2 were stablished as evolutions of AGATA electronics in the Project Definition for the Phase 2. Version 2.0 will be a simple substitution for Phase 0 and Phase 1 electronics including the PACE system as a basis status. In Phase 2.1, the PACE system will be used to improve capabilities with possibly some other minor elements of the electronic chain modified. Phase 2.2 would eventually include major changes in the rest of the detector like Digital-Preamplifier and Full electronics inside the detector.

Chapter 3:
AGATA Phase 1 Electronics Test System

3.1 Motivation and testbench

My first contact with the AGATA electronics was during the commissioning of the first production of the Phase 1 version, in particular with the commissioning of the Digitizer part. While the main components of the Phase 1 digitizers were already produced before I joined the group, the DIGI-OPT-12 board by INFN-Milano and the Control Board by one of our colleagues from IFIC and ETSE-University of Valencia [80], I started my work on the development of the digitizer power supply and mounting the complete Digitizer. Meanwhile, I joined the collaboration team in LNL-INFN (Legnaro, Italy) and GANIL (Caen, France) to perform its commissioning. During this period, I learned the requirements and details of AGATA electronics and searched for possible improvements.

Later on, I took care of the installation of the Phase 1 Digitizers at GANIL. From the first installed devices we realized that AGATA electronics required a previous test before including it into the whole system on the AGATA host laboratory.

The test systems were as well used under this thesis to gain know-how and analyse possible changes for the Phase 2 electronics. The tests were carried out for the Digitizer and some of the Pre-processing of the Phase 1 second generation electronics. The testbench included as possible device under test (DUT): The Digitizer Box, the local power supply AGATA DB-PSU or the GGP Pre-processing board. Each of them could be tested by substitution of the DUT on a well-known working chain with almost all the elements of the complete AGATA Phase 1 electronics.

The full test-bench included an industrial chiller SK3318.610 from Rital to feed the cooling system [86], a server workstation with an Intel i5-4590 and the last acquisition and API software for the PCI-E GGP Pre-processing board, developed by INFN-LNL, the optical fibers and the AGATA fiber splitter, a laboratory DC Power supply Instek GPS-3303 to feed the 48V, a crate to fit the Digitizer Boxes and the set of reference tested elements. The reference tested elements were a Digitizer Box, a GGP and a AGATA DB-PSU. Fig. 3.1 shows the test-bench and the described parts.

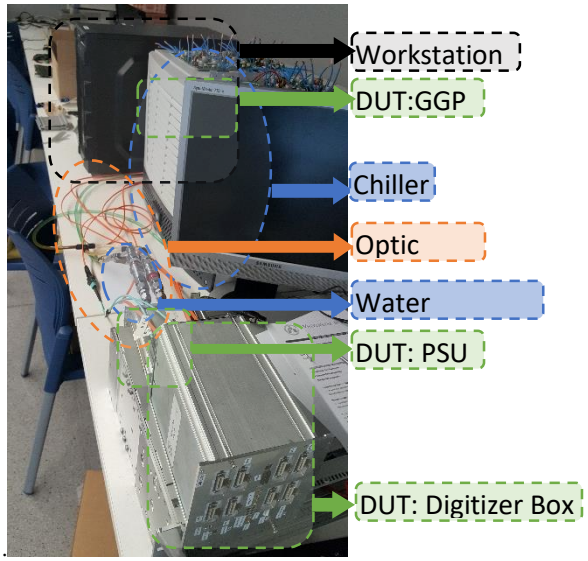

Fig. 3.1. The AGATA Phase 1 electronics Test-bench. The devices under test (DUT) are the Digitizer Box, the Power Supply Unit (PSU) and Pre-processing board inside Workstation (GGP).

3.2 Performed Tests

In order to ensure system quality there were several test to perform on thermal and power stability, internal digitizer box connections, optical connections and transceiver, data acquisition and ADC noise and data characterization.

AGATA electronics must perform its duties under continuous operation over several years, so power and thermal stability test are necessary and must be done with the fully assembled Digitizer Box. The test must ensure that there is no failure on cooling, power leak, unstable backplane connection between boards or any mechanical problem.

To monitor the DUT power and temperature, the internal sensors of the board are read continuously. Every digitizer board populates an ADC MAX11607 [87] dedicated to power voltage monitoring. In the Control Card, the voltages could be measured through the ispPAC POWR1220AT8 [88] power controller. Furthermore, every board includes temperature sensors MAX6625-26 [89] for temperature monitoring; on the Control Card board there are four of them distributed over the board surface.

These thermal and power tests were done in runs lasting above 1h for all the boards with every system fully online and once thermal stability was reached for all the components. For some of the Digitizer Box units an extra monitoring test beyond 24h was conducted as sample control. This test was normally performed through a Pre-processing interface based software, but a standalone test was developed to run directly through an USB connected to the Control Card.

The second critical point is the internal communication. To ensure this functionality a slow control bus sweep was done from the Control Card via the Pre-processing board (GGP) through a protocol implemented directly on the acquisition software of the workstation. All optical links were tested this way to ensure the transceivers functionality.

Finally, a test over the digitizer boards ADC and data acquisition was done by measuring a voltage sweep over all the dynamic range of the ADC. The digitizer boards are capable of generating a differential offset by adding a fixed value to the input differential signal through a digital potentiometer AD5254 [90]. This capability was used to test the ADC behaviour over all the working range. At every offset, several traces of 100000 samples were acquired and, for each of the offsets, the test evaluated if the electrical noise, the ENOB and the SNR were within the accepted values.

There was an extra ADC linearity test that generally was not applied, but it was implemented on the testbench. A ramp signal was applied to the ADC and data was acquired over time. The software took this data to evaluate the linearity response. This test was time consuming and usually was not required.

As well as performing the different tests, the generated testbench and associated tools are also useful for diagnostics to locate associated troubles, plotting retrieved data and results and automatically locating malfunctions.

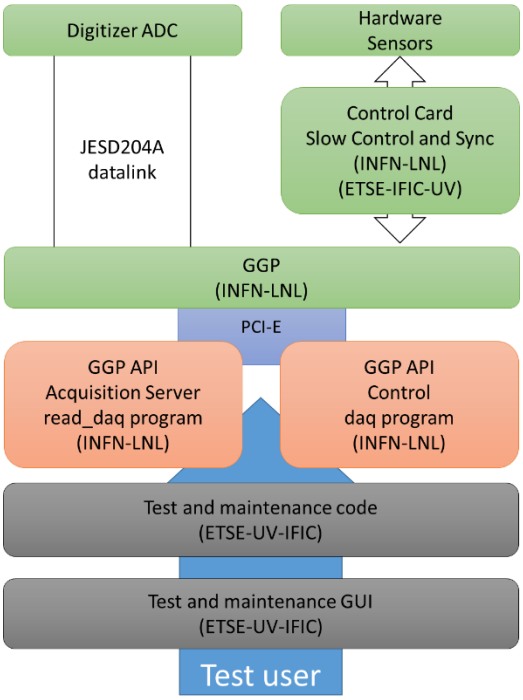

Fig. 3.2. Test-bench general diagram with the responsible developers of each bloc INFN-LNL (Laboratori Nazionali di Legnaro, Italy) are the developers for de Pre-processing GGP and its acquisition software meanwhile Digitizer ADC is developed by INFN University of Milano.

From the user point of view, two software layers have been developed, in order to perform the test, represented on the bottom of Fig. 3.2 The first is a script based automation code for the testbench and the second one is a graphical user interface (GUI).

3.3 Software

3.3.1 Stage I: Automation Code

The test system was initially developed as scripts in Python language and bash shell. Among the tools developed there were a visualizer to read data from ADCs, a temperature monitor, a temperature and power history visualizer, an automatized ADC offset values sweep measure and characterization with automatic extraction of the interesting values and the linearity analyser.

These scripts detect the system errors, retrieve associated data and create a report with the corresponding data. The documentation generated includes data channels with possible failures, power or thermal failures and values, control system problems or linearity issues.

As mentioned before, it is possible to perform thermal and power use characterization of the digitizer box standalone, just in case there is no full system with GGP included. The Control Card includes a USB socket offering full access to the digitizer slow control and the corresponding software was developed [91]. This software has been updated to include the mentioned tools and include an automated test of the Digitizer Box for power and thermal analysis. How this analysis is shown to the users can be seen in Fig. 3.3.

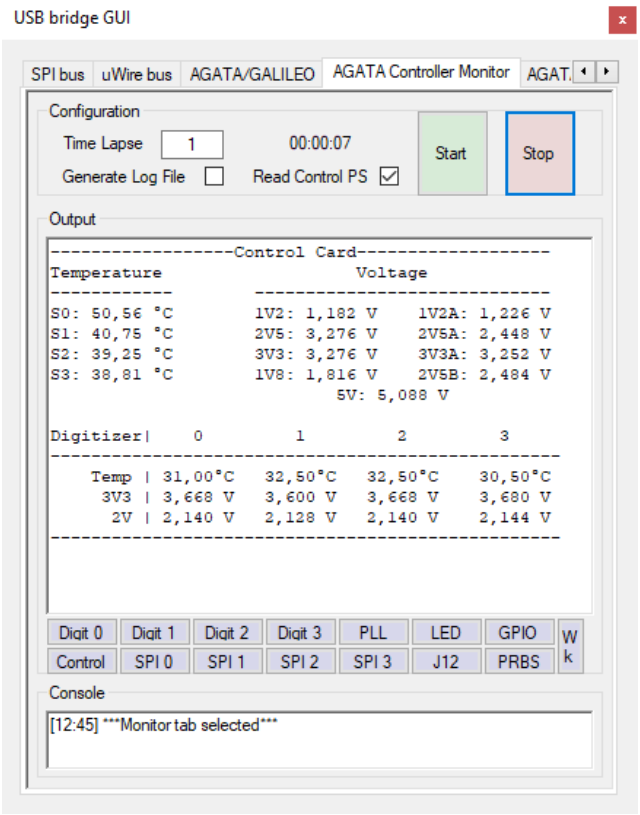

Fig. 3.3. USB bridge update to read the temperatures and voltages of the Digitizer Box through USB. This method is useful as a laboratory debugging without the full electronics chain.

The test system was working for the AGATA phase 1 electronics production chain. It detected anomalies in the digitizers that were solved or repaired before sending the complete Digitizer Box to be integrated with the rest of the detector system. Fig. 3.4 shows a comparative of test between a healthy digitizer and a one with several failures.

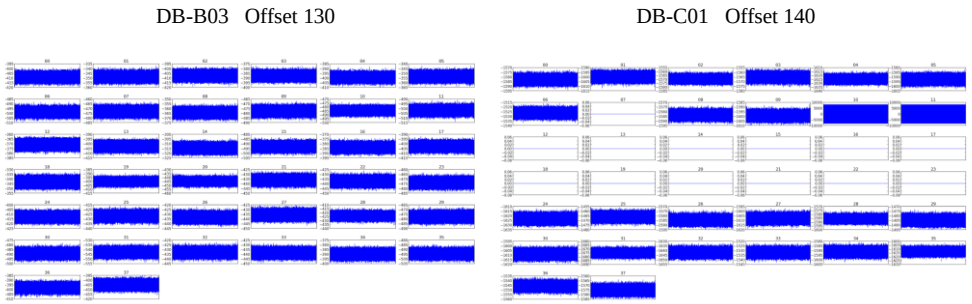

Fig. 3.4. Offset data analysis plot from a working system (up) and a falling Digitizer box (down), the software detects problems for offset value 140 with 13 non-working channels.

The software generates a report in a log file informing on which channels and offset values failures are found as well as the data values extracted. Another report includes the temperature and voltage failures with timestamp and the unstable links. The reports helped to find the failure and reduce the time of diagnostics for correctly repairing the system elements.

3.3.2 Stage II: Graphical User Interface

In order to simplify the user control of the testbench, a Graphical User Interface (GUI) was developed. This GUI included a stage test and a visual control of the full test-bench and made the analysis of the data easier; this software was completely based on the automation code from the Stage I. Fig. 3.5 depicts the automatic test functions and the GUI equivalent control and representation.

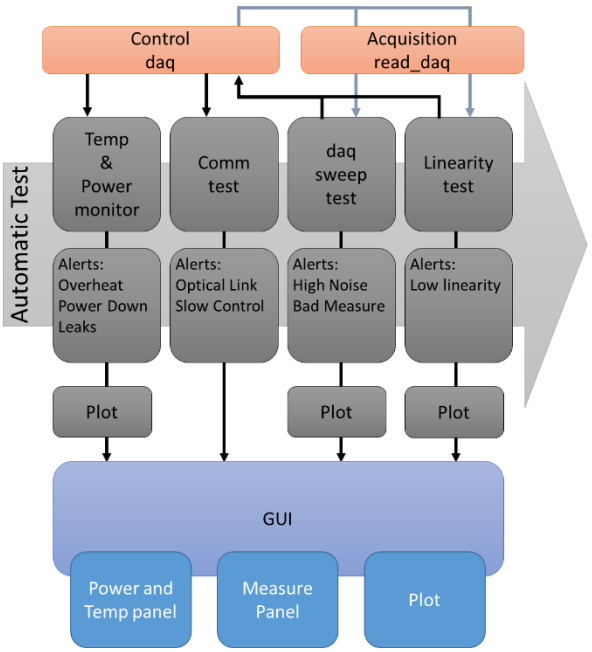

Fig. 3.5. Testbench software functionality diagram, displaying the Automatic Tests, outputs and the GUI interface.

The GUI displays registers and provides monitors for the digitizer voltage and temperatures. It includes a status window of the full digitizer box with several maintenances, diagnostics and possible tests, as initializing independently each channel, configuring digitizer and data taking. All this environment has a visualizer for each data retrieved and can also perform the automated test included in the Stage I software.

The voltage and temperature status interface is shown in Fig. 3.6, together with the control panel and status of the digitizer channels. The GUI prompts in promptly all failures and returns a similar report as in the Stage I if we start the automatic test.

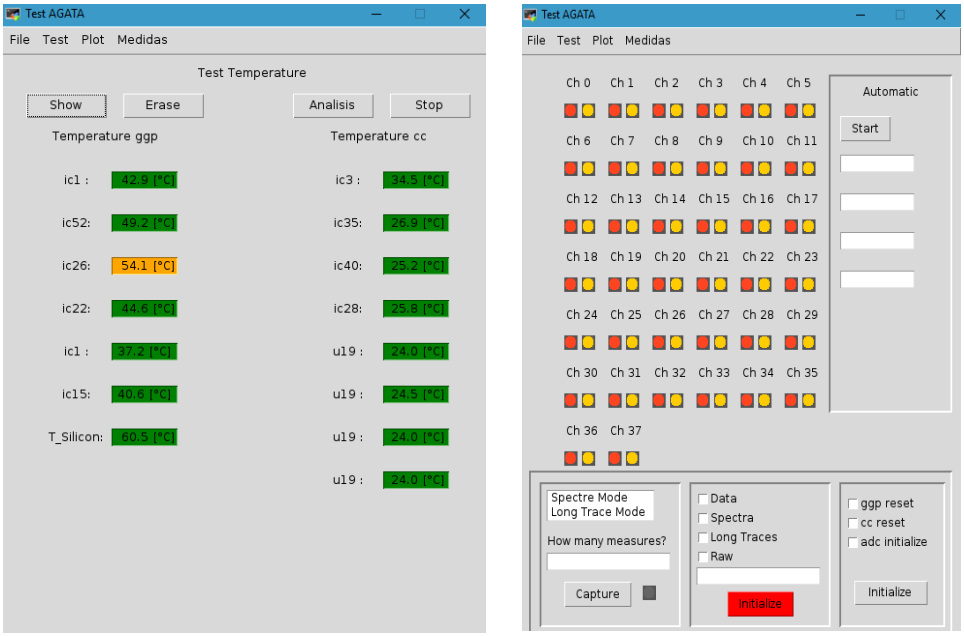

Fig. 3.6. Two of the GUI panels with the digitizer system status.

3.3.3 Stage III: Standalone test upgrade

The standalone Control Card USB test was updated during the Phase 2 electronics development to fully control the ADCs, from the Digi-Opt12 boards, with a new menu represented on Fig. 3.7. In addition, a slight modification of the Control Card firmware was carried out to set JESD204 signals and clock from an external device instead of using the Phase 1 GGP Pre-processing interfacing. This allows to implement the test-bench without the needs of a GGP Pre-processing board of Phase 1electronics, as well as the required server workstation to make it work. This standalone upgrade takes control over the ADC initialization, optical transceivers and IO expanders. It is not fully equivalent to the test of Stage I but is allows to perform a fast diagnostic on site.

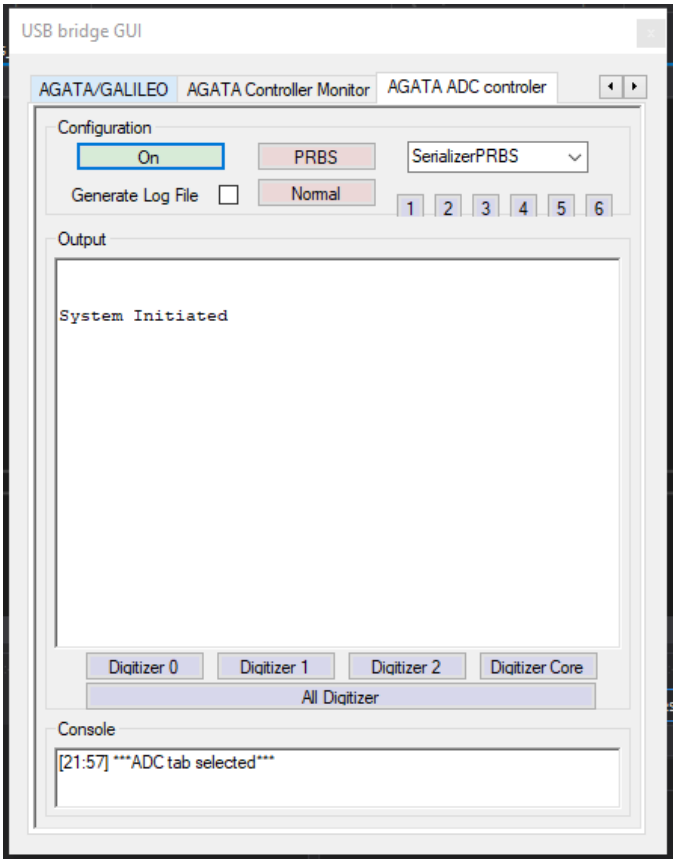

Fig. 3.7. USB Bridge Update for accessing and programming the ADC to start up in a standalone mode.

3.4 PSU analysis.

The Phase 1 electronics power supply unit was characterized to extract the full specifications. Initially, it was analysed with the original testbench described in previous sections. The main issue of this method was that power measurements were done in the Digitizer and Control Card boards, being this values filtered by internal components. On a second approach, a LabView program was developed controlling a BNC-2110 BNC [92] input connected to an ADC board PCI-6115[93] on the PCI-E computer socket, both devices from National Instruments. This second system was built in two stages, the first one measured the input voltages from the PSU itself and, in the second one, a specific board was design to read currents and voltages.

The tests were performed to retrieve several hours of data and build histograms with the voltages and currents measured. The Fig. 3.8 represents the normalized histograms for 3.3V and 2 V power supplies.

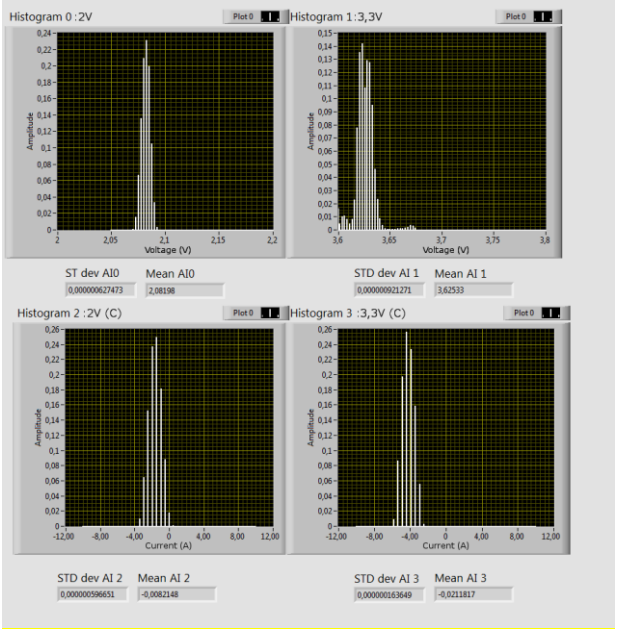

Fig. 3.8. Example of histograms output for 3.3V (left) and 2V(right) of PSU in voltage (up) and current(down).

The final test system was capable of reading the currents and voltages for the 5V, 3.3V and 2V inputs of the Digitizer Box, calculating power consumption and monitoring the power supply directly from its output. The obtained knowledge will be used, as specifications in terms of noise and stability, to develop the power supply needed for the Phase 2 electronics for the Digi-Opt12 boards.

Chapter 4:
AGATA Phase 2 electronics

4.1 Goals for the Phase 2 Electronics of AGATA

As presented on Chapter 2, the goals for Phase 2 electronics were: increase integration, an Ethernet Standard readout, increase readout bandwidth, increase modularity, externalize maintenance and include friendly testing and monitoring systems. To fulfil all the goals let's start with the basis: increase integration.

- Increase integration

The AGATA detector is an array of detectors, that requires an electronic channel per crystal from preamplifier to readout. As described in Chapter 2, these electronic channels have several stages. Therefore, two possible options could be conceived: the integration of one or more electronic stages on the same electronic channel, or the integration of the processing of more than one crystal in the same electronic channel. We will name the first one as multiple stage integration and the second one as multiple crystal integration.

At the beginning of the R&D work for the Phase 2, back in 2014, and based on these two simple concepts, two paths were considered possible and are depicted in Fig. 4.1.

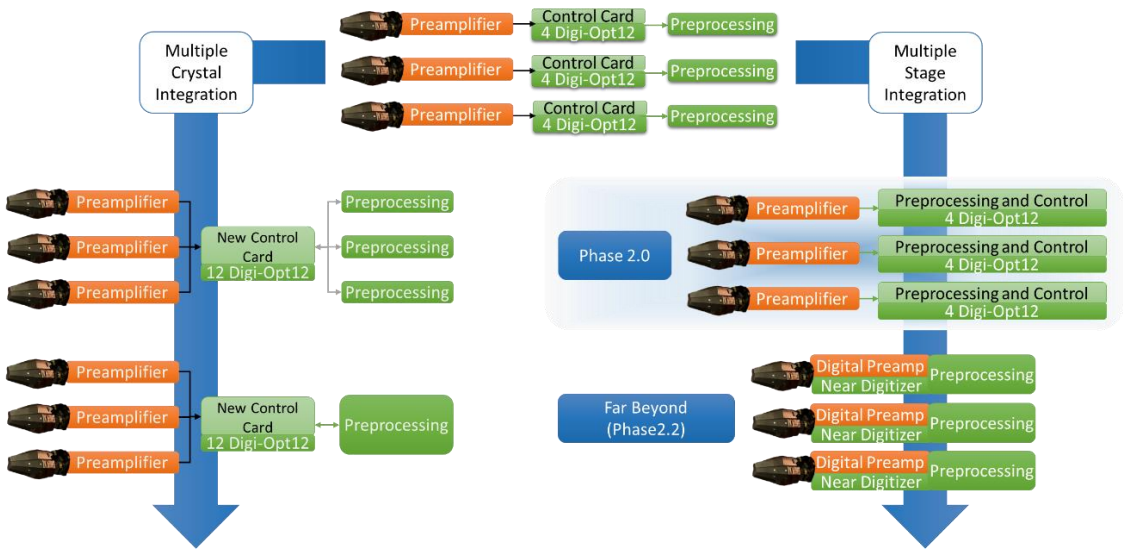

Fig. 4.1. Original proposal methodology plan map.

Taking first into consideration the multiple crystal integration, there are two electronic stages on phase 1 that would need redesign: The Control Card and the Pre-processing. For the Control Card it would be necessary to study the possibility of a new board that would provide clock and control for two, three or six crystals at once. This Control Card would face the critical problem of serving clean clock to 21 Digi-Opt12 boards in the worst case. Besides the Control Card modification also the Pre-processing would need to work with multiple crystal data. The critical drawback on this side is complexity for FPGA, although this could be overcome with present devices.

For the multiple stage integration study, there are two ways to go: the mentioned digital preamplifier and digitizer, or the Control Card, Pre-processing and digitizer. The digital preamplifier, although it is under research in the collaboration, it is foreseen as long term development and won't be considered on this work. The Control Card, Pre-processing and digitizer integration was thus thought as a stage integration possibility, with the Control Card and the Pre-processing combined in a single device side by side with digitizers on the same crate, working as a whole standalone device.

- Ethernet readout, increase bandwidth and modularity

The next main goal was the update to Ethernet readout that, to fulfil the modularity goal, was thought to become an independent mezzanine. On this side, the critical part to study was the FPGA Ethernet protocol implementation and the output throughput. The minimum output considered to maintain backwards bandwidth compatibility was 10Gb Ethernet, because, even PCI-E v2 from Phase 1 is up to 16Gbps, not all of its bandwidth is used. Nevertheless, the possibility to 40Gb Ethernet needed to be studied.

- External maintenance, monitoring and testing

The externalized maintenance goal was a common one for all the parts on the new development and was taken into account at the design of each element. The monitoring and testing was introduced later on the conceptual idea.

4.2 Design of the AGATA Phase 2 Electronics

4.2.1 Preliminary PACE design.

The original proposal, with a generic device covering all possibilities was presented to the AGATA collaboration [94] for evaluation on September 2015 during the 16th AGATA week held at IFIC - Valencia. The idea was accepted and a development team of experts was stablished.

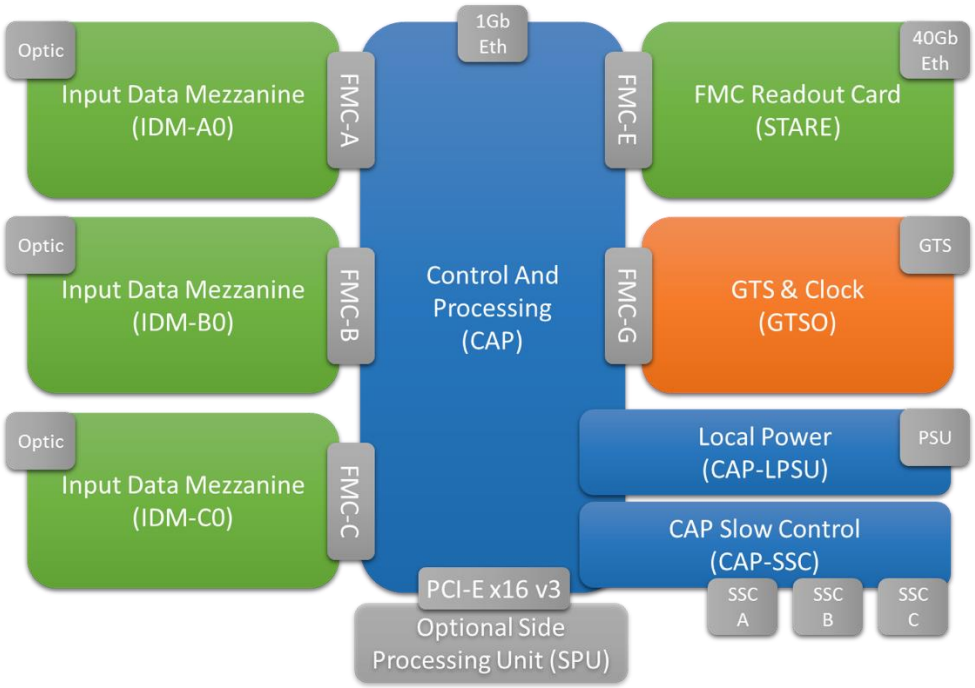

Fig. 4.2. The preliminary PACE system main design.

With the original concept in mind, an early conceptual design was developed and presented on the Phase 2 Electronics first Town Meeting on 21st January 2015 (Paris). This conceptual design is shown on Fig. 4.2. The main elements of this design are: A Motherboard for the Pre-processing and control (the reasons for such decision are explained latter), a set of three input mezzanines to represent the multiple crystal integration and the Ethernet mezzanine. In the original design, it was also included the possibility of a GTS specific mezzanine to comply with the modularity, allowing a synchronization and triggering hardware update in the future.

The whole system was named Processing and Control Through Ethernet, PACE. The mezzanines in charge of the incoming data from digitizer are the Input Data Mezzanines (IDM), the mezzanine in charge of the Ethernet readout is named Serial Transfer Acquisition Readout over Ethernet (STARE), and the motherboard hosting the mezzanines and also the Pre-processing and control is named Control And Processing (CAP).

Each of the parts answer to one of the goals mentioned on the previous section. CAP and IDM are the solution for the integration, STARE is meant to solve the Ethernet readout and bandwidth increase and the fact that they are mezzanines fulfils the modularity objective. For the integration part, it is relevant to mention here that, while the developments in commercial FPGAs have substantially increased the transceivers transmission speed, detectors like AGATA, with limited signal bandwidths, do not require higher sampling frequencies than the ones already used. This fact limits the transmission speed of the data after sampling. The use of a low costs concentrator design allows to optimize the use of the transceiver capabilities of the FPGAs, allows to optimize the balance between the number of transceivers and the resources required for the Pre-processing and, finally, this helps, as well, to optimize the cost of the FPGA. This goal is assigned to the IDM mezzanine board and will be discussed in detail in the next chapter.

4.2.2 The Phase 2 electronic collaboration.

The development of the project was distributed, with University of Valencia on charge of the IDM prototype development and full system demonstrator, as well as a future work on the development of the PACE-motherboard and the data reception part of the firmware. The STARE and 40Gb Ethernet design was assigned to CSNSM (Orsay - Universite Paris Sud) as well as the software part of the Ethernet link. The Pre-processing firmware development was assigned to IPHC Strasbourgh and all the issues related to monitoring and inspection to STFC Daresbury.

This work leaded to a design status publication on the RealTime IEEE. 20th Real Time 2016 Conference (5 – 10 June, Padova Italy [94]). Also a working document was started in order to collect information on the collaboration requirements and regular meetings were stablished.

4.2.3 IDM prototype and PACE design

The development of the IDM and STARE prototypes were initiated in parallel in the corresponding groups. The IDM prototype development took the second half of the second year (2015-2016) and the first production of the board was carried out the first half of the third one (2016-2017). The conceptual design of the PACE system design evolved, for reasons that will be mentioned later, in subsequent meetings. The IDM design and prototype was presented in the 2016 IEEE-NSS conference (Strasbourg, France)[95].

Finally, during the 17th AGATA week (CSNSM- Orsay (Paris)) the multiple stage integration solution was selected instead of the multiple crystal integration. The main reason for choosing this option was the production and maintenance costs. The costs of the FPGAs does not increase linearly with the amount of resources available, in addition to the complexity of the firmware, the costs of an FPGA, and, moreover, the availability of commercial solutions, that will be discuss latter, drops for the larger FPGAs. Thus, it was decided that for the Phase 2 electronics there would be one set of boards for each encapsulated detector electronic channel, using the IDM to optimize FPGA resources, merging the Control Card and Pre-processing and the Ethernet readout with a minimum data readout bandwidth of 10Gb.

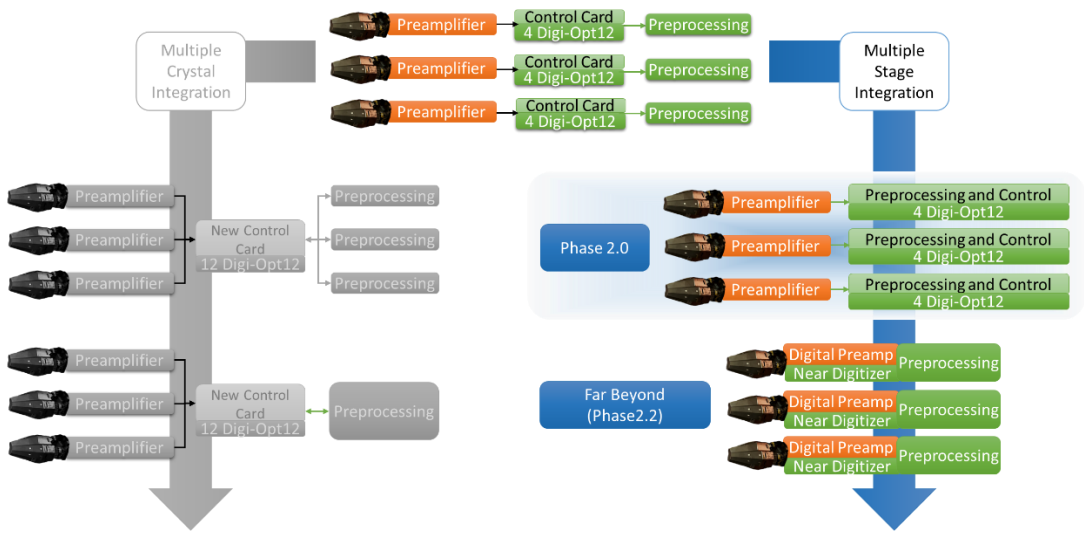

Fig. 4.3. Final Path Selected from original map.

This decision was taken after long discussion on the benefits of each solution. Finally, the reduction in board production costs in the chose option and the fact that a fault in the system while an experiment is running would only affect a single crystal, made up the decision for the multiple stage integration. Besides, given that the Pre-processing is fully parallelizable, it had no benefit implementing it for several crystals in the same device because the increase in the FPGA costs did not compensate the cost reduction of having one Control Card in the multiple crystal integration. After this decision was taken, the last version of the prototype scheme was stablished as shown in Fig. 4.3.

4.2.4 Description of the AGATA Phase 2 electronics

The final version design for the PACE system is based in a motherboard with a maximum of two mezzanines: IDM for one crystal data input and STARE for Ethernet readout. The motherboard would hold the GTS capability without a mezzanine part but maintaining compatibility with possible future triggering system developments. The new design of the PACE CAP motherboard is described in Fig. 4.4.

The Input Data Mezzanine (IDM) maintains the same conceptual design and it was in prototype production when the final decision was taken.

For the implementation of the connection to the DIGIOPT12 digitizer boards, two possible options have been considered: the optical connection to the digitizers, to be fully compatible with the Phase 1 electronics or future versions, and the copper connection one. The first one uses optical transceivers and optical fiber. The second one requires a specific cable with the socket connections from the optical transceivers 9x9 MEG-Array [96].

The validation system prototype of the PACE and Ethernet for AGATA is developed under this final conceptual design and will be described in Chapter 6. The CAP motherboard capabilities are considered by using an evaluation board and several components to simulate the slow control and clock system. The STARE has been also implemented in another evaluation board and they communicate through the final protocol used between the mezzanine and the CAP. Since it doesn't exist any evaluation board with the characteristic of the concentrator board used in the system, the IDM prototype is fully developed at this stage for validation purposes.

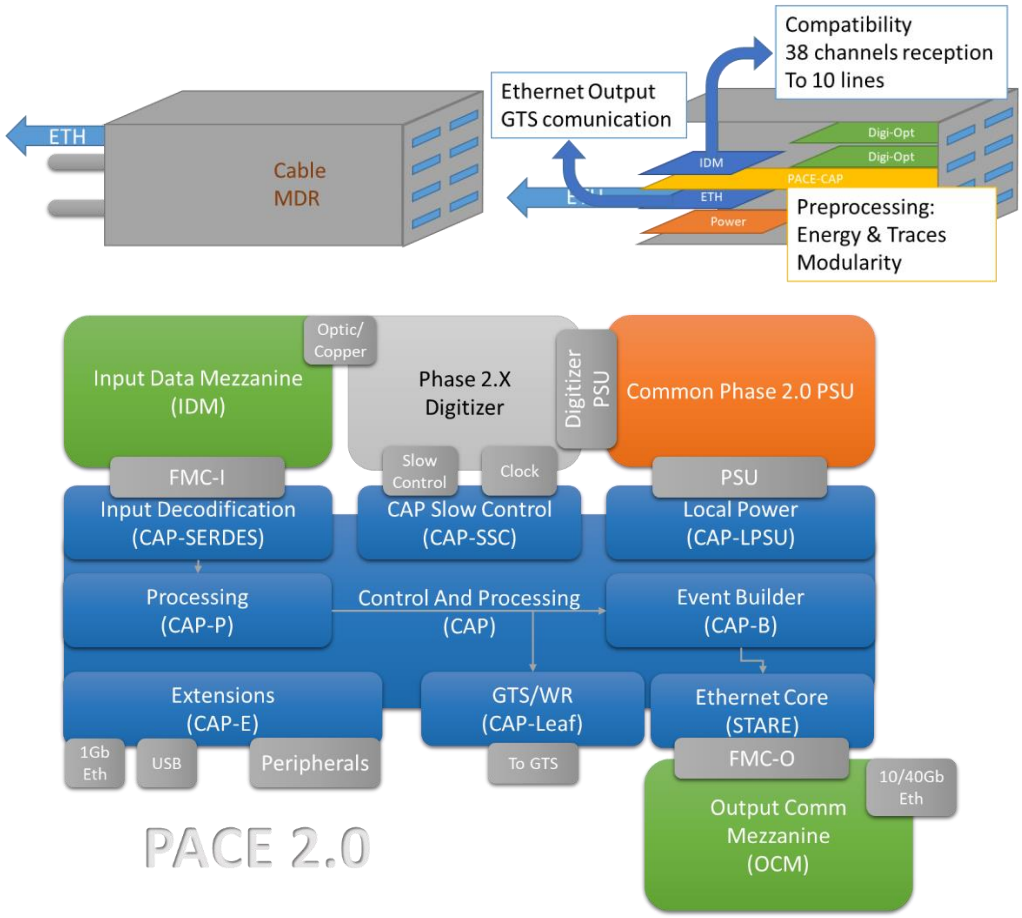

*Fig. 4.4. PACE 2.0 for AGATA phase 2.0 electronic final design. **Up**: the mechanical assembly. **Down**: The conceptual block design.*

Control And Pre-processing motherboard

The motherboard will be capable of hosting two mezzanines based on High Pin Count (HPC) FPGA Mezzanine Connector (FMC) ANSI/VITA57.1 [97] a standard designed for FPGA system. The Pre-processing FPGA hold ten 10 Gbps transceivers for IDM, four for STARE and one for GTS.

To implement the Pre-processing and all the high speed connectivity a Xilinx Kintex Ultrascale XCKU115 FPGA [98] has been selected. This device will be able to work without resources limitation, but with the drawback of an increasing in compilation time.

The slow control of the digitizers and mezzanines will be managed and distributed autonomously through the CAP board which also receives orders from the STARE mezzanine and will keep the status information of the whole system constantly. The system is designed to rise alarms if some problem appears on the system and to send them to the user through the STARE mezzanine.

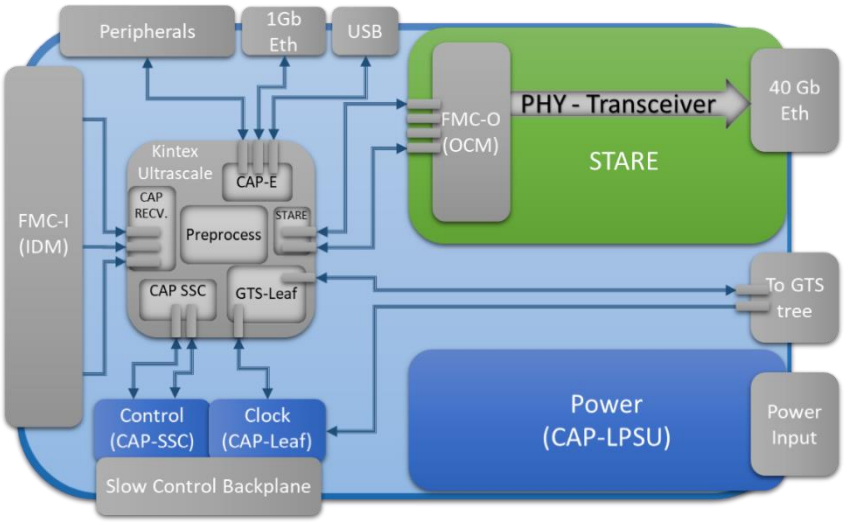

Fig. 4.5. PACE 2.0 CAP motherboard conceptual design.

All the power supply in the PACE system design is delivered from the motherboard. This board should also include multiple connectivity for debugging or possible future modifications, including a USB and one 1Gbps Ethernet port.

The GTS leaf will be completely implemented in the CAP board. To accomplish this, external delay integrated circuits and the SFP/SFP+ optical transceiver will be included. Compatibility with future trigger systems like SMART is assured because the hardware needed is similar and only firmware modifications are expected.

IDM – Input Data Mezzanine

The IDM mezzanine is in charge of receiving digitizer data and aggregate it to optimize FPGA resources. The mezzanine receives data from the optical lines through several Avago MiniPod optical transceivers or the compatible copper connector. Each of the mezzanines receives 38 channels corresponding to one crystal and is in charge of the time division multiplexing in a ratio 4:1 of the 2Gbps Digi-Opt12 JESD204 channels. This results in an aggregated output bandwidth through the FMC of ten 8Gbps channels.

The mezzanine is built in a 12 layer FR408HR with HDI (High Density Interconnect) and high speed requirements. A modular based firmware has been developed for the FPGA to provide an autonomous control of the IDM with automated alerts and only one fast I2C line for slow control. All the system is controlled by a low power Lattice ICE40LP4k FPGA [70], that initializes and monitors all the devices in the mezzanine and rises alarms if some failure happens.

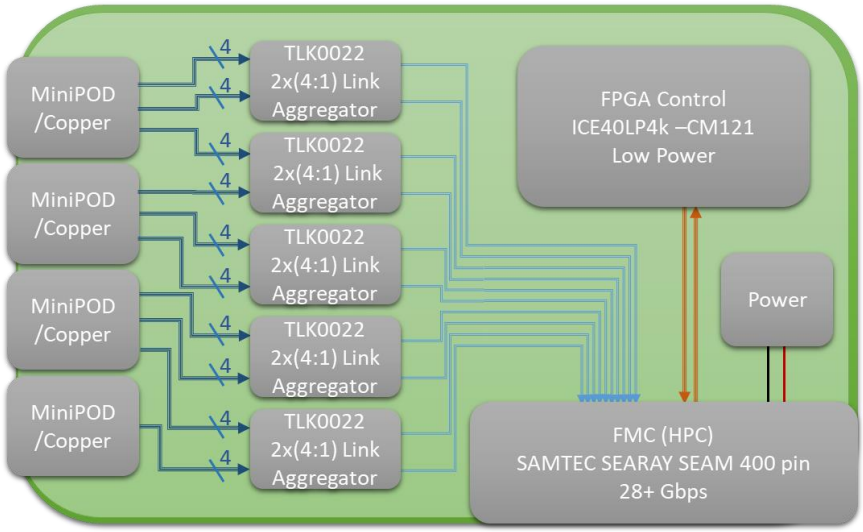

Fig. 4.6. The Input Data Mezzanine original conceptual design.

The mezzanine takes simple orders from the Motherboard FPGA using I2C commands through the FMC connector in order to modify the configuration of the components or to obtain monitoring information. This element is the main development from this work and is extensively described from the point of view of design and construction in Chapter 5.

STARE – Serial Transfer Acquisition over Ethernet

The Serial Transfer Acquisition over Ethernet (STARE) mezzanine was originally conceived to be an independent, FPGA based, 40Gb Ethernet communication module. The first prototype starts with a 10Gb link that is the minimum requirement for the pre-processed Data Readout.

All the system is managed using an FPGA with a software processor for the control algorithm (smart distribution of data over multiple servers). The slow control is based on the IPBus protocol [99] and communicates with the CAP board to manage the system. In the output, the data transmission of the 38 channels per crystal would rely on RATP (Readout Acquisition Transfer Protocol) protocol. This protocol, presently under design, will insure data consistency and implement several layers of data distribution, including communication with the AGATA data acquisition system NARVAL [85]. Memories will be implemented on each side of the communication channel to avoid latency and light packet control will be used to avoid data loses

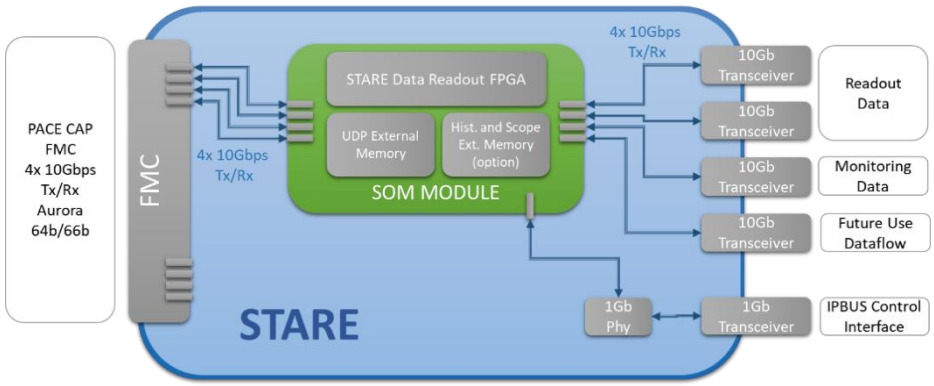

Fig. 4.7. The Serial Transfer Acquisition over Ethernet mezzanine conceptual design. Based on the last version presented at 20th AGATA Week 2019 (LNL-INFN) by CSNSM Orsay.

A later review of the project, after discussion within the electronics working group, modified the implementation of the mezzanine keeping its main goal. The final prototype version relies on four 10Gbps links and stablishes a TCP/IP protocol in FPGA on a well-known developed firmware [100]. The FMC is connected to the CAP by four 10 Gbps links using the 64/66b Aurora protocol [101]. The rest of the mezzanine remains as in the original conception.

From these four 10 Gpbs Ethernet links, two are reserved for readout, one as spare or future possible developments and one exclusively for monitoring. The monitoring is developed to be a non-invasive scope for any step in the data Pre-processing performed by the CAP FPGA firmware. The 10 Gbps monitoring exclusive link extends capabilities, with respect the current electronics, with the possibility of a scope-type direct measurement over few channels on line without triggering.

4.3 Production PACE design

After the development of the proof-of-concept system, the design has been updated with a last improvement, that will be incorporated for the production in 2021 after the full validation test.

The main difference between the production version and the prototype is the use of System On Module (SOM) devices. These SOM devices are industrial small form mezzanine PCBs with all the basic elements of common FPGA boards like external DDR memories, programming memory and power supply besides the FPGA itself. The main reason for this decision was the reduction in costs, design time and production time as well as the external maintenance of this key element of the system by a commercial company. This improvement was possible because the SoMs with the required characteristics for our development became available in the market starting early 2019.

During the proof-of-concept described on Chapter 6, the new design has been tested using a System-on-Module (SoM) board XCZU15EG-1FFVC900E from Trenz Electronics [102] which is compatible with the firmware already developed and that properly fulfils the specifications. The manufacturer company of the SOM modules ensures a maintenance of the production line for this device up to 2030, which is in accordance with the timescale of the Phase 2 AGATA electronics long life components requirement.

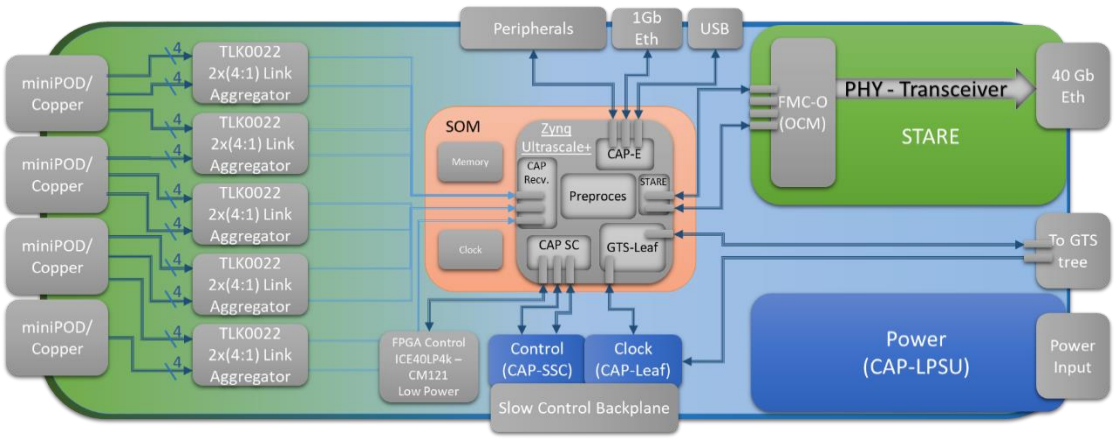

Fig. 4.8. PACE and CAP motherboard production conceptual design.

The idea of using of the SoM that now holds the FPGA processing device (instead of the CAP board as previously conceived) has changed a bit the role of the IDM that is now conceived as the motherboard where the CAP board, now a SoM mezzanine will be connected. All these changes are schematically shown in Fig. 4.8.

Chapter 5:
Input Data Mezzanine Design

5.1 Design requirements

The characteristics of the PACE-IDM design for the prototype version, mentioned in the previous chapter, were: compact FMC board compliant, in principle, with the standard Vita 57.1, connectivity to receive 38 channels from Digi-Opt12 through optical or copper lines, capability of time multiplexing of lines to reduce high speed lines in a factor 4:1 and autonomous slow control and clock adaptability.

Among the goals of the AGATA Phase 2 electronics design are: the reductions of power consumption, volume and the cost, if possible. Regarding the power consumption, the IDM is not expected to exceed 28 W. The Vita57.1 FMC standard recommends a maximum power dissipation of 10 W, so this is one of the features of the IDM prototype that is not compliant with the standard and that will require further considerations in the final design. The power consumption of the digitizers is the same as in Phase 2 electronics, the main changes are on the Control Card and Pre-processing.

The current Pre-processing power consumption is not easy to determine, as it is sitting in a PSA farm server but it was determined in laboratory conditions to be of the order of 70 W. However, on the Phase2 electronics, the corresponding power consumption has to be accurately determined because is on a common box with digitizers and powered by the same Low Voltage Power Supply of AGATA. The estimation of the total maximum power for the new electronics, including digitizer and Pre-processing, is 150 W, with IDM being about 18 % of the total power.

Regarding the production costs, in comparison with the AGATA Phase 1 electronics, the use of IDM represents a reduction on the transceiver lines to link to the FPGA, therefore, for an equivalent FPGA complexity there is a price reduction. The goal is to increase Pre-processing capabilities without increasing the costs. Taking into account that the maximum cost of the current selected FPGA SoM for Motherboard CAP (based on a Xilinx Zynq UltraScale+ XCZU15EG-1FFVC900E) is about 1350 €, it will be reduced to less than 1100 € buying large quantities for the production phase. To compare, the best cost we had for a single Phase 1 FPGA device (the Xilinx XC6VHX250T-3FFG1154C) is in the order

of 1800 € and only by special prototyping agreement with Xilinx. So with the ned design we expect a minimum saving of 700 € per crystal.

Moreover, the Phase 1 Xilinx Virtex 6 FPGA device (Xilinx XC6VHX250T-3FFG1154C) is an old model and to have the equivalent upgraded Kintex Ultrascale FPGA with double amount of resources will costs about 3000 €.

In the case copper is used for the connection between the DIGIOPT12 and the Pre-processing, an extra cost reduction is expected from the removal of the optical transceivers, but, for the moment, is not account as such, provided the optical transceiver option is also included in the design.

The current cost of the input mezzanine in Phase 1 Pre-processing is about 500 € each, excluding the transceivers. The IDM is the replacement of this board, and it has to be considered in the cost evaluation. The cost of the IDM prototype is about 2500 €, but no more than 750 € is expected for the production version. Details of the prototype cost are presented in section 5.5.

The dimensions of the board are not a major concern for the prototype but they are so for the final production. In the prototype version the final design is slightly wider than the Vita 57.1, standard. In the production design, the IDM-CAP motherboard version will be developed with the crate size constraints. The crate for the new electronics is expected to be the one used for Phase 1 described on Chapter 3, but with a box bigger in depth due to the needs of the new Pre-processing.

5.2 The IDM design

As it was described in the conceptual design, shown in Fig. 4.4, we divide the board into several areas related to the data path and functionality. These are the transceiver Input Area, followed by the 4 to 1 Link Aggregation area, the FMC area, the control area, the Clock Network and the Power Supply. Next subsections describe each one of these areas.

5.2.1 Input Area.

The incoming data from a Digi-Opt12 board is received through inputs connected to the IDM board with a single 9x9 meg-array connector from Amphenol [96]. We have two option for the connection: in the first option, a board to board cable has been developed to provide a copper connection. In the second option, a MiniPod [55] optical transceiver that fits on the same connector is used.

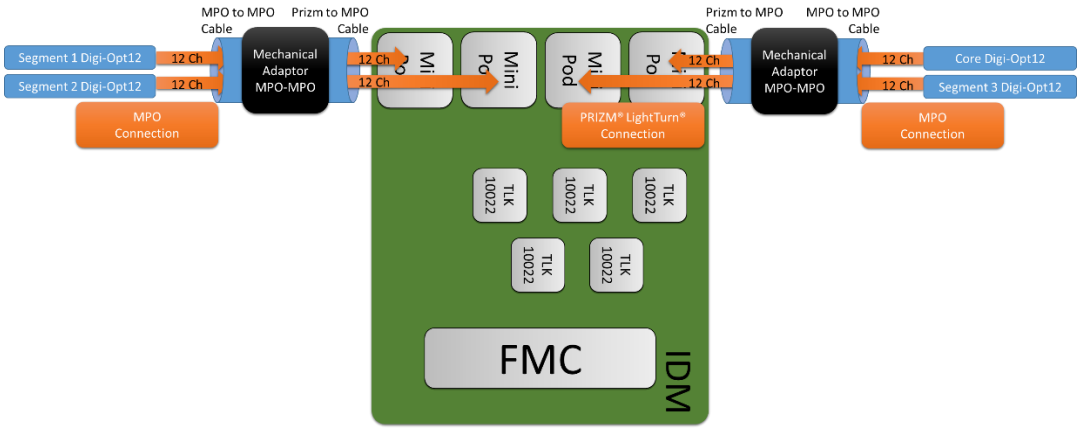

Fig. 5.1. The IDM Optic input concept and connection to Digi-Opt12 for 38 channels. There is a mechanical adaptor to change the PRIZM® LightTurn® to MPO mechanical connection.

The optical transceiver input remains mainly to have backward compatibility with the Digi-Opt12 optical transceiver PPOD type [54]. The change from the PPOD version to a MiniPod comes from the fact of the surface occupation reduction and the board to board connection features of the Prizm optical cables [103] that is the optical connection implemented for the prototype and validation. To connect the MiniPod Prizm LightTurn to the MPO of the PPOD, a patch cord is needed, as shown in Fig. 5.1. In this connection, due to the size constraint of the MiniPod IDM placed on the board, the Prizm has to be connected in pairs of MiniPods.

For the copper connection option, two possibilities have been studied: a flexible PCB and two PCB with a copper fast link connection. The flexible design has been done as a Flexi-Rigid model with five stiffeners, where the connectors are placed, and a flexible connection between them. Four of the stiffeners are smaller, with a 10x10 meg-array for the Digi-Opt12, and the fifth is for the IDM with four 9x9 meg-array. The design has been carried out with special care in the differential impedance of the lines and with the proper flex material for high speed applications. A 3D representation of the designed prototype board can be found in Fig. 5.2.

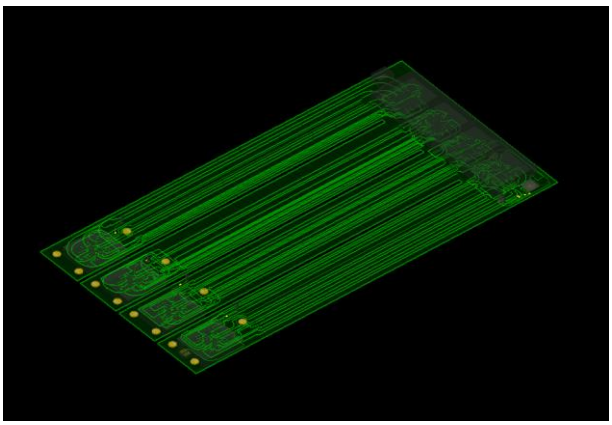

Fig. 5.2. The Flex-Rigid board PCB design for the Copper connection option.

The second option for the copper input connection is based on Samtec Twinax coaxial cables pairs with a similar design as the Flex-Rigid model but with five rigid PCB parts and the Twinax pairs connecting each PCB.

5.2.2 Link Aggregator Area.

All the 4 to 1 aggregation is performed using the TLK10022 from Texas instruments. This device is an Ethernet link aggregator designed to merge up to four lines in one with four times the bitrate [104]. The maximum output bitrate is 10 Gbps, and the expected configuration is from four lines at 1 to 2.5 Gbps to one line at 4 Gbps to 10 Gbps.

The integrated circuit is capable of decrypting 8b/10b data and encrypting data once again at high speed. Each TLK10022 has up to two output high speed channels, A and B. The device is full duplex and it's capable of aggregating transmission signals and disaggregating reception signals from other TLK in only one device. Fig. 5.3, extracted from its datasheet, represents the data flow for transmission (Tx) and reception (Rx). In our case, only the Rx side will be active.

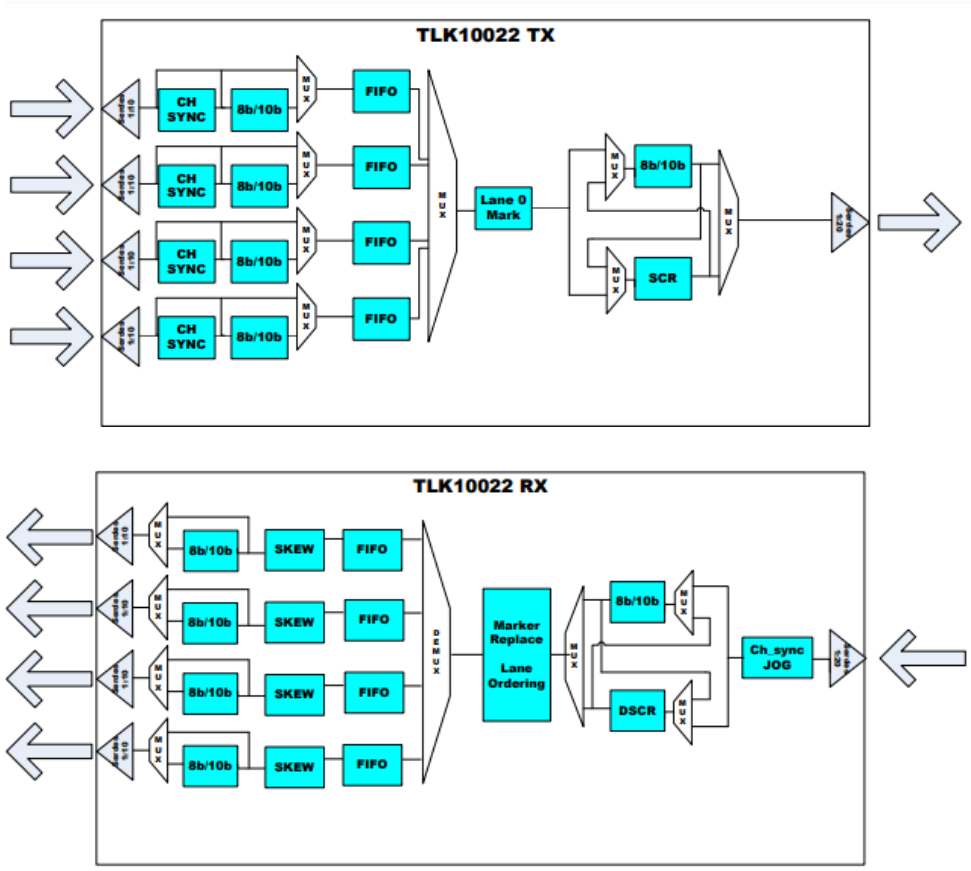

Fig. 5.3. The TLK10022 structure and behaviour as is presented don the datasheet for transmission (Up) and reception (Down).

In AGATA, 38 channels per crystal at 2 Gbps are sent by the four Digi-Opt12 boards to the IDM. To reduce the number of connections, five TLK10022 receive the 38 lines and combine them to 10 lines at 8 Gbps. These 10 lines are connected to the ten high speed links present on the FMC-HPC Vita57.1 standard connector.

The power consumption of this device is mainly due to the high speed transceivers. Every TLK10022 has a maximum consumption of 600 mA for each one of the four 1 V core voltage inputs, and few mA for the 1.8 V to feed the I/O and Phase Locked Loop (PLL). The total maximum power consumption with the device fully running is 2.5 W, but, in practice, only half of the device is going to be used, so the final power consumption is estimated to be about 1.5 W. All the interconnection between the optic transceivers, link aggregators and the output FMC are schematically shown in Fig. 5.4.

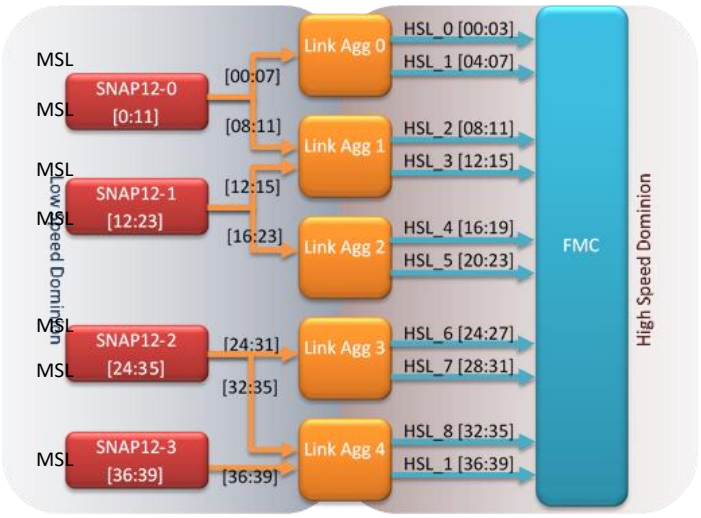

Fig. 5.4. The mid and high speed links from channel flow for IDM.

In Fig. 5.4, HSL identify the differential High Speed Lines at 8 Gbps and MSL represent the differential Mid Speed Lines at 2 Gpbs . All differential lines below 1 Gbps are named as Low Speed Lines (LSL), and normally refer to the reference clocks at 100 MHz and 200 MHz.

Clock Analysis

The TLK10022 has specific requirements for the reference clock depending on the desired input and output data rates. Table 5.1 shows the values to compute the optimum reference clock.

MID SPEED LINES (MSL)								
SERDES PLL MULTIPLIER (MPY)	Reference Clock		Full Rate (Gbps)		Half Rate (Gbps)		Quarter Rate (Gbps)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
4x	250	425	2	3.4	1	1.7	0.5	0.85
5x	200	425	2	4.3	1	2.2	0.5	1.06
6x	167	417	2	5	1	2.5	0.5	1.25
8x	125	312	2	5	1	2.5	0.5	1.25
10x	123	250	2.5	5	1.2	2.5	0.6	1.25
12x	123	208	2.9	5	1.5	2.5	0.74	1.25
12.5x	123	200	3.1	5	1.5	2.5	0.77	1.25
15x	123	167	3.7	5	1.8	2.5	0.92	1.25
20x	123	125	4.9	5	2.5	2.5	1.23	1.25

HIGH SPEED LINES (HSL)										
SERDES PLL MULTIPLIER (MPY)	Reference Clock		Full Rate (Gbps)		Half Rate (Gbps)		Quarter Rate (Gbps)		Eighth Rate (Gbps)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
4x	375	425	6	6.8	3	3.4	1.5	1.7	-	-
5x	300	425	6	8.5	3	4.3	1.5	2.2	1	1.06
6x	250	417	6	10	3	5	1.5	2.5	1	1.25
8x	188	313	6	10	3	5	1.5	2.5	1	1.25
10x	150	250	6	10	3	5	1.5	2.5	1	1.25
12x	125	208	6	10	3	5	1.5	2.5	1	1.25
15x	123	167	7.4	10	3.7	5	1.8	2.5	1	1.25
16x	123	156	7.7	10	3.9	5	2.0	2.5	1	1.25
20x	123	125	9.8	10	4.9	5	2.5	2.5	1.2	1.25

Table 5.1 Line Rate and Reference Clock Frequency Ranges for the Low and High Speed Sides of SERDES.

For the IDM, the input line rate is 2 Gbps and the output is 8 Gbps. With the aid of equation 5.1 the possible reference clocks are calculated, were RCF is the reference clock frequency, LR each of the Line Rates, RS the Rate Scale and MPY the PLL multiplier. The computed possibilities extracted from Table 5.1 are presented on Table 5.2.

$$RCF = (LR \times RS)/MPY \quad (5.1)$$

Low Speed Side SERDES (MSL)			
SERDES PLL MULTIPLIER (MPY)	Reference clock (MHz)		
	Result at Half Rate	MIN	MAX
4	500	250	425
5	400	200	425
6	333	166.667	416.667
8	250	125	312.5
10	200	122.88	250
12	167	122.88	208.333
15	133	122.88	166.667
20	100	122.88	125

High Speed Side SERDES (HSL)			
SERDES PLL MULTIPLIER (MPY)	Reference clock (MHz)		
	Result at Full Rate	MIN	MAX
4	500	375	425
5	400	300	425
6	333	250	416667
8	250	187.5	312.5
10	200	150	250
12	167	125	208.333
15	133	122.88	166.667
16	125	122.88	156.25
20	100	122.88	125

Table 5.2 Optimal Computed reference clock with selected Half rate on the Low Speed Side and Full rate on the High Speed Side.

Rates Calulation						
Ref Frecuency: 200 MHz		PII MPY	PII MPY Code	Rate	Fmin	Fmax
HS: Hi Speed	8,00 GHz	10x	0111	Full Rate	150,00 MHz	250,00 MHz
LS: Low Speed	2,00 GHz	10x	0101	Half Rate	122,88 MHz	250,00 MHz

Table 5.3. Frequency calculation for 4:1 in 2GHz input and 8GHz output and configuration of TLK10022.

The optimum reference clock is marked in green in Table 5.2 and corresponds to 200 MHz. In this case, the PLL multiplier has to be set at 10x for both sides, the Rate Scale parameter at half rate in the Low Speed Side and at full rate on High Speed Side. For test purposes, the same process has been followed to calculate the reference clocks for the 2:1 combination from 5 Gbps to 10 Gbps, with reference frequencies at about 250 MHz. The PLL multiplier has to be set at 10x and the Rate Scale parameter at full rate for both sides, in Low Speed Side and High Speed Side. Another selected combination for testing purposes is 1:1 with 2 Gbps input and output in a bypass mode, with a 200 MHz clock. In this case the PLL multiplier has to be set at 10x again for both sides and the Rate Scale parameter at half rate in Low Speed Side and quarter rate on High Speed Side. These values are used to decide the PLL possible configurations clock network.

5.2.3 FMC Output Area.

As mentioned in the general description, the connection of the IDM to the CAP is done through an FPGA Mezzanine Card (FMC). The selected FMC connector is a Samtec's 400 pin ASP-134488-01. The CAP side is designed with an ASP-134486-01 that is its compatible counterpart. The FMC connectors are fully compatible with the VITA57.1 FMC standard [97] that is the one generally used in Xilinx FPGA based Mezzanine designs.

The IDM output for the motherboard needs ten 10 Gbps connexions, a few slow control connections and power supply. There are two possibilities for Vita 57.1 regarding the pin count of the connectors: LPC with 160 connections and HPC with 400 pins. The standard HPC has 10 high speed differential lines routed meanwhile LPC has only one. The selected Samtec FMC ensures 10 full-duplex up to 10 Gbps differential lines and 82 normal speed differential lines. As the standard sets, it has also the JTAG and I2C reserved lines. The power supply from FMC comes from four pin connections of 3.3V (maximum total current of 3A), two 12V (maximum total current of 1A) and 4 at 1.8V (maximum total current of 4A). The power distribution from these lines is described in the Power Supply section.

The FMC Vita 57.1 standard specifies the dimension for the transceiver area shown as Region 2 on Fig. 5.5. with a width of approximately 70 mm. In our design, the transceivers selected on the Input Area don't fit on the required are and so, the mezzanine does not comply with the standard from the point of view of the dimensions. In practice, the width of the mezzanine was extended to 80 mm and the screw holes have custom positions.

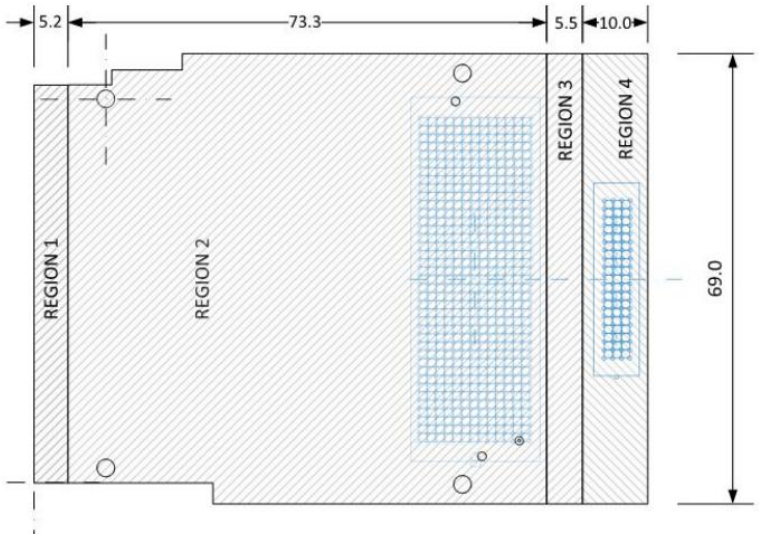

Fig. 5.5. The ANSI Vita 57.1 standard design regions and the associated dimensions.

Appendix A lists the pinouts of the IDM and the CAP, with the name of the associated signals. The DP0 to DP9 high speed differential lines going from the mezzanine to the carrier transmit the received signal from the TLK10022 link aggregator outputs.

5.2.4 Control Area.

To integrate and automate the slow control, a control system has been foreseen in the design of the IDM board. This control system has to take care of the initialization, set-up, control and monitoring of each element of the board. It is, therefore, the controller of the board and the bridge to the rest of the elements. To make it simple, for the CAP and the rest of the elements, the idea is to have only one connection as a Two Wire Interface (TWI, often seen as Inter Integrated Circuit I2C or IIC) standard slave [105] used to control all the devices from a controller.

Several devices can perform the role of the controller but they have to follow the guidelines for the design of the AGATA Phase 2 electronics, i.e. the component selected should have low cost, low power consumption, small outline and stable over time. Even though there are low power and economical microprocessors, normally stable under watchdog systems, an FPGA has been selected. These devices are usually found on the PC motherboards and more complex system working as IC initializers and power controllers, freeing the processors or bigger FPGAs from this duty. These type of FPGAs require less power and complexity than the high-end FPGA used for Pre-processing.

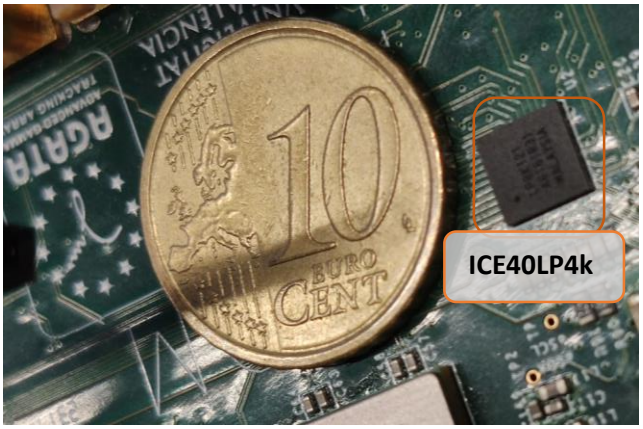

Fig. 5.6. Size of the ICE40LP4k in relation to a 10 cent coin

The ICE40LP4k FPGA from Lattice [70] with 4000 logic cells is the device selected to carry out the on-board tasks of the slow control for the IDM. This integrated circuit, on its 121 pin version, has a very small outline of 6x6 mm as shown in Fig. 5.6. The chosen device is a low power (LP) version of the FPGA with a consumption of ~400 µA for a 1.8 V voltage input. The most problematic aspect of this device is the 0.4 mm distance between pins, that requires for the design to set the vias on the PCB inside the footprint pad. This is solved using the HDI (See Section 1.2.1) technology and laser microvias in the PCB production.

The Lattice device is programmed to perform an autonomous initialization and monitorization of the board. The firmware sets the ICE40 as a standalone TWI device, from the point of view of the motherboard FPGA, accessible through the FMC serial lines. Nevertheless, if required, the master FPGA on the motherboard could directly control the IDM board TWI lines.

A set of registers accessible by TWI from the master FPGA side provides the monitoring information related to the status of the board. It also allows to set up an alarm, to alert the motherboard, in case some problem arises. The IDM is intelligent itself and does not need to be initialized or controlled externally. In case the IDM devices have to be set up with a non-default configuration, it could be done through the proper TWI/I2C registers on the FPGA.

Programming the FPGA

The ICE40 programming is done using the SPI Interface. To perform a permanent programming there are two valid options. The first one is to burn the internal ROM, but is one-time writable so it is not a good option in case the system requires an update afterwards. The second possibility is to implement an external Flash SPI Memory. This last solution is the selected method for the IDM FPGA, using a Micron N25Q032A family SPI flash memory. The advantage of this family is that it is very unlikely they will cause obsolescence issues because they are pin-to-pin compatible between generations. The component chosen for the prototype is the N25Q032A-13EF640X that fulfils all the requirements.

Two alternatives to program the ICE40 and the SPI flash memory have been implemented: through the FMC connector by the CAP master FPGA or directly from a connector mounted on the IDM board. To select the preferred option, we use a 74LVC157A multiplexer. The programming configuration is set by a switch as described in Table 5.4.

Pos	On	Off	Connection
1	Not Used	Not Used	Not Connected
2	ICE40 program Activated	ICE40 program Deactivated	ICE40_SS to SS Mux
3	Flash program Activated	Flash program Deactivated	S_FLASH to SS Mux
4	Program SPI from FMC	Program SPI from U4 con	74LCD157A A/B pin

Table 5.4. Programming area switch configuration possibilities.

There is a small green LED in the board to indicate the position of this switch. The green light off indicates that the programming is done through the FMC connector while when the LED is turned on, the local connector is selected.

The ICE40 FPGA is used to control every element on the board: the four MiniPod Optical inputs, the five TLK10022 link aggregators, the DS90CP04 input and output clock multiplexers, the PLL clock, the voltage control ADC, the six temperature sensors and the power supply IO expander. All connections to the ICE40LCP4k are described on Appendix B

Sensors.

The temperature sensors are directly controlled by the ICE40 FPGA and the registered values are accessible as IDM's master internal registers. A similar register is defined for the Voltage monitor and the "Power Good" signals from the IO expander. The table below shows all the sensors in the system.

Device	Ref	Wire	Description	Address
TMP100	IC17	I2C	Reads Top North PCB temperature	0x48
TMP100	IC19	I2C	Reads Top South PCB temperature	0x49
TMP100	IC22	I2C	Reads Bottom North PCB temperature	0x4A
TMP100	IC18	I2C	Reads Bottom East PCB temperature	0x4B
TMP100	IC20	I2C	Reads Bottom West PCB temperature	0x4C
TMP100	IC23	I2C	Reads Bottom South PCB temperature	0x4E
MAX1161	IC21	I2C	Reads Power supply currents	0x35
TCA9539	U14	I2C	Power Good signal from 1V and enable	0x74

Table 5.5. Sensors and power control devices configuration.

The measurement points for the temperature have been located near the elements with more power consumption and heat dissipation: near the TLK10022 link aggregators on the top and bottom layers respectively, under the optical transceivers, with the 1V power modules on the top and bottom layers respectively, and side by side to the FMC connector, as an enclosure temperature reference. The six devices provide a temperature map for the IDM to monitor the system and trigger the alarm in case of temperature issues.

Firmware

The firmware provides the IDM with standalone capability and receives orders from the motherboard. The code is divided into several conceptual blocks communicated by an internal parallel bus. The main firmware block is the IDM core controller, in charge of communication with the incoming TWI bus and of setting orders to the other blocks. To control each peripheral there is a specific module based on the same firmware architecture.

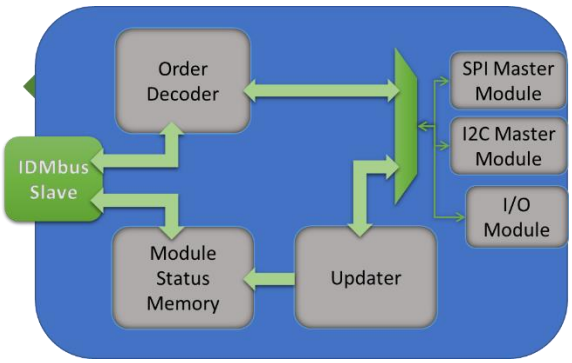

Fig. 5.7. The conceptual design a firmware module from the IDM Firmware.

The IDMbus is a simple 32-bit bus with 32 bit read and order/read signals, and a Call Signal to select the firmware module. The Call Signal is selected via a specific register and stays always active targeting one firmware module. To indicate its state, 3 red LEDs on the board are connected to the bus selection Call Signal.

Each firmware module has a decoder for the incoming orders, a Status Memory, an updater and several IO, TWI (or I2C) and SPI firmware interfaces. The Updater is regularly reading the interesting registers from the devices controlled by the firmware module and writing them to the Status Memory. The decoder takes the orders from the IDM bus and has priority over the Updater. It has an ordered instruction queue incorporated, just in case the IO and Serial firmware interfaces are busy. The output firmware modules respond to a prioritized local call request from the Decoder or Updater, with preference for the orders coming from the decoder. The Fig. 5.7 is an example of one of this firmware modules.

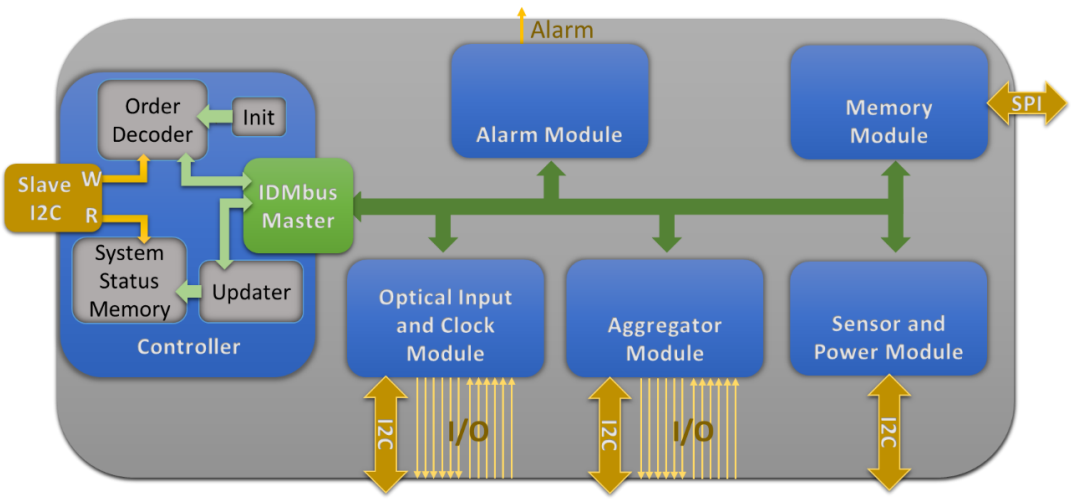

Fig. 5.8. The global conceptual design of the IDM firmware.

The firmware modules implemented are the Optic and Clock Block (O&C), Sensor and Power (S&P), Link Aggregator Block and Alarm. There is also an extra Memory Module to access the SPI memory but presently it is not active. Fig. 5.8 represents a graphical description of the IDMbus interconnection between firmware modules and the main Controller.

The Order Decoder in the Controller determines if the incoming TWI is a Master command for the device or a command for one firmware module to be sent to the IDMbus. The Updater from the Controller maps the Global registers and all the firmware modules memories into the first memory page.

The rest of the firmware modules are seen as different pages of a memory via the IDMbus Call Signal. If an TWI write (also called order/command) is detected, the active firmware module is the one responding, unless the Call Signal is 0, in which case the Controller responds. A description of the memory map and commands is presented in Appendix C.

Table 5.6 shows the relation between each mapped page, the related module and the controlled systems.

IDM Memory Address	Page	Module Name	Controlled Devices
0x000 to 0x010	0	Global Regs	8 LEDs, I2Cslave, Memory (Provisional)
0x100 to 0x199	1	Sensor & Power	TMP100 (1-6), Power ADC, IO Expander
0x200 to 0x2FE	2	Optic & Clock	DS90CP04 Switch In/Out, PLL (I2C, GPIO, PDN), Optical Transceiver 1-4 (I2C, PDN)
0x300 to 0x3FE	3	Link Aggregator	TLK10022 1-5 (MDIO interface, Power ON, Channel Power On, Signal Loss)
0x400 to 0x430	4	Alarm	Local
0x500 to 0x5FE	5	Memory	Not implemented yet
0xXFF	X	Page Change	

Table 5.6. Modules memory and command address relations and their controlled devices.

All the firmware modules have their own map table, described in Appendix C.

Table 5.6 shows, as an example, an excerpt of a map table, where each row shows the local addressed register in relation to the Global Address that includes the page address for the selected module. The registers are 32 bit long as the IDMbus and IDM registers but many of the commands are 8 bit only in this particular example because they are interfacing with several I2C devices.

When we perform a read command, the last valid value stored in the register table will be read instead of the one present in the device. This is not an issue because values can be at most 1 second old. The Updater can be turned off with a register called Lpoint on the table, to reduce the power consumption. In such case, when we perform a read command, the responsible communication module (I2C/TWI, I/O, MDIO or SPI) will start communicating with the IC device immediately.

Module	Global Address	Address	Function	Explanation	31	…	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sensor & Power	0x150	0x50	Temperature Bottom South Regs IC23	Temperature Integer		…										lastest temperature read Integer							
Sensor & Power	0x151	0x51	Temperature Bottom South Regs IC23	Temperature Fractional		…										lastest temperature read Fractional							
Sensor & Power	0x152	0x52	Temperature Bottom South Regs IC23	Configuration		…										Config							
Sensor & Power	0x153	0x53	Temperature Bottom South Regs IC23	THigh – Alarm Integer		…										Temperature high limit alarm Integer part							
Sensor & Power	0x154	0x54	Temperature Bottom South Regs IC23	THigh – Alarm Fractional		…										Temperature high limit alarm Fractional part							
Sensor & Power	0x155	0x55	Temperature Bottom South Regs IC23	Tlow – Alarm Integer		…										Temperature low limit alarm Integer part							
Sensor & Power	0x156	0x56	Temperature Bottom South Regs IC23	Tlow – Alarm Fractional		…										Temperature low limit alarm Fractional part							
Sensor & Power	0x160	0x60	IO module Set U14	Input		…		Port 0 and 1 input read															
Sensor & Power	0x161	0x61	IO module Set U14	Output		…		Port 0 and 1 output write															
Sensor & Power	0x162	0x62	IO module Set U14	Polarity		…		Port 0 and 1 polarity															
Sensor & Power	0x163	0x63	IO module Set U14	Config		…		Port 0 and 1 config: 1-input 0-output															

Table 5.7. Reduced part of the memory table on IDM.

For all the I2C/TWI serial transmissions, having as target a device in the IDM, there is a write-register custom command, compliant with the protocol, containing the device address, the device register address and the data on a 32-bit register at once. In the same way, we can also use another register to force the firmware module to read a register on a selected device. In this case, we need also to provide the memory address of the destination register for the incoming data. It is highly recommended to use the 0xEE register to read from the serial modules, because this is the default value and the reserved register for this purpose.

5.2.5 Clock Network.

The clock quality is an important requirement for the high speed link transceivers. To prepare the clock for each element, a clock conditioning section/area has been defined in the IDM PCB. The TLK10022 requires a clock with a jitter lower than 100 ppm. It has been decided to have this clock synchronous with the FPGA RX transceiver reference clock and with the digitizer sample clock of Digi-Opt12 boards. The TLK10022 input clock has been determined in section 5.2.2 and a 200 MHz frequency has been chosen as the proper reference to our system. However, to make the IDM able to work with other systems or for the testbench, this frequency has to be selectable. All the clocking system is controlled by the local FPGA accessing, through the motherboard, the corresponding TWI registers.

The differential input clock signals of the IDM from the FMC are named as CLK_FMC and CLK_AUX_FMC. Also output contacts named FMC_CLK_B_0 and FMC_CLK_B_1 are present to return the selected clock back to the motherboard.

The input clock signal for the PLL is selected by a DS90CP04 4x4 crosspoint switch from 4 possibilities: the two FMC signals, the available MCX connector pair or from the FPGA clock. The output is designed to allow a PLL bypass, so the TLK10022 SERDES reference clock could be set from the motherboard or the FPGA directly. The other option is to select the link aggregator reference clock from the PLL. The possible PLL and bypassed outputs are connected to another DS90CP04 crosspoint switch that sets up a connection to the reference clock, an ICE40 FPGA input, the FMC_CLK_B_0 motherboard FPGA feedback or the MCX output connector pair. The clocking network implemented is represented in the Fig. 5.9.

The SERDES reference has a LMK00725 low jitter six output fan-out differential clock driver before feeding all the TLK10022 link aggregators. There is also an extra output on the clock driver connected to FMC_CLK_B_1 that feeds the FPGA transceiver GBT clock at the motherboard. All these signals are LVDS.

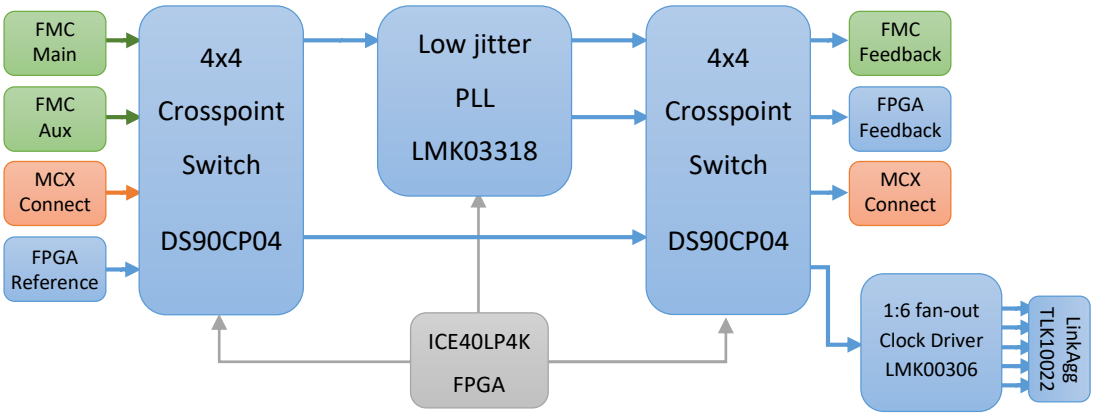

Fig. 5.9. The clocking network for the IDM, controlled through the Optic & Clock Module registers of the FPGA.

For the final connection with PACE, the common clock is originated by the motherboard and received through the FMC. The FPGA GTH clock reference is generated in the local PLL or originated by the motherboard. The full system control is done through the Lattice FPGA.

5.2.6 Power Supply.

The power input of the IDM comes from the FMC connector described in 5.2.3 with 12 V, 3.3 V and a variable Vadj fixed at 1.8 V. The 12 V is reserved for the five link aggregator core and transceiver voltages. The power system has been designed to support up to four 5 A at 1 V outputs because the aggregator device needs four different 1 V power supplies. The 12V input is lowered to 1.5 V with a LTM4637 DC-DC switching regulator, mounted on the board, in order to limit the power dissipation; the maximum output current for this device is 20 A. The resulting 1.5 V feeds four LT3070 LDO to 1 V with a maximum output of 5 A. These values are highly overrated: the 1 V power supply currents are not supposed to consume more than 2.5 A.

The TLK10022 also needs a 1.8 V voltage for the I/O. This voltage is extracted directly from the FMC Vadj at 1.8 V. This voltage has four different RLC filters for each one of the supplies connecting to the high speed and low speed transceiver sides power inputs of the TLK10022, both in transmission and reception.

When using the IDM with Optical links, the AFBR miniPod requires 2.5 V (max 670 mA) and 3.3 V (max 200 mA), both provided from the FMC 3.3V, with an LDO LT1764-25 for the 2.5V. Furthermore, the Optical Transceivers require a specific filter to clean the power signal to work properly, shown in Fig. 5.10.

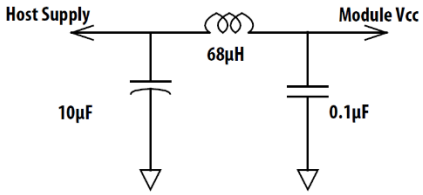

Fig. 5.10. The miniPod power filter implemented in IDM and recommended by AVAGO.

The FPGA ICE40 requires a power supply of 1.2 V with approximately 15 mA maximum input current and 3.3V/1.8V for the IO with less than 300 mA of current. It requires two different sources of 1.2 V, one for the core and one for the embedded ultra-low power Phase Locked Loop (PLL). The latter voltages are generated using the 1.8 V, from the FMC input connector, using the DC/DC adapter LT3021-12 LDO from Linear Technologies. The IO power is taken directly from the FMC inputs.

Name	Voltage	Description	Lines	Connection
VCC	1.20 V	Core supply voltage	4 lines	P1V2core
VCCIO0	1.8 V	I/O bank 0 – TLK inputs	1 line	P1V8
VCCIO1	2.5 V	I/O bank 1 – Clock System	1 line	P2V5
VCCIO2	3.3 V	I/O bank 2 – FMC and Optic	1 line	P3V3
VCCIO3	3.3 V	I/O bank 3 – Differential	2 line	P3V3
VPP_2V5	2.5 V	NVCM program Voltage	1 line	P2.5V
VPP_FAST	unconnected	Optional fast NVCM	1 line	NC
SPI_VCC	3.3 V	SPI interface supply voltage	1 line	P3V3
VCCPLL	1.2 V	PLL supply voltage	2 line	P1V2pll
GND	GND	Common GNC	5 line	DGND

Table 5.8. Power supply connections for FPGA, needs, description and connections

Table 5.8 is a summary of all the needs from the integrated circuits in terms of voltage and Fig. 5.11 shows the interconnection of the power tree.

In order to estimate the maximum power consumption for the IDM mezzanine prototype it is necessary to use the maximum ratings of all devices shown in Table 5.9. The results are: 1.05 A at 12 V, 3.5 A at 3.3 V and 1.7 A at 1.8 V, resulting in a total maximum power rating of 27.5 W.

Name	Voltage	Current Max	Origin	Feeds
fmc12V0	12 V	1 A	FMC	Input
fmc3V3	3.3 V	3 A	FMC	Input
fmc3V3aux	3.3 V	500 mA	FMC	Input
fmc1V8aux	1.8 V	4 A	FMC	Input
p2V5	2.5 V	2 A	fmc3V3	Optical transceiver, Clock network, FPGA IO1
p3V3	3.3 V	2 A	fmc3V3	Optical transceiver, FPGA IO2, Temp and Volt Sensors, PLL, FPGA IO2,3
p1V2core	1.2 V	15 mA	fmc1V8aux	FPGA core
p1V2pll	1.2 V	15 mA	fmc1V8aux	FPGA PLL clean
p1Vla1/ VDDA	1.V	3 A	fmc12V0	Link aggregator core analog 1
p1Vla2/ VDDT	1 V	3 A	fmc12V0	Link aggregator core analog 2
p1Vld/ VDDD	1 V	3 A	fmc12V0	Link aggregator core digital
p1Vld2/ DVDD	1 V	3.5 A	fmc12V0	Link aggregator core digital 2
p1V8pll	1.8 V		fmc1V8aux	Link aggregator PLL clean
p1V8core	1.8 V		fmc1V8aux	Link aggregator IO, FPGA IO0

Table 5.9. Power lines names, feed devices and consumption current.

This power value is a safe maximum, knowing that the TLK devices consume much less in practice, with approximately 15 W in the working conditions used in the IDM board. The FMC Vita 57.1 recommendation is 10W and as mentioned before this is the second aspect where IDM prototype is not compliant with the standard. Nevertheless, the Samtec FMC connectors are fully capable of providing this power.

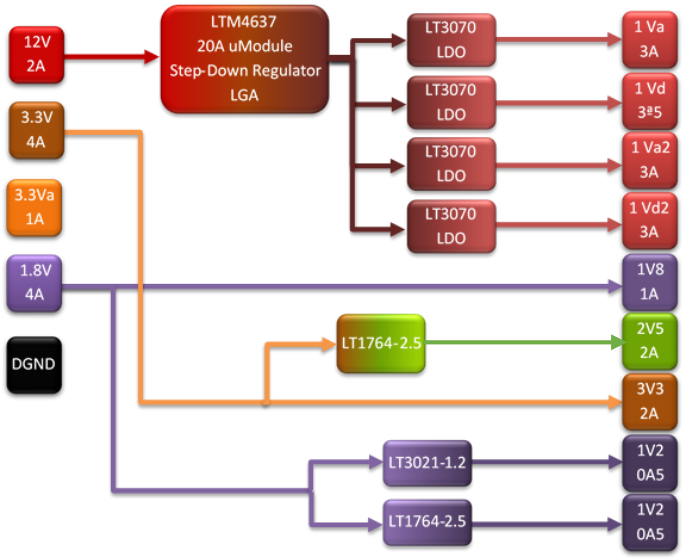

Fig. 5.11. Power distribution scheme for IDM motherboard.

5.3 Timing and High Speed considerations

The high speed digital design has extra considerations to add to the selected components and firmware. There are specific constraints to be fulfilled on the Stack-Up distribution, the material used for the PCB construction and specific routing strategies to ensure proper timing and signal integrity. All the design procedure is complemented with simulations to reduce the number of possible failures on the prototype production.

5.3.1 Design, Stack-up and materials.

The design has been carried out with Cadence Design Entry Capture [106] for schematic design and Cadence Allegro PCB Designer for layout [107]. To design the board a specific set of component libraries, with the required devices, has been created in the framework of the Cadence PCB Librarian.

After several iterations of placement and routing, the number of layers was optimized to 12 with a distribution set as seen on the Fig. 5.12. The TOP, BOTTOM, L2 and L9 are the high speed layers with 100 Ω controlled differential impedance traces. In order to ensure this impedance, 4 ground (GND) planes, L1, L3, L9 and L11 are required. The four internal core layers are used for power distribution (L4, L5 and L6) and common line routing (L7). As shown, the internal layers are built form a simple FR4 6-layer PCB whereas the outer ones, meant for high speed interconnections, use the HDI FR408HR material.

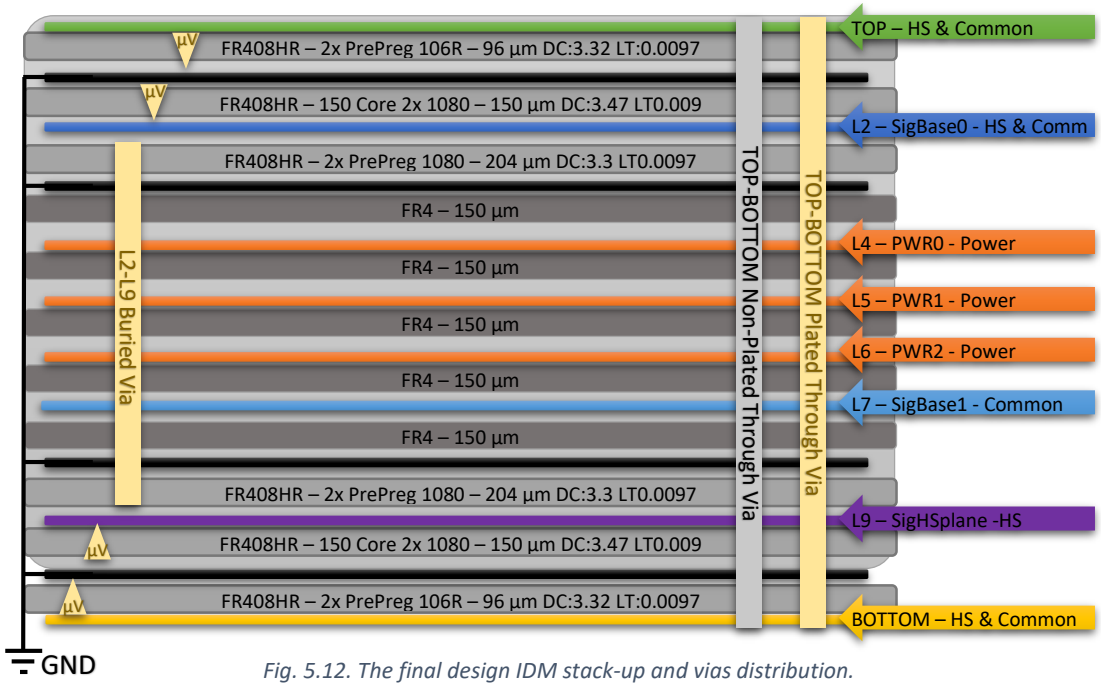

Fig. 5.12. The final design IDM stack-up and vias distribution.

The high speed capabilities are brought by the high speed isolator material on the prepreg (bonding sheets for use in multilayer printed circuits) and cores between GND and the high speed layers. The first approach to the design was done using a N4000-12 Nelco [58] dielectric with 0.008 loss tangent and 3.8 dielectric constant for a 1 GHz signal. Nevertheless, the need of HDI technology and laser Microvias for proper production is not compatible with common N4000-12, so many manufacturers prefer to use other materials. The solution selected was the FR408HR from Isola, available and recommended by the manufacturing company and also with a lower price. The Nelco company has also a version of the N4800-20 material fully compatible with the HDI procedures at a higher price, that will be studied for future productions.

The FR408HR has a higher dielectric constant and tangent loss, nevertheless, the manufacturer presents the product as a high speed material acceptable in ranges below 10 Gbps as it's our case. The characteristics of FR408HR are found in Table 5.10 up to 10GHz [60], far away the requirements of IDM.

Signal Frequencies	Dielectric Constant (Dk)	Loss Tangent (Df)
100 MHz	3.72	0.0072
1 GHz	3.69	0.0091
2 GHz	3.68	0.0092
5 GHz	3.64	0.0098
10 GHz	3.65	0.0095

Table 5.10. The Isola FR408HR properties in relation to the frequency of the signals.

Working with HDI technology forces us to work with a specific set of microvias and standard vias. The HDI basic design is made out of a Core with possible metalized vias in it, representing the L3-L8 in this design. Once the core is prepared, layers are added on top and bottom of the core one by one and the laser drilling is performed each time a layer is added. Once the design is finished the final top to bottom through vias are drilled. This derives in only 7 possible different vias represented on the Table 5.11.

Layer	Via Type	Minimum Size	Considerations
TOP-L1	Micro Via	75 um (ratio 8:10)	Via in Pad 150um
L1-L2	Micro Via	75 um (ratio 8:10)	
L2-L9	Buried Via	200 um	
L9-L10	Micro Via	75 um (ratio 8:10)	
L10-BOTTOM	Micro Via	75 um (ratio 8:10)	
TOP-BOTTOM	Through	250 um	
TOP-BOTTOM NP	Through non-plated	250 um	

Table 5.11. The possible type of vias for IDM prototype and size limitations.

5.3.2 Differential line design

The differential lines are separated on High Speed Lines (HSL), Mid Speed Lines (MSL) and Low Speed Lines (LSL) as defined on 5.2.2. The HSL are routed with priority over the dual striplines (dual TEM transmission lines routed between inner GND planes) in inner layers L2 and L9, both placed between the two upper GND planes and the two bottom GND planes respectively. All the lines, HSL, MSL and LSL, require a 100 Ω differential impedance. For the L2 and L9 striplines, calculations result in 125 µm trace width and 136 µm trace separation. The results of the calculations, done using the Cadence Software, can be found in Fig. 5.13. This result provides an impedance of 100.08 Ω, which is within the tolerances. For the TOP and BOTTOM layers, the dual microstrip (dual TEM transmission lines routed between air and GND planes) traces are 145 µm width and with 125 µm trace separation.

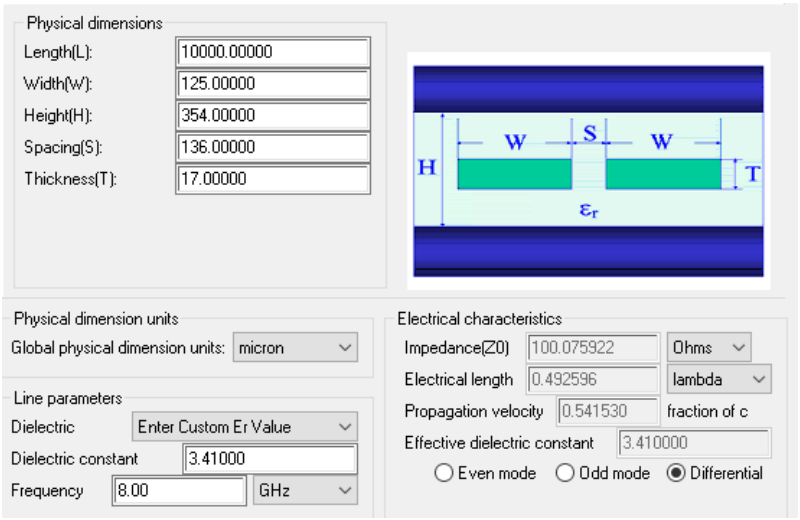

Fig. 5.13. Microstrip space and width values calculations for L2 and L9 for the selected stack up configuration.

This HSL lines have been designed with continuous impedance analysis and all the lines included the possibility to add a capacitor for AC coupling if needed. In the standard production a 0 Ω resistance is mounted because AC coupling is not needed for the motherboard FPGA connection. The calculated phase difference between non-inverted and inverted lines has been fixed at a maximum of 1 ps, and the maximum skew between different lines has been set to 10 ps. The total electrical length of all lines is fixed to 325 ps.

To avoid crosstalk, each line has a separation to the adjacent of a minimum of 1.2 mm and traces are routed at 90 degrees between layers in the case of crossing, see an example in Fig. 5.14. More information about the crosstalk analysis can be found in section 5.4.

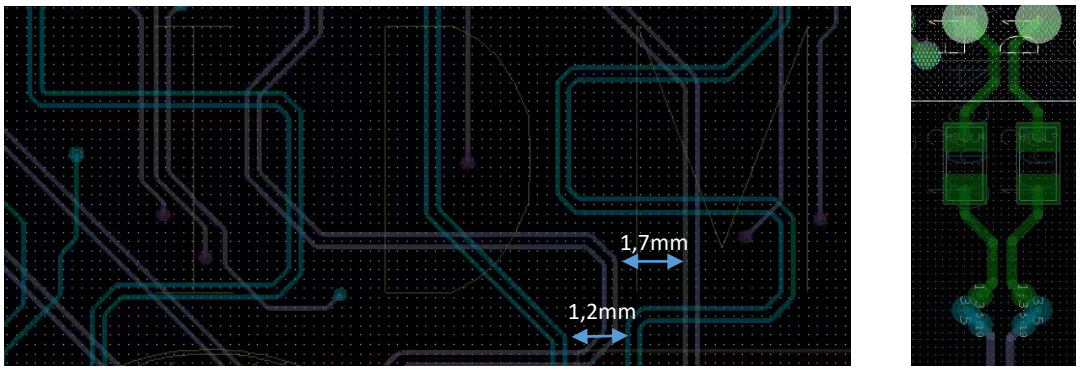

Fig. 5.14. ***Left****: Some of the HSL lines layout with the minimum separation between lines.* ***Right****: Output from the Top TLK10022 differential line to the L2 microvia bridge and the 0 Ohm resistor*

The microvia bridge from the TOP layer to the signal layer is done in a rhombic design with successive microvia steps, represented in Fig. 5.15.

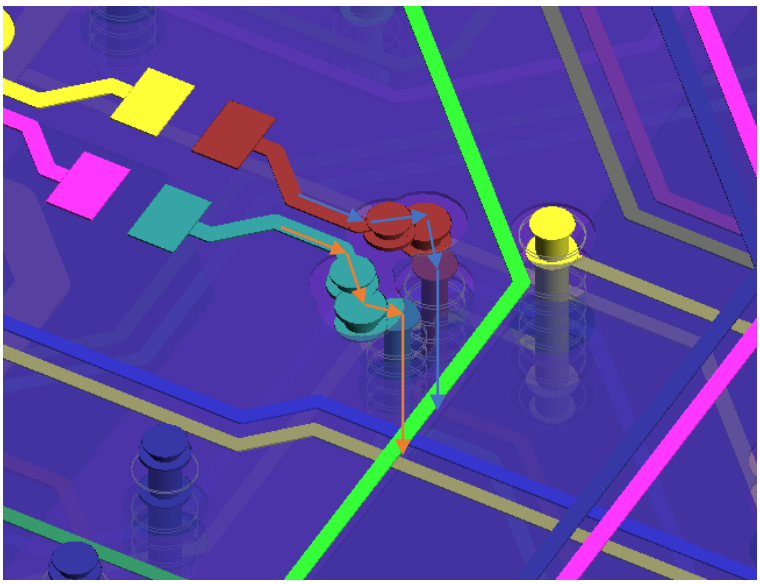

Fig. 5.15. Analysis of the Microvia rhombic bridge.

The placement of the components and the HSL connection lines to the FMC connector has been reordered to minimize the number of crossings between them. Table 5.12 shows the full interconnection path from the IDM input to the FPGA in term of routing layers.

IDM											
IC4 - Input 4	DOUT0-3	NC									
	DOUT4-7	NC				FMC	SOM - FPGA - TE0808 / XCZU15EG-1FFVC900E				Firmware
	DOUT8-11	INA	IC10 - TLK4	OUTA	HSL 9	DP1	228_1	X1Y5	R2/R1	FPGA X1Y1	Rx1
IC3 - Input 3	DOUT0-3	INB		OUTB	HSL 8	DP9	230_1	X1Y13	C4/C3	FPGA X1Y3	Rx9
	DOUT4-7	INA	IC9 - TLK3	OUTA	HSL 7	DP0	228_0	X1Y4	R4/R3	FPGA X1Y1	Rx0
	DOUT8-11	INB		OUTB	HSL 6	DP2	228_2	X1Y6	M2/M1		Rx2
IC2 - Input 2	DOUT0-3	INA	IC8 - TLK2	OUTA	HSL 5	DP8	230_0	X1Y12	D2/D1	FPGA X1Y3	Rx8
	DOUT4-7	INB		OUTB	HSL 4	DP3	228_3	X1Y7	L4/L3	FPGA X1Y1	Rx3
	DOUT8-11	INA	IC7 - TLK1	OUTA	HSL 3	DP7	229_3	X1Y11	F2/F1	FPGA X1Y2	Rx7
IC1 - Input 1	DOUT0-3	INB		OUTB	HSL 2	DP4	229_0	X1Y8	K2/K1		Rx4
	DOUT4-7	INA	IC6 - TLK 0	OUTA	HSL 1	DP6	229_2	X1Y10	G4/G3		Rx6
	DOUT8-11	INB		OUTB	HSL 0	DP5	229_1	X1Y9	H2/H1		Rx5
IDM						FMC	SOM - FPGA - TE0808 / XCZU15EG-1FFVC900E				Firmware

Table 5.12. Full interconnection path from the Optical input to the FMC output.

The MSL lines from the Optical input to the TLK10022 are routed on the TOP and BOTTOM layers with microstrip traces and on the L2, L9 layers as striplines. The traces are designed with a calculated phase difference, between non-inverting and inverting, signals of less than 5 ps and the propagation delay is adjusted to 490 ps for all traces. As the striplines have slower propagation speed than microstrips, there is a mixed use of the inner and outer layers per line. Furthermore, when required, delay lines were added to fit to the propagation time.

5.3.3 Synchronous clock networks

On the clocking system all the lines are LSL. In this system, the most critical part is clock synchronicity from the clock fanout to all the TLK10022 aggregators. These traces are all routed with a calculated 0.4 ns fixed delay and less than 0.3 ps phase difference. All must be AC coupled with a capacitor and with a 100 Ω termination resistor.

5.4 Mechanical, Power and High Speed analysis.

5.4.1 Power analysis.

The power supply design has been validated with simulations. All the power distribution network, shown in Fig. 5.16, has been completely simulated in the LTspice environment from Analog Devices. The simulation results show that the output voltages are stable. The 1.5V has a forced smooth delayed start to delay the 1 V start from the rest of the system.

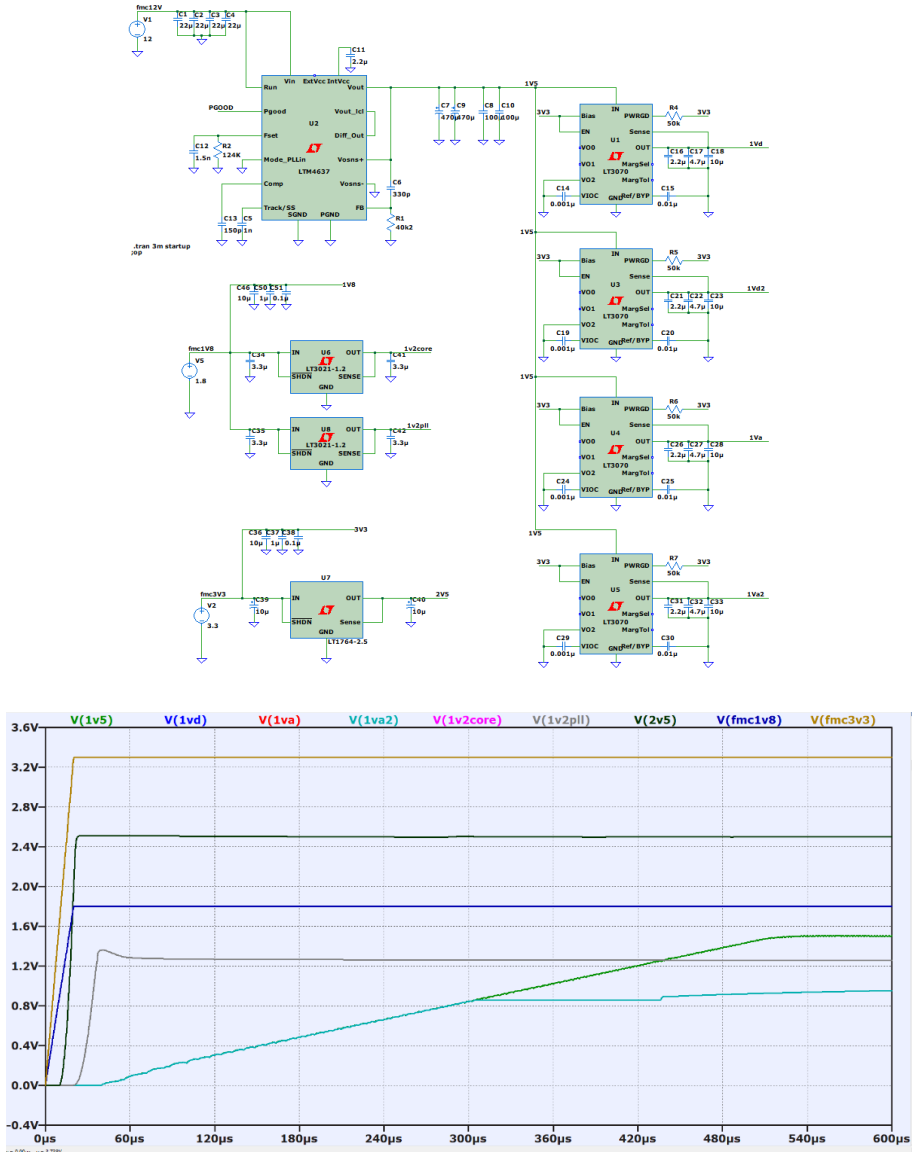

Fig. 5.16. The IDM power simulation schematic and plot, the first 7 are the generated supplies, the resting are from taken from the FMC connector.

The Fig. 5.16 shows the simulation result of the power-on sequence of the system. The first four voltages set on are the four TLK10022 1V inputs; next, the FPGA ICE40 1.2V input core and PLL are switched on; the last one of the generated supplies is for the crosspoint switch, the fanout of the clock system and the optical transceiver. The fmc1v8 and fmc3v3 (see Table 5.9) correspond to the FMC power inputs as defined in the of Vita 57.1 specifications. The 12V power supply is not shown.

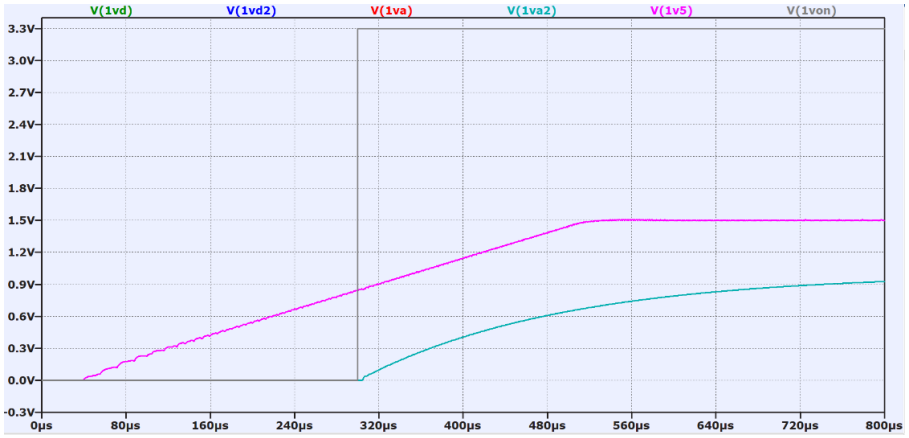

Fig. 5.17. Example of the power on system with a delay of 300 us and soft start.

The LT3070 has a power-on enable input controlled through the IO expander that is simulated in Fig. 5.17. This is done to fit to the FMC standard that requires a minimum delay of the power drain. The only element powered-on at start is the FPGA, that requires the 1.2V voltage from the beginning. The 3.3V and 2.5V will never be used until the Optical transceiver or the Clock system are enabled.

5.4.2 Mechanical simulation

In order to check the final placement of the IDM board, inside the digitizer box mechanics of Phase 2 electronics, it is useful to have a 3D design of the board. For this purpose, a Step model with the assembled components was compiled. Fig. 5.18 shows the mechanical 3D model.

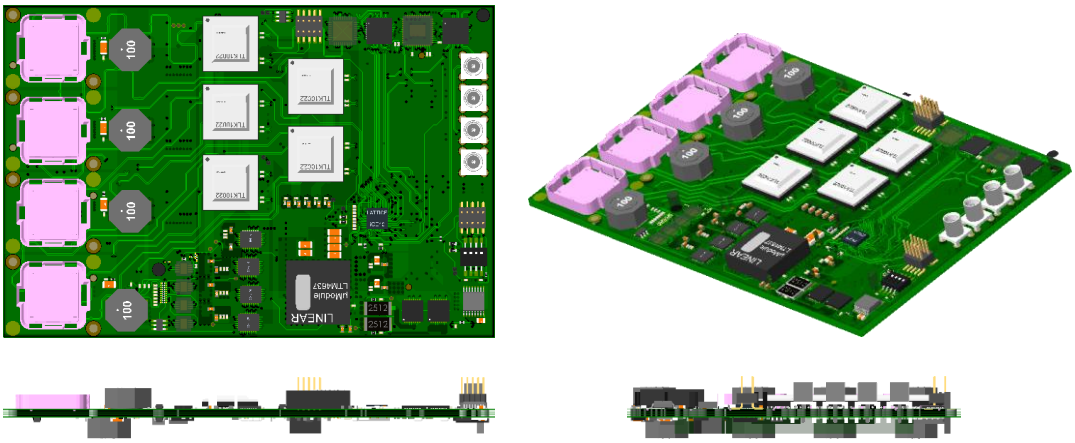

Fig. 5.18. The step 3D mechanical model of IDM.

This model has been also used to test the mechanical of the IDM in the evaluation board, as this board is not compliant with all the dimension specified in Vita 57.1.

5.4.3 High speed analysis.

For all of the differential traces, the impedance, phase and continuous impedance is calculated in parallel with the routing of the lines. This is done by the combination of Cadence Alegro software and Cadence Sigrity SI. In this way, it is possible to route the board properly since the beginning avoiding iterations with high time cost simulations. The simulations confirmed that the previously calculated dimension for the stripline and microstrips were correct, as shown in Table 5.13. In the column labelled "Typ Diff Impedance" (Typical Differential Impedance) we can see that the mean impedance values are around 100 Ω with a 1.5% maximum of deviation in Min and Max Diff Impedance (Maximum and Minimum Differential Impedance), which is within the acceptable values for this type of differential lines. It also confirms that there are no crosstalk aggressors for the HSL and MSL lines.

Net count	Net name	No. of vias	Max Diff Impedance(Ohm)	Max Diff Impedance Length(%)	Typ Diff Impedance(Ohm)	Typ Diff Impedance Length(%)	Min Diff Impedance(Ohm)	Min Diff Impedance Length(%)
52	MSL_0_0_P / M...	2 / 2	99.4	21.61	98.7	47.02	98.7	47.02
53	MSL_0_1_P / M...	0 / 0	102.8	0.24	98.7	56.94	98.7	56.94
54	MSL_0_2_P / M...	2 / 2	100.2	87.06	100.2	87.06	98.6	3.14
55	MSL_0_3_P / M...	2 / 2	99.3	8.06	98.7	66.47	98.7	66.47
56	MSL_0_4_P / M...	3 / 3	100.2	24.78	98.7	30.76	98.7	30.76
57	MSL_0_5_P / M...	2 / 2	100.2	93.65	100.2	93.65	100.2	93.65
58	MSL_0_6_P / M...	6 / 6	100.2	42.77	100.2	42.77	98.6	2.37
59	MSL_0_7_P / M...	0 / 0	99.4	33.35	98.7	49.92	98.7	49.92
60	MSL_0_8_P / M...	2 / 2	100.2	83.17	100.2	83.17	98.6	7.87
61	MSL_0_9_P / M...	2 / 2	100.2	88.63	100.2	88.63	98.6	4.61
62	MSL_0_10_P / ...	4 / 4	100.2	56.51	100.2	56.51	98.6	33.42
63	MSL_0_11_P / ...	4 / 4	101.5	0.29	100.2	33.64	98.6	0.35

Table 5.13. excerpt of the Sigrity SI report with the table of the differential impedance variations for some of the MSL lines.

After the routing of the full board, the high speed signals are simulated using the extracted S-parameters of the traces and generating a known stimulus. This task is done with the Cadence Sigrity PowerSI software.

For some of the critical HSL also a 3D EM simulation was done with the same software. The 3D elements extracted are shown in Fig. 5.19 where the specific delay (serpentine) to match all HSL can be noticed in the middle part of the trace. The critical parts to measure are also in the figure with the rhombic microvia, the resistor bridge and the ball soldering at the beginning of the trace.

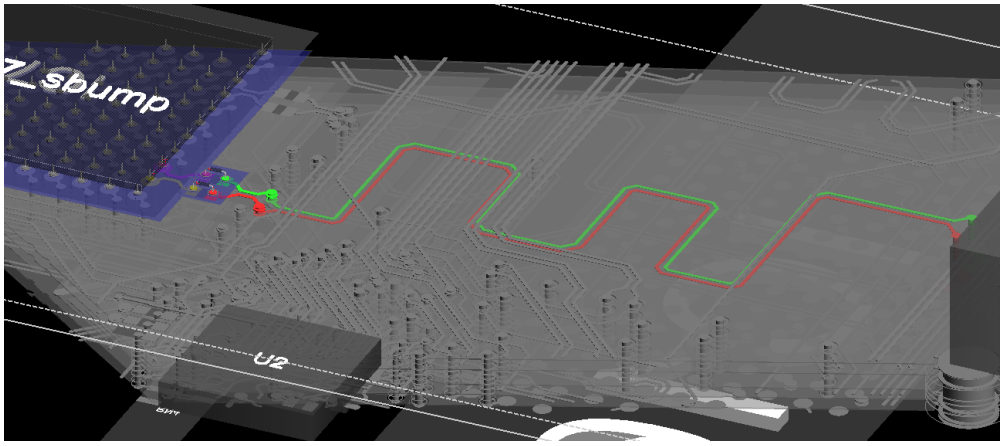

Fig. 5.19. The selected differential line HSL_4 (Fig. 5.4) for 3D EM simulation with its environment.

The 3D EM simulates the frequency response of the traces using the extracted S-parameters, returning a differential impedance value of about 115.8 ohm at 2 GHz and about 97.5 ohm for 8 GHz. Also the reflection coefficient and the transmission of the differential traces are calculated.

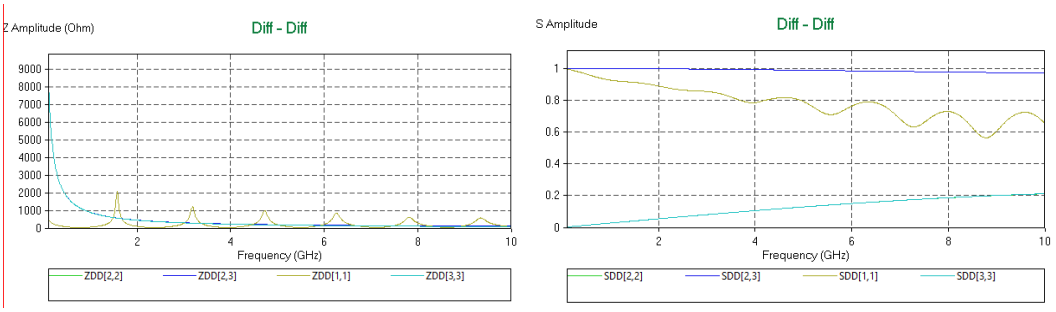

*Fig. 5.20. **Left**: Calculated impedance of HSL_4 with 3D Electromagnetic simulation. **Right**: The S parameters of HSL_4 in 3D EM simulation.*

Fig. 5.20 show the simulation results for the SDD[2,2]/SDD[2,3] ratio that measure the reflection coefficient (R) for differential signals. The value of this coefficient at frequencies of 8 GHz and 2 GHz are R = 0.182/0.976 = 0.19 (19%) and R = 0.054/0.996 = 0.05 (5%) respectively. The transmission coefficient is calculated from the ratio SDD[1,1]/SDD[2,3] and its value is of T = 0.75 at 8 GHz and T = 0.85 at 2 GHz.

5.5 Layout and prototype production

5.5.1 Layout

In addition to the difficulties to design properly the differential lines, discussed on previous sections, the design of the layout of the IDM has several critical parts. The ICE40LP is a FPGA in an 81 pins µBGA package with 0.4 mm pitch. To locate this device in the design, laser microvias from HDI have to be created in the same soldering pads. The present technology allows to build vias with a minimum diameter of 75 µm, in a 150 µm pad, small enough to avoid the common via-in-pad soldering problems.

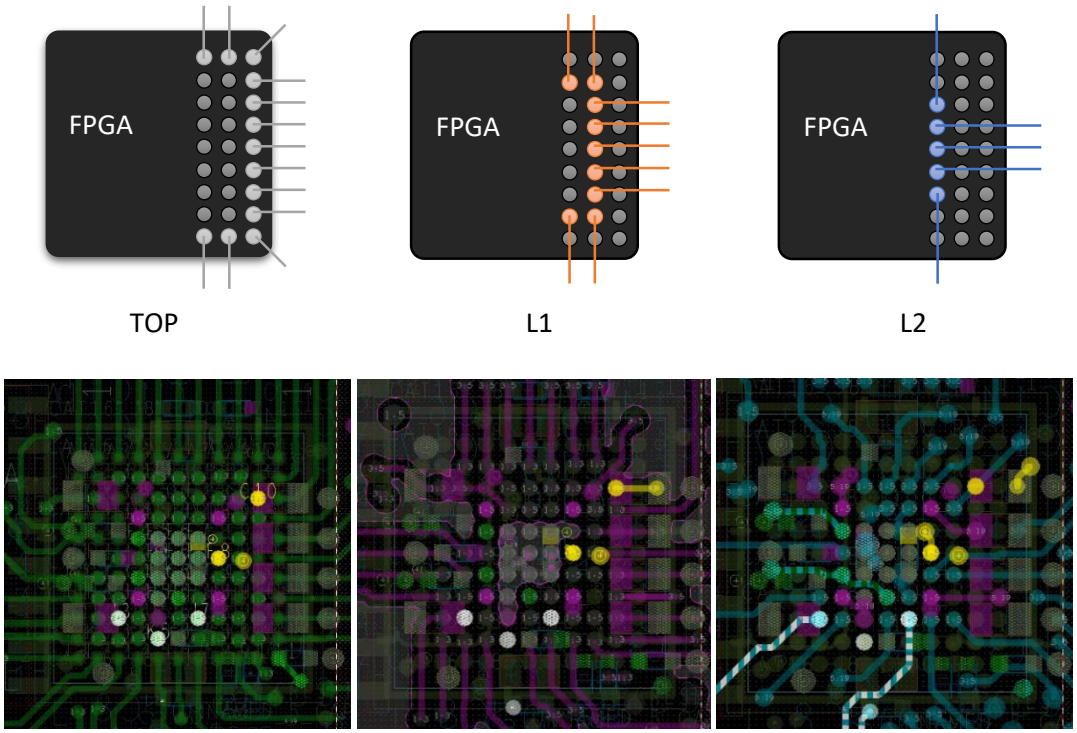

Fig. 5.21. The TOP, L1 and L2 of the IDM in the FPGA area, on the top we find the recommended layout on the bottom the final design.

The FPGA manufacturer provides a recommended output layout, described in a layer by layer basis, to extract all signals, shown in Fig. 5.21. The layout is done starting from the outer signals through the TOP layer of the board and placing one microvia per layer for each row/column towards the centre of the integrated circuit. In this way the second row/column of pins will be extracted through layer L1 and the third through L2 and

so on. The inner pins of the FPGA are the power ones, so they are directly connected to their voltage planes using the inner blind vias.

All the components with a high profile are placed on the TOP layer of the board because the BOTTOM layer of the board has a maximum free space of 1 cm due to the FMC connector height. This forces to place the Optical connectors, the programing and PRBS pins and MCX connectors on TOP layer. This 1 cm spacing constraint affects also to the high thermal dissipation elements such as link aggregators, PLL, clocking distribution and DC-DC converters, that are also placed on TOP layer. The decoupling capacitors for TLK10022, PLL and FPGA are placed on the BOTTOM layer of the board and side by side with their related power supply pins.

5.5.2 Manufacture and prototype productions

The production of the PCB was carried by Cipsa Circuits using HDI technology. In the first run (IDM v1.1) 6 PCB were produced, but only two of them were mounted by Rompal Ingenieros. The first test of the boards discovered an FPGA power problem and a clock network bad connection. The board was then used as a system for slow control test. All devices mounted were tested through an I2C external interface. The found problems were corrected on the new version of the IDM prototype, called v1.2, and two new boards were fully produced, an image of the produced IDM prototype board is shown in Fig. 5.22.

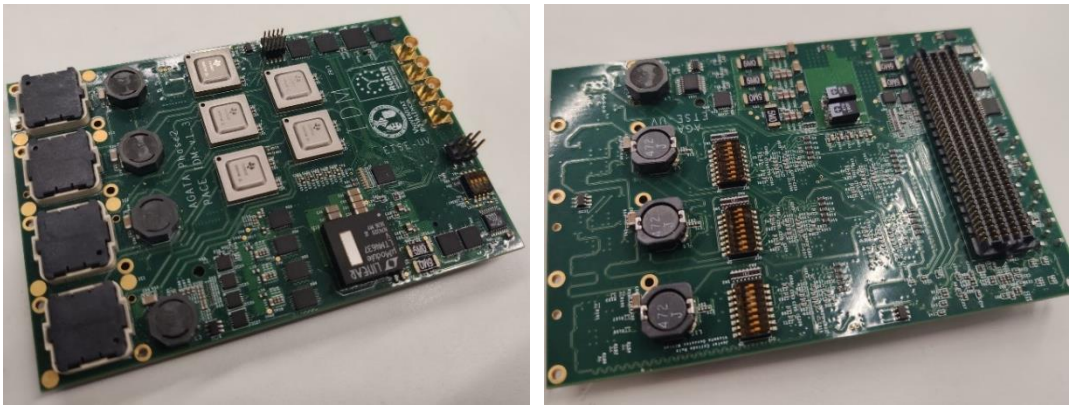

Fig. 5.22. The IDM prototype v1.2, TOP and BOTTOM view respectively.

The full process of production lasted about 4 months due to several mounting problems of some elements. The testing of the second board revealed a problem with a power supply on an unknown element over the VDDT 1 V power for both boards. This problem was investigated and resulted in an internal shortcut in one of the TLK chips. The removal of the IC solved the issue and allowed to continue with the tests described in Chapter 6.

The prototype production costs were 1420 € for mounting 2 boards, 2360 € for the PCB production for 2 boards and 570 € for component procurement. The final cost for the prototype is 2460 €/unit, mainly due to HDI initial costs that are diluted on higher production numbers.

The cost of producing 10 PCB boards will be less than 3000 € and the component mounting of more than 10 board will be over 60 € per unit. Probably, the component cost itself could be reduced about a 30 % but this is not included on the calculations. The final cost per 10 units would be around 9000 €; 900 € per unit is within the calculated budget without taking into account the cost reduction if the optical transceivers are finally not used. The higher cost components are the five TLK10022 with ~40€ per element, the four Optical transceiver sockets with 25 € per element and the 12 V DC-DC converter about 40 € each. The TLK10022 are a key element part, but for the socket and the DC-DC, compatible components with lower cost can be considered.

Chapter 6:
Test and validation.

6.1 Preliminary tests

6.1.1 Test for IDM v1.2

The IDM board prototype arrived on March 2017. The first test carried out was to check all the voltages traces in the power supply section looking for shortcuts. On the IDM v1.0, the 12V to 1.5V DC-DC converter was mounted rotated 90° clockwise with respect to its proper position, resulting in a shortcut of the 12V power plane. The board was sent to the assembly company again to correct this mistake.

After the correction, the IDM prototype passed the shortcut test of the main power supplies so it was powered-on to verify voltages. The board had also a malfunction in the FPGA due to a problem in the 2.5 V power pin of the non-volatile memory. Nevertheless, to minimize the possible issues on the next production, several tests were done on the board. The serial lines were connected to an external microprocessor and all the devices, except the TLK10022, were read through the Two Wire Interface. This test revealed a second issue located on the clocking system: the connection of the input clock for the IDM prototype on the FMC connector didn't have the corresponding connection on the evaluation board used to test the board.

The clock system was redesigned to include a second input from the FMC to provide two possibilities compatible with the evaluation board carrier. The new design solved some minor issues in the FPGA programming connections and the 2.5 V problem for the FPGA. This new version, called IDM prototype v1.3, was sent to prototype production on mid-2017.

6.1.2 Test for IDM v1.3

This second prototype of the IDM was received beginning of 2018. Unfortunately, it came with the same mounting problem and had to be sent back to the assembly company to rotate 90° again the DC-DC converter. Once connected, it showed up a shortcut on the 1V for the analogue input of the TLK10022 transceivers. After hard effort tracking the

problem, a shortcut in one of the aggregator was found. This component was replaced and the board started to power on properly by mid-2019.

After the powering the board, all voltages values were correct. The Lattice ICE40 FPGA was programmed and the evaluation board communicated to the FPGA with the TWI. All the components were correctly addressed from the ICE40 and programmed; the clock system was programmed to receive the 200 MHz clock and the TLK10022s serial PLLs were locked.

6.2 The data receiver firmware system for CAP-PACE

6.2.1 The CAP Pre-processing firmware description.

The Pre-processing firmware for the PACE system of AGATA Phase 2.0 is written in HDL code (Verilog and VHDL) for the Xilinx Zynq Ultrascale XCZU15EG on the TE0808 SOM module. This firmware can be separated in conceptual working blocks as presented on Fig. 6.1.

Following the data flow, the first part is dedicated to receive data from the Digitizer ADCs and align it. The next block is the triggering system that sends a trigger request signal to the GTS system if a core signal pulse is identified. This block is implemented as a digital constant fraction discriminator (CFD) or a triangular discriminator both with a trigger threshold value. When a trigger is fired, while waiting for the Validation/Rejection response from the GTS, the system continues recording the traces.

The traces on the current electronics are recorded using 100 samples for each of the 38 digitizer channels in the case of a trigger. This value could be increased in Phase 2 and is a critical part of the data bandwidth because 100 samples, 16-bit each, acquired at the maximum specification rate of 50 KHz and for 38 channels of the digitizer, represent an aggregated data bandwidth of 3 Gbps. In general, the data bandwidth increases approximately in 1 Gbps for each additional 35 samples. Furthermore, the energy, timestamp and event number has to be added to this bandwidth. Nevertheless, one 10 Gbps Ethernet link is capable of retrieving all the data even multiplying by 2 the number of samples per channel. There is, however, another factor to take into account that may limit

the maximum data acquisition bandwidth that it is the input bandwidth in the PSA and acquisition computer farms.

In addition to the standard acquisition traces, long traces or even continuous sampling of several parts of the Pre-processing data flow can also be recorded and sent to the monitoring system for debugging or further analysis. For these cases, a dedicated 10 Gbps Ethernet link is reserved.

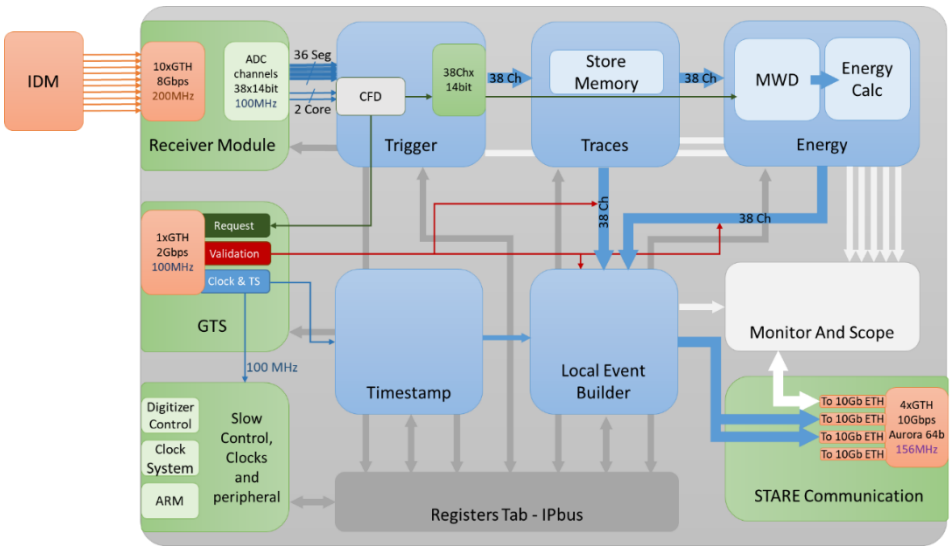

Fig. 6.1. The Phase 2.0 PACE SOM Firmware blocks for AGATA Pre-processing.

If the GTS trigger processor validates the event, the stored traces, the Energy calculated with the Moving Window Deconvolution and the event timestamp and identifiers, are sent via the 10 Gbps Ethernet to the PSA server farm. The data sent is packed in a specific format with all the channels, timestamp, energy and other required data on the Local Event Builder. This packaged data is sent through STARE to the Ethernet network, where it is distributed to the machines in the processing farm to perform PSA.

The PSA computation is the last processing that is performed at the detector level (local level). After the PSA, all the processed and validated data, belonging to one event, is joined together by the Event Builder, merged with data provided by complementary instrumentation, if existing, in the Event Merger and finally sent forward for storage or on-

line analysis. The GTS is distributing the timestamp which is used to join different detector data using the event builder.

External to the dataflow, the rest of firmware blocks are the Slow Control, the Clock Control and the Peripheral Connections. The Slow Control takes care of the communication to the digitizers, IDM and PACE board devices, with initializations and automatized tasks programmed. The Clock Control is responsible of the GTS clock distribution, and the management of the derived clocks, with the GTS proper external delay lines control. The Peripheral block includes the Ethernet link for the IPBus, connectivity to the quad core processor available inside de FPGA that can be used in automation, the USB connection and other extra devices.

The FPGA Zynq Ultrascale were firmware is implemented has an ARM Cortex-A52 quad core processor and a two core Cortex-M4 microcontroller. On this processing unit, called Processing System (PS) in Xilinx documentation, an embedded Linux operative system can be installed. This could be useful as an automation tool for slow control, initialization or maintenance, therefore, a link to the PS to Pre-processing FPGA fabric is foreseen on the firmware.

The receiver module, which has been developed in the context of this work, for the testbench system and the future Phase 2 PACE board, is described in the next section.

6.2.2 The receiver module

The receiver module duty is to serve the 38 channel data from the ADCs synchronously in 14-bit wide words at the 100 MHz common Pre-processing clock domain. This is achieved through several modules performing each one of the required tasks: deserialization of the aggregated data of ten input lines at 8 Gbps, the 8b/10b decoding, the reordering of the data to reconstruct the 38 ADC channels, the JESD204 data and synchronization layer per line and the elastic buffer together with the sync pattern detector. The complete receiver module is depicted in the Fig. 6.2.

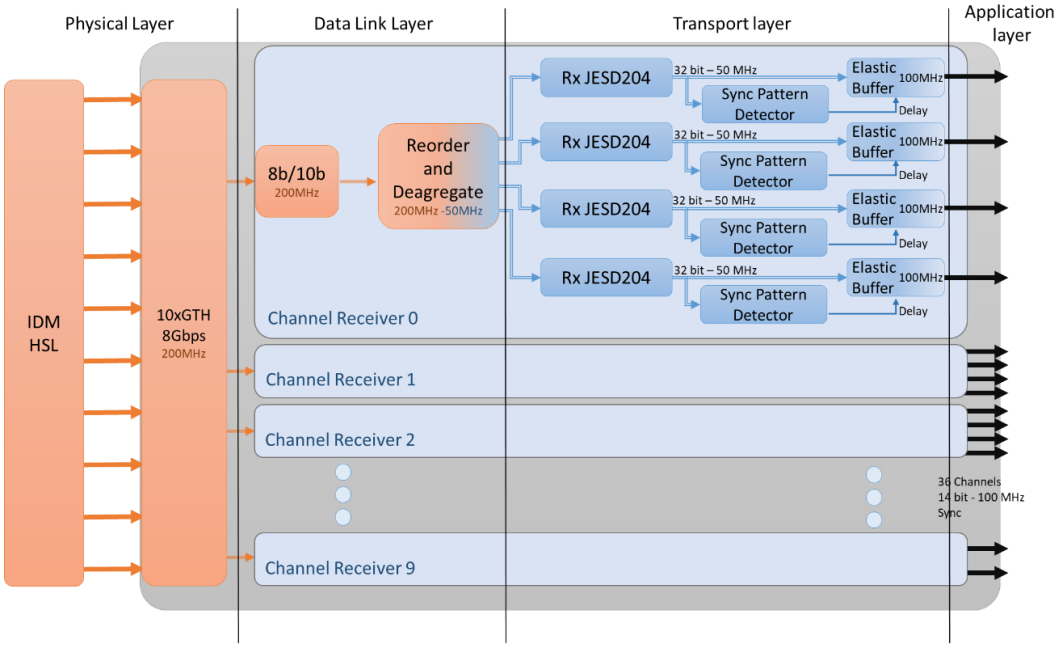

Fig. 6.2. The PACE firmware receiver module. The clock domains are referenced with different colours, red is the 200 MHz from link aggregator, blue is the 50 MHz for the JESD204 decoding and black is the 100 MHz common reference clock.

Speaking on ISO/OSI layers, the Link Aggregator TLK10022 only affects the Data Link layer or lowers. The physical layer on the original JESD204 coming from the ADCs, in a differential Current Mode Logic (CML) output format, is transformed to an optical line and back to a CML in case of Optical transceivers. In case of using a copper connection, it is directly connected to the TLK10022. This is properly adapted from the IDM board so, in any case, the TLK10022 receivers are compatible.

As already discussed in Chapter 5, the CML Link Aggregator outputs are also adapted to the motherboard FPGA Rx transceivers with a 0.7 V common voltage using an AC-coupled 100 Ω termination as the TLK10022 datasheet suggests [104]. The reception of the data is performed in the Xilinx Transceiver of the FPGA. This module also performs the deserialization of the 8 Gbps data to the local reference clock and the data clock recovery (CDR). The data is served to the firmware in fabric as a 40-bit word at 200 MHz local clock.

Data link and transport layers

The input data link format is the JESD204, with a slight modification, introduced by the TLK10022, that is reversed before applying the JESD204 decoder. The JESD204 has several parameters that define the link. Each JESD204 link of the AGATA digitizer communicates only one data channel. This data comprises K=9 frames in each multiframe, F=2 octets in each frame with 8 bits each. Each frame transports one 14-bit data sample from ADC, the two remaining bits are non-relevant data.

Regarding the ADC, there are two lanes per device (L=2) and two converters per device (M=2), codifying one sample per frame (S=1). The two octets of a frame are sent in 20 bit and at 100 MHz sample in a 2 Gbps line.

The 8b/10b encoding is designed to codify the 8-bit data into a 10-bit word with a maximum parity of ±2, which means that the number of ones respect to number of zeros is less than 2. To ensure disparity between octets, if an octet has a disparity of -2, next octet must be sent with disparity +2 and vice versa; if the parity is 0 nothing changes. For this reason, there are two encoding tables, one for previous octet parity +2/0 and another from -2/0. Mixing all this up, it results in 256 data values per 10 bit symbol from D0.0 to D31.7 and 12 especial symbols used for communication from K28.0 to K28.7, K23.7, K27.7, K29.7 and K30.7 [108]. This task is performed by the 8b/10b module represented in Fig. 6.2 and in hardware it is a part of the Xilinx FPGA transceiver. It performs a reduction from the 40 bit to 32-bit data and several signals to mark the incoming data as symbol, data or disparity error.

The TLK10022 contributes to the link layer only to mark the Lane 0 for the 4 aggregated lines and the 1:4 combinations. To determine which of the four incoming octets is the lane 0, 1, 2 or 3, it marks lane 0 by substituting of one of the K characters used commonly on the link layer by an unused one. The JESD204 link layer is based on the K28.5 (0xBC) or /K/ symbol from Table 6.1 [109]. This symbol is sent continuously from the JESD204 Tx until the octet is aligned in what is called the Code Group Synchronization (CGS).

The aim of this K28.5 symbol is the 4 octet line alignment on the GTH Rx, as a comma to stablish the position of the Bit0 for the 40 bit-wide deserializer, with the help of the recovered clock (CDR). Once the GTH Rx is aligned to the incoming DataStream from the Link Aggregator, the Line 0 alignment starts. The TLK10022 is programmed to change the K28.5 characters to the unused K23.7 symbol only on channel 0. If this symbol is detected, the Reorder and De-aggregate (RaD) block aligns the selected octet as the first one and labels the rest of them as channel 1, 2 and 3 in increasing order. After this, the K23.7 symbol of channel 0 is changed to K25.8 for the next step on the JESD204 Rx Core and the link alignment of the four channels start in the CGS stage.

Control Character	Control Symbol	8-bit Value 3b/5b	10-bit value, RD=-1	10-bit value, RD=+1	Description
/R/	K28.0	000 11100	00111110100	11000001011	Start of Multiframe
/A/	K28.3	011 11100	00111110011	11000001100	Lane Alignment
/Q/	K28.4	100 11100	00111110010	11000001101	Start of Link Conf. Data
/K/	K28.5	101 11100	00111111010	11000000101	Group Synchronization
/F/	K28.7	111 11100	00111111000	11000000111	Frame Alignment

Table 6.1. JESD204 special characters meaning and values. The 10bit RD=-1 and RD+1 corresponds to the table with previous polarity -2 and +2 respectively.

The decoding of the JESD protocol is done by the Xilinx JESD204 Core block [110]. This block needs an 8b/10b decoded sequence in a frequency of 1/40 of the input data rate. For that reason, a double clock FIFO is implemented at the end of the RaD block to change the input frequency to the 50 MHz JESD204 Core clock domain. At the same time, 8 bit words change to 32 bit words in the clock domain change. After the CGS is finished, the SYNC signal is deasserted to indicate the ADC that the link is stablished and to start with the Initial Lane Alignment Sequence (ILAS). This SYNC signal has to be connected from the FPGA motherboard to the digitizers. If any problem arises with the parity of the data, in the ILAS procedure or in the synchronization, the SYNC signal is asserted and the digitizers start to send the CGS again.

The 8b/10b /K/ symbols are used by the JESD204 on the transport layer to understand when the octets, frame and multiframes start. For the ILAS sequence, a series of 4 multi frames is sent with the link configuration data. If this configuration matches the expected one, then the ADC starts sending data. The full data pattern is represented in Fig. 6.3.

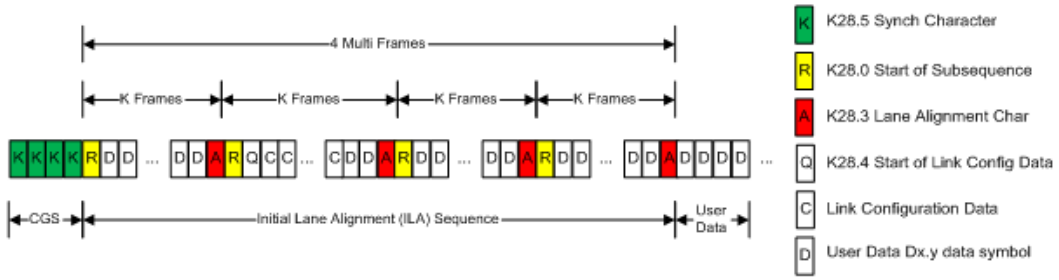

Fig. 6.3. Representation of the JESD204 pattern for CGS, ILAS and User Data. On the AGATA case the K would be 9 frames.

The output data of the JESD204 block gives the data in 32-bit word, separated by four octets, and a signal marking which octet is the first of the frame and which is the first of a multiframe. This has to be translated into two 16-bit words and with two possibilities: either the frame starts from octet 0 and 2 or it starts from 1 and 3. This data is reordered before sending it to the Sync Pattern and Elastic Buffer blocks.

The elastic buffers and data output to Pre-processing

One of the most important requirements of the AGATA detector is the timing and synchronization of the different segment and core signals. It is critical to align all the signals at the same time reference. The digitizers have a stochastic latency that depends on various uncontrolled factors, such as when they are powered-on or when the transceiver transmission/reception starts. This latency is different in each ADC, so the data has to be aligned. The signal backplane connecting all the Digit-Op12 board and the Digit-Opt12 boards themselves are designed to send a Sync Pattern signal with minimum delay differences. In the Phase 1 electronics this synchronization pattern was generated by the Control Card but in Phase 2 electronics it will be done through the PACE board itself.

To synchronize the ADCs, a pulse train signal is sent through the Sync Pattern connection and, this signal, is recognized in the Sync Pattern Detector block. Once the signal is recognized in one channel, a 100 MHz counter on each Sync Pattern Detector starts, rising as well flags indicating the detection of the pulse train signal. The counter for all the Sync Pattern Detectors will stop when the 38 lines, corresponding to the 38 channels read, detected flags are on. The value of the counters will be added to a fixed value selected by the user from an external register, to fix the latency to a defined value. If the register value is zero, minimum latency is ensured.

The total latency calculated for each channel is applied to its respective Elastic Buffer. The Elastic Buffer FIFOs will also change the clock domain from the 50 MHz JESD204 cores clock to the 100 MHz common clock domain. The output of the Elastic Buffer are 38 synchronous channels of 14bit each at 100 MHz.

6.2.3 Other Firmware modules

The rest of the firmware, excluding the STARE Ethernet firmware and monitoring, is based on the previous generation HDL code. The firmware upgrading to the new FPGA for Phase 2 is in charge of IPHC (CNRS / Université de Strasbourg, France), consisting in Trace, Energy, Event Builder, Timestamp and GTS. It includes also the combination of the whole system register for IPBus control.

For the Monitor and Scope module, there is an improvement respect to older generations due to the 10 Gbps Ethernet specific link. It includes a scope mode to connect to each signal on the data path as inspection. The development of this module is assigned to STFC (Daresbury, UK).

The last block to mention is the STARE communication module to send data, that is a basic block based on Xilinx Aurora 64b/66b protocol IP. It is a four link full duplex interface that will send detector data and monitoring in formatted packages to the STARE SOM board. The STARE SOM board manages the communication of these data links with the Ethernet network. The STARE communication firmware block was developed together with CSNSM (Orsay, France) and ETSE-IFIC (Valencia, Spain) under the context of this thesis.

6.3 The IDM testbench

6.3.1 Testbench description

The test of the IDM prototype board and the development of the firmware has been carried out in several stages. Since the TE0808 SOM was not existing at the beginning of this development, on a first stage, the IDM prototype was installed on a HiTech Global K-800 board. This evaluation board includes a Kintex Ultrascale XKCU115 FPGA with more than 1.4 million of logic cells, 75 Mb in block rams and 64 16.3 Gbps transceivers [68]. The evaluation board also includes two clock generators, two HPC Mezzanine connectors, 2.5 GB of DDR4 memory and an 8x PCI-E v3 connection [111].

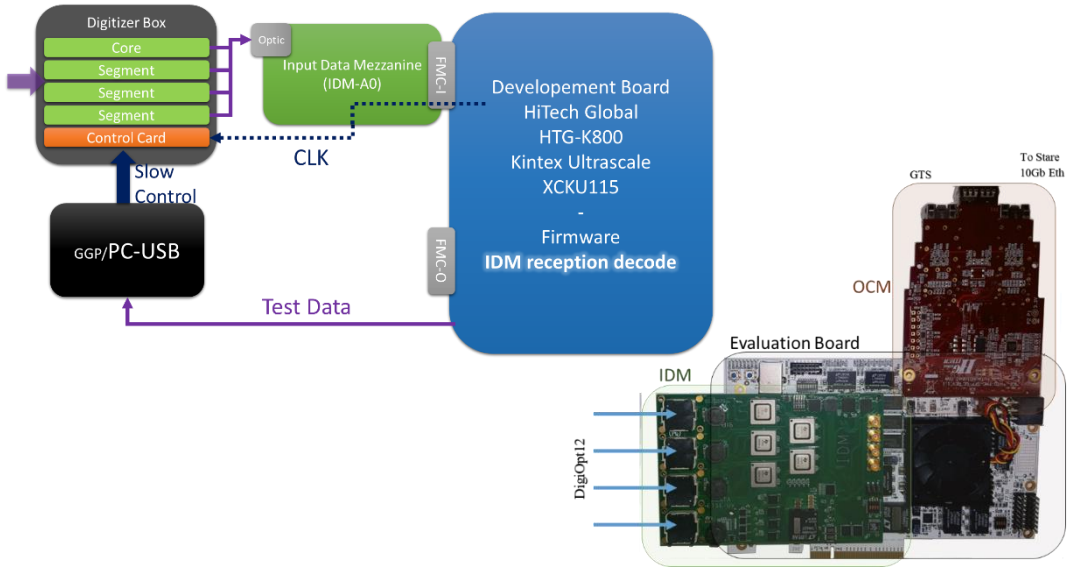

*Fig. 6.4. **Left**: The connection conceptual design of the K-800 IDM prototype testbench. **Right**: The connected IDM prototype and SFP+ output board to the K-800 evaluation board.*

This evaluation board has no capability to connect to the slow control and clock system of the Digi-Opt12. In order to do this, the Control Card from Phase 1 electronics was reprogramed to act as an interface between them. The power-on and control of Digi-Opt12 boards can be done through the Control Card USB connector, with the software described in Chapter 3, or with the GGP from Phase 1 electronics. The K-800 has no SMA outputs, so the SYNC~ signal from the JESD204 core had to be connected through a parallel female 2.55 mm pitch pin connector adaptor. The clock for the digitizer was extracted from the IDM prototype clocking system as depicted in Fig. 6.4.

The decision to move to a SOM-based solution, taken at the end of 2018, implied a change in the testbench evaluation board to fit the final version. The selected SOM board for the PACE testbench was the TE0808 model from Trenz Electronics with a Xilinx Zynq Ultrascale+ ZU15EG-1FFVC900E MPSoC (Multi-Processor System on Chip), 4 Gb of DDR4 memory and 20 transceivers routed to the motherboard. The Zynq device has two interconnected parts, one for programmable logic (PL) or FPGA and another for the ARM processor core, called processing system (PS). The PL contains approximately 750 k logic cells, 3500 DSP slices, 28 Mb of memory in blockrams and 16 GTH transceiver. On the PS side, it has 4 GTR transceiver, a quad-core ARM Cortex-A53 processor, a dual-core ARM Cortex R5 real time processor and a Mali 400 graphics unit [112].

To host the TE0808 the testbench includes a TEBF0808 from Trenz Electronics, an ATX form board with a HPC FMC connector, a dual socket for SFP+ and a Samtec FireFly connecting the 16 gigabit transceivers. There is also a PCI-E, a USB3 and a 1 Gbps Ethernet interfaces for the PS side of the MPSoC.

This board has a clock generator with a SMA connector output that will provide the Digi-Opt12 with the 100 MHz clock in the testbench. The Digi-Opt12, as in the previous testbench, is connected through the Control Card from the AGATA Phase 1 electronics. Another parallel female 2.55 mm pitch pin connector adaptor was built on this board to output the SYNC~ signal from the JESD204 link layer and the Sync Pattern signal for the Elastic Buffers.

The test-bench makes available three connections of the data paths:

A) from the Digi-Opt12 transceivers to the IDM prototype transceivers and Tlk10022,
B) from the TLK10022 to the motherboard FPGA
C) from the motherboard to the STARE 10 Gbps Ethernet (see Fig. 6.5).

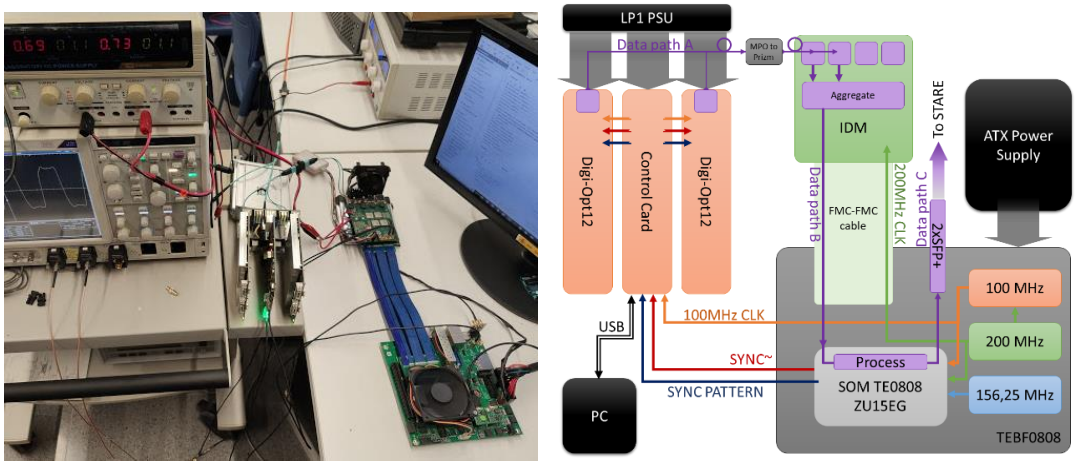

Fig. 6.5. ***Left****: Image of the testbench, at the bottom right it is placed the TEBF0808 evaluation board with the TE0808 Zynq, the blue FMC-FMC cable extension is connected to the board on one end and to the IDM on the other. The Digi-Opt12, the Control Card and its power supply are on the centre of the image.* ***Right****: Conceptual design of the IDM testbench, data path is represented on purple.*

There are five important clocks generated in the system: the main clock at 100 MHz for all the processing tasks and for the Digi-Opt12 ADC, the 200 MHz clock for the IDM prototype link aggregators, the 156.25 MHz clock for the Aurora link to the STARE, the 62.5 MHz clock for the Aurora DRP and the 50 MHz for JESD204 cores and for the data path B GTH transceiver DRP. The first one is generated from the motherboard clock generator, the next two clocks come from the SOM Clock generator since it has a low jitter and because of its proximity, and the last two are from the internal FPGA PLL. There is one more clock for the PS processors and is generated independently in the TEBF0808.

For debugging and control purposes, the ARM Cortex M5 processor has a server programmed with access to all the slow control, debug signals and data path, in combination with the Xilinx Vivado ILA and VIO analyser on the hardware manager software. The server is controlled through the UART serial connection of the MPSoC programming platform. A specific GUI has also been developed, for the control of this server, as shown in Fig. 6..

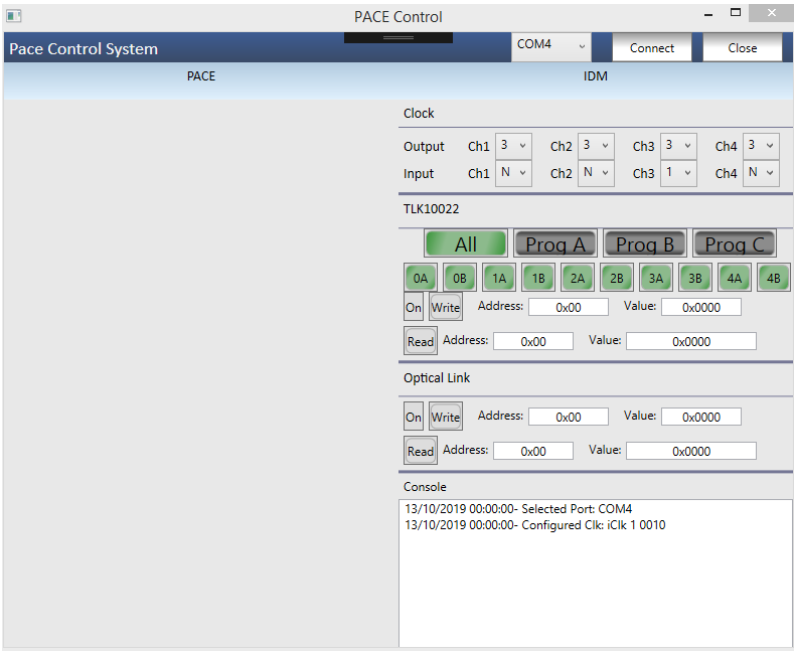

Fig. 6.6. The testbench Pace Control System software GUI on the IDM side. It has direct connection to the server on the SOM MPSoC and to the slow control lines.

The software developed initializes the PLL from the evaluation board and the SOM in order to generate the required clocks. It has different programs for the TLK device at each of the steps of the test-bench and it performs the control over the IDM prototype sensors, clock system and optical transceivers.

The IDM prototype validation focused on the data path A and B, meanwhile the proof-of-concept focused first on the data path C.

6.3.2 Verification of the data path.

To validate data path A, a pseudo random PRBS7 signal is generated from the ADC on the Digi-Opt12. This signal is received in the TLK that validates the PRBS7. There is also a test point (LOS) at the optical transceiver indicating whether there is an active optical signal. Table 6.2. shows the optical channel power and the LOS value for all the optical channels.

Channel	Transceiver 0		Transceiver 1	
	Op. Power (µW)	LOS	Op. Power (µW)	LOS
0	400,0	0	464,8	0
1	506,7	0	478,3	0
2	505,3	0	481,5	0
3	497,8	0	471,6	0
4	560,5	0	572,6	0
5	491,4	0	508,6	0
6	517,4	0	392,9	0
7	546,6	0	564,0	0
8	540,0	0	492,9	0
9	499,1	0	453,2	0
10	570,0	0	532,9	0
11	504,4	0	504,3	0

Table 6.2. Table of the MiniPod Rx Optical transceivers link, the LOS signal 0 indicates the link is stablished with the Tx device and the Op. Power is the received light power measurement. When the ADC are powered down LOS becomes 1 for al channels and Op. Power is 0 µW.

The next checkpoint in data path A is the TLK10022 PRBS validation signal. The information regarding the validation signal is placed in register 0x13 of the device in the LOS signal field. For the 24 channels receiving data with PRBS, the LOS signal is off whereas in the 8 channels without optical transceiver there is a LOS signal. Data shown in Fig. 6.6 (left) represents the status of input 1 for all the link aggregators in the IDM taken from register 0x13. This test is carried out for all the links at each initialization to ensure the connection on data path A.

Fig. 6.6. The IDM server reading of the IDM register 13 and the TLK10022 register table. All Channels from TLK0 to TLK2 are connected, TLK3 has no Rx optical transceiver attached in this example (LOS signal High) and TLK4 is powered off. There are two lines for each TLK representing input 1 of channel A and B respectively.

The data path A has been characterized with a differential probe on a Keysight URX0334A Oscilloscope of 33GHz bandwidth and 128GSa/s. Although the result is acceptable, the measurement has not the best accuracy due to the use of a contact probe and not a soldered probe.

Fig. 6. 7. The Oscilloscope data path A measurement, the data decoding of the 8B/10B along with the Real-Time Eye. Image granted by Keysight Technologies Spain collaboration from a UXR0334A Oscilloscope.

The Eye diagram can be found on Fig. 6. 7, with a time window >300ps and eye height over 300mV. The decoded data is digitized data and the symbol K28.7 is a comma from the 8B/10B protocol of JESD204 to maintain sync. The Table 6. 3 represents the jitter measurement values for the data path A, where the higher value is Inter Symbol interference from Data Dependant Jitter [113], this is due to same link interferences by reflexions due to the point of measurement.

Jitter Results 2Gbps link IDM					
Jitter	Value (ps)	Name	Jitter	Value (ps)	Name
TJ	120,35	Total Jitter			
RJ	5,80	Random Jitter			
DJ	58,04	Deterministic Jitter	DCD	21,02	Duty Cycle Distortion
$PJ_{(\delta-\delta)}$	6,25	Periodic Jitter (Cross)	ISI	44,53	Inter Symbol Interf.
PJ_{rms}	1,76	Periodic Jitter RMS	DDJ	58,96	Data Dependant Jitter

Table 6. 3. IDM data path A link Jitter value table.

To validate data path B, a PRBS7 and a PRBS31 signal are generated in the TLK10022. For this link, the FPGA resources are capable of analysing the EYE and BER with the Xilinx IBERT module [114] and the PRBS detection of the transceiver.

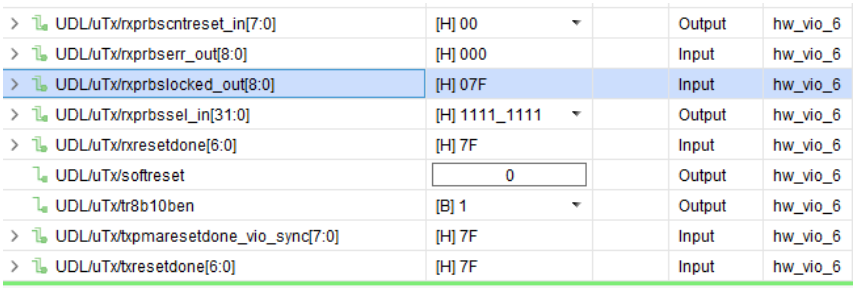

Fig. 6.8. The Xilinx Vivado VIO controlling the PRBS signals and some of the GTH transceiver controls. The rxprbslocked_out indicates all 7 channels on the example are receiving data from TLK.

The GTH Rx transceivers have a specific module for PRBS incoming pattern detection in which the *rxprbssel* signal selects which pattern is detecting. In the case shown in Fig. 6.8, all channels are in PRBS7 mode and the TLK10022 is generating this signal as well. The *rxprbslocked_out* is stable in the 7 channels with no errors found on *prbserr_out* signal.

The eye diagram depicts the successive signals arriving to the transceiver. Transitions on both edges are superimposed to give a statistic representation of the signal reception quality. The eye aperture is proportional to the stability of the transceiver reception: a wider eye opening represents that each bit can be read in a bigger time window whereas a higher eye opening represents a bigger margin for the receiver to detect the change on the voltage level. On the IBERT Eye Diagram representation, the vertical axis represents the voltage codes from the receiver and the horizontal one the relative time over transition. The colour represents the Bit Error Rate (BER) of the incoming data in that area.

In Fig. 6.9. the Eye diagram of channel 5 shows a 71% of eye opening, extracted by the IBERT module from Xilinx Rx transceivers, while the working channels is in 2 Gbps. Once the data from TLK10022 link is aggregated to 8 Gbps the eye diagram reduces to 50% on the worst cases as shown in Fig. 6.10.

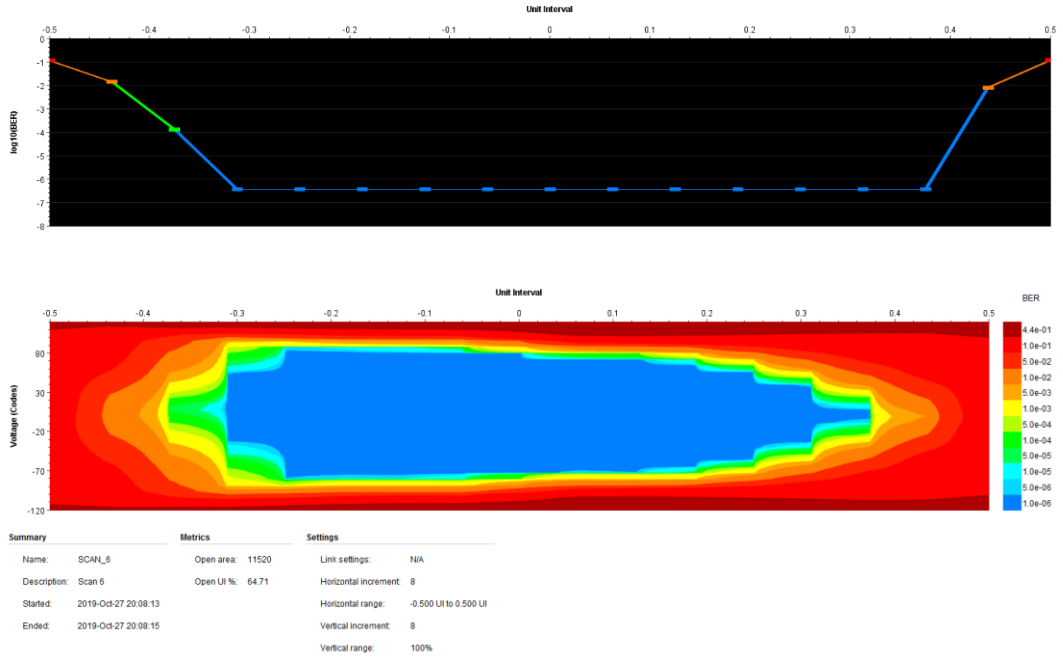

Fig. 6.9. The bathtub (up) and the Eye diagram (Down) of the channel 5 from the GTH X1Y9 from data path B HSL 0 corresponding to TLK10022 1 (IC6) channel B for 2Gbps.

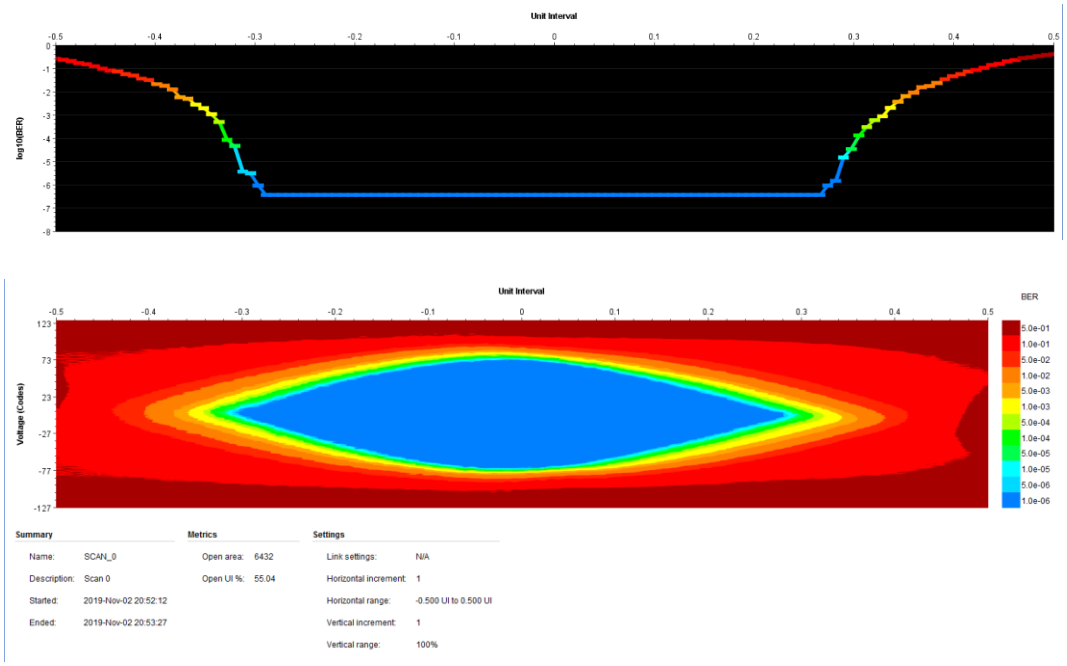

Fig. 6.10. The bathtub (up) and the Eye diagram (Down) of the channel 5 from the GTH X1Y9 from data path B HSL 0 corresponding to TLK10022 1 (IC6) channel B with normal data link at 8Gbps.

After the PRBS test and Eye Diagrams acquisition, the normal data is sent to stablish the 8b/10b coding and later JESD204 alignment connections.

Before starting data transmission, each low speed lane deserializer, sends a lane alignment pattern. An example of this pattern is presented in Table 6.4. In this case, the pattern ends with a /K30.7/ symbol indicating that the Tlk10022 has found an error (for this example the reason was that Rx link on TLK10022 was not active).

Preamble		
Meaning	Symbol	Type of data and Value
IDLE and Sync (Repeat)	/K28.5/	Control K : 0xBC
Start transmission	/K28.7/	Control K : 0xFB
Data sequence (Repeat 12 times)		
Meaning	Symbol	Type of data and Value
Stream Data	/D21.6/	Data D : 0xD5
Stream Data	/D30.5/	Data D : 0xBE
Stream Data	/D23.6/	Data D : 0xD7
Stream Data	/D3.1	Data D : 0x23
Stream Data	/D7.2/	Data D : 0x47
Stream Data	/D11.3/	Data D : 0x6B
Stream Data	/D15.4/	Data D : 0x8F
Stream Data	/D19.5/	Data D : 0xB3
Stream Data	/D20.0/	Data D : 0x14
Stream Data	/D30.2/	Data D : 0x5E
Stream Data	/D27.7/	Data D : 0xFB
Stream Data	/D21.1/	Data D : 0x35
Stream Data	/D25.2/	Data D : 0x59
Error Found	/K30.7/	Control K : 0xFE
Post amble		
Meaning	Symbol	Type of data and Value
IDLE and Sync (Repeat)	/K28.5/	Control K : 0xBC
End Transmission		

Table 6.4. The TLK10022 line alignment pattern in 8b/10b coding.

The signal is sent by each of the low speed lines on the TLK and aggregated before sending, so it can be used as well to test the aggregation. The sent pattern is shown in Fig. 6.11, where the TLK devices are aggregating and sending the data in a stable link to the SOM board.

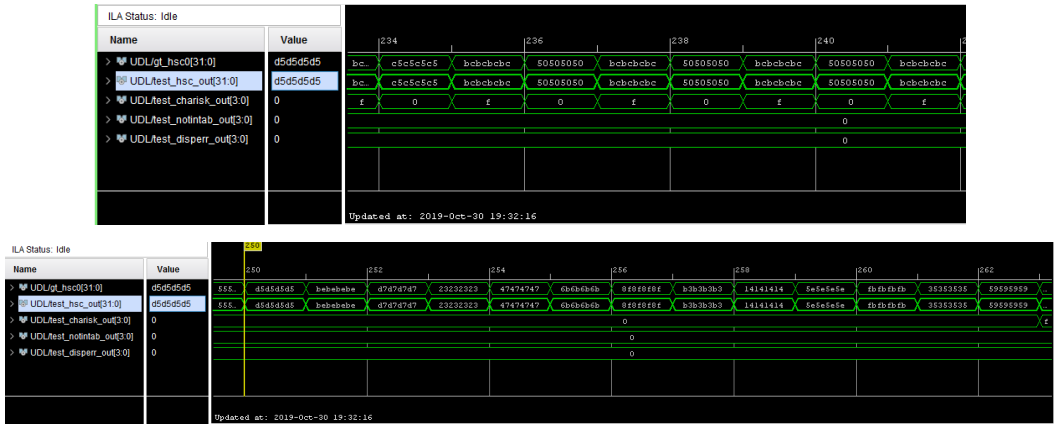

Fig. 6.11. Lane alignment preamble for the TLK10022 to FPGA link (up) and link pattern (Down).

The data path B has been also tested with the Oscilloscope as in data path A. The 8Gbps signal is represented on the Fig. 6. 12, with the Real-Time Eye. Although the low accuracy of the measure due to the contact probe and the point of measurement, the decoding is possible and the eye is still open.

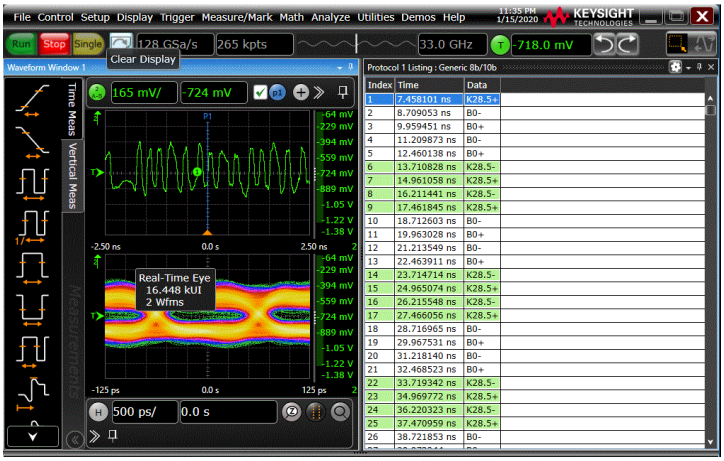

Fig. 6. 12. The data path B signal of 8Gbps connected with a differential contact to the HSP_2 parallel differential line decoupling capacitors. The signal is triggered on 8b/10b pattern and decoded to symbols on the right side of the screen. Image granted by Keysight Technologies Spain collaboration from a UXR0334A Oscilloscope.

The jitter analysis from Table 6. 5 reveals high periodic jitter, and the decomposition shows up excessive Data Dependent Jitter coming mainly from the Inter Symbols Interference. This is explainable because we are positioning the probe near the transmitter driver of the TLK10022 and the reflection from the same transmission line degrades the measurement. Even taking this into account the signal integrity is acceptable to the link, and reveals low cross-talk values (PJ).[113]

The random jitter is partly from measurement connection, further measurements with a soldered probe on the same point revealed 2.5 ps values for random jitter but similar Deterministic Jitter distribution.[115]

Jitter Results 8Gbps link IDM					
Jitter	Value (ps)	Name	Jitter	Value (ps)	Name
TJ	102,91	Total Jitter			
RJ	5,80	Random Jitter			
DJ	21,15	Deterministic Jitter	DCD	2,43	Duty Cycle Distortion
$PJ_{(\delta-\delta)}$	13,36	Periodic Jitter (Cross)	ISI	11,14	Inter Symbol Interf.
PJ_{rms}	1,85	Periodic Jitter RMS	DDJ	12,58	Data Dependant Jitter

Table 6. 5. IDM data path B link Jitter value table.

After the validation of data path, A and B, the full connection is tested with the JESD204 protocol with only one line in bypass mode at 2 Gbps, and for 4 to 1 link aggregation at 8 Gbps. The first data link is a PRBS7 generated by the Digi-Opt12 and detected in the transceiver block. After the detection of the PRBS7, the data is sent from the ADC using the JESD204 protocol and received by the FPGA motherboard. The ADC is capable of sending, using the JESD204 protocol, test patterns consisting of all '0', all '1', '01' pattern or a PRBS as well as the digitalized data.

On the basic data signal from ADC test the first data received on the FPGA is the alignment commas /K/, on the FPGA side the 4 channels commas arrive at once on the high speed link as presented on Fig. 6. 13. The first line is the decodification value and the second line a 4 bit signal refering to wich of those bytes is or not a comma. The four bytes represent each a low speed differential line, the F(1111) value on the second line signify that all values are commas and value 0xBC represents a K28.5, a sync comma. The third and fourth line are respectively dispersion and out of table error, a 0 implies no errors on transmission for the presented trace of 1024 values.

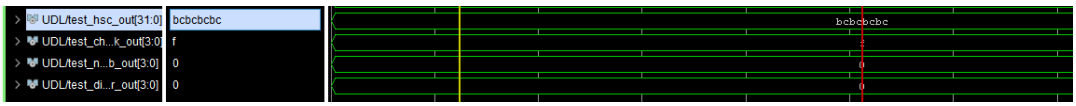

Fig. 6. 13. The comma reception on the FPGA from the HSL_4 combining four lines from Optical Link 2.

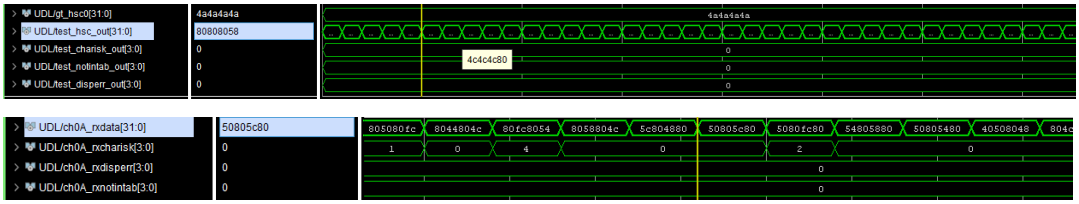

Fig. 6. 14. ***Up:*** *The data coming from the ADC on the FPGA from the HSL_4 combining four lines from Optical Link 2.* ***Down:*** *The data received for one channel.*

JESD204 decoded ADC data							
ADC OFFSET	JESD204 FRAME		Decoded ADC Value	ADC OFFSET	JESD204 FRAME		Decoded ADC Value
	OCTET 1	OCTET 2			OCTET 1	OCTET 2	
100	AF	50	11220	160	46	C8	4528
100	AF	54	11221	160	46	C4	4532
100	AF	4C	11219	160	46	C0	4530
100	AF	48	11218	160	46	C4	4529
120	8C	84	8993	180	23	E4	2297
120	8C	90	8996	180	23	E0	2296
120	8C	74	8989	180	23	E8	2298
120	8C	8C	8995	180	23	D8	2294
140	69	AC	6763				
140	69	B0	6764				
140	69	A8	6762				
140	69	AC	6763				

Table 6. 6. JESD204 decoded data from ADC on CAP FPGA receiver module ready to Pre-processing.

Once the four link are synchronized the ~SYNC signal is changed to high and ADC start to send data, received inside the FPGA (Fig. 6. 14). In Table 6. 6 is represented the decoded values for ADC baseline measure with several DigiOpt-12 offsets set by slow control.

6.4 The AGATA Phase 2.0 Electronics proof-of-concept.

The first proof of concept of Phase 2.0 AGATA electronics was performed at CSNSM in Orsay (France) with the combined work of IFIC-UV and CSNSM during three weeks in June 2019. In this first proof of concept the main goal was to validate the capability of sending data from the ADCs of Digi-Opt12 through Ethernet. The task was divided in several steps: the first one was to stablish a connection between the Pre-processing SOM module and a workstation server through the STARE Ethernet board.

The test-bench for the proof of concept was a combination of the IDM prototype testbench and STARE prototype testbench. The STARE prototype consisted of a KCU105 evaluation board with a Kintex Ultrascale XCKU040 FPGA with the STARE firmware implemented, simulating all the functionalities of the future mezzanine. The IDM prototype testbench connection to this evaluation board, as shown in Fig. 6.5, was using the SFP+ connector, a SFP+ OM3 cable and the SFP+ from the KCU105 board. The KCU105 board was connected to a workstation server with an Ethernet input using a SFP+ mezzanine installed on its FMC socket. The proof of concept testbench is depicted in Fig. 6.15.

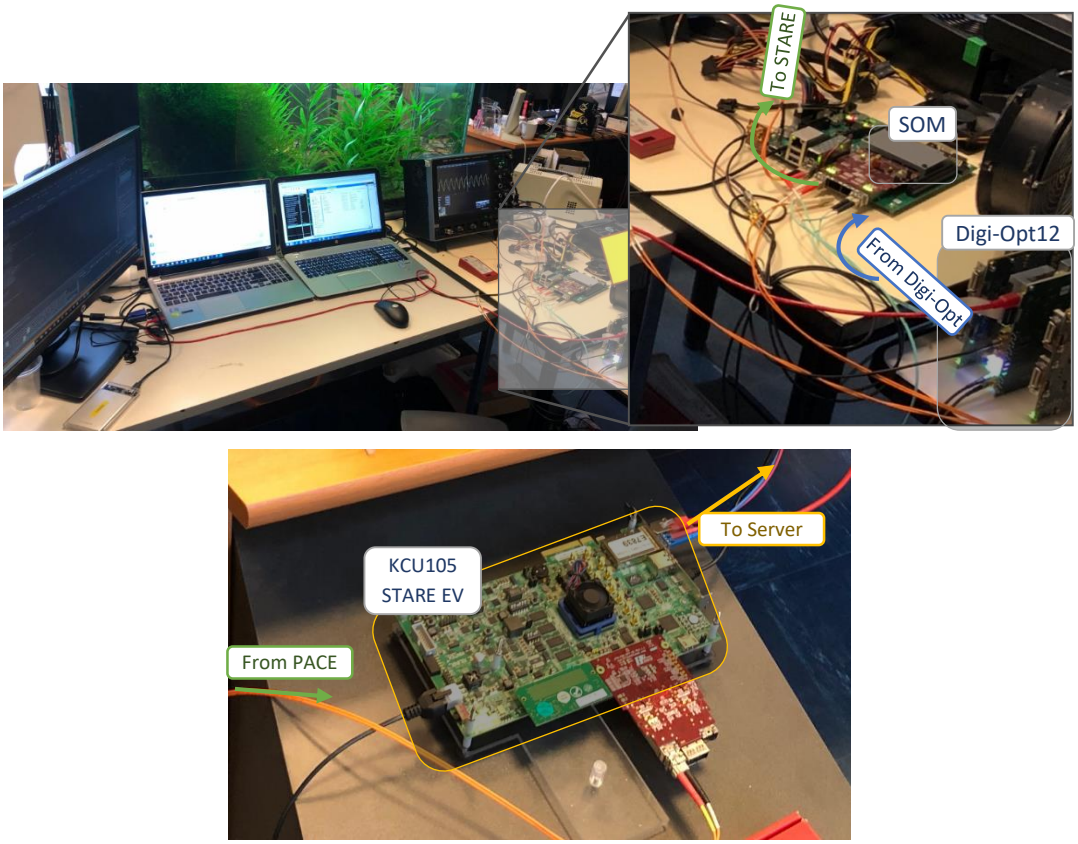

Fig. 6.15. The proof of concept with the IDM and PACE prototypes (Upper panel) and the STARE prototype (lower panel).

The protocol for the connection of the PACE prototype to the STARE prototype board was the Xilinx Aurora 64b. The output data is sent to the Aurora core by an AXI stream protocol. A simple firmware sending a counter value developed by CSNSM was adopted during the proof of concept to fit on the Zynq ZU15EG. The SFP+ from the TEBF0808 motherboard was selected to connect to the STARE prototype board.

In this step, the most critical issue was the configuration of the clocks for the Aurora GTH. The connection was successfully stablished and the device was capable of sending data at 9 Gbps and 5 Gbps. In Fig. 6.16 this is represented as Step I.

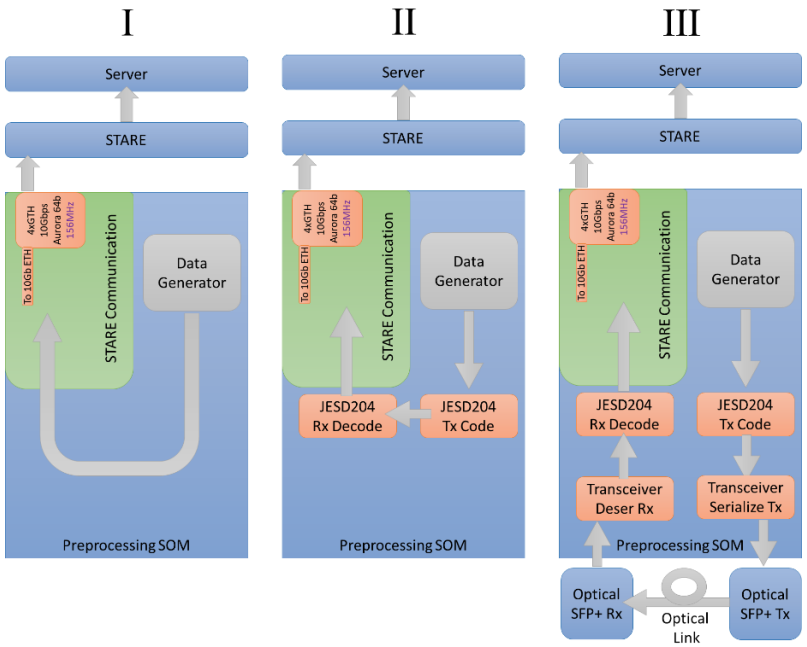

Fig. 6.16. The three steps on the Proof of Concept firmware for the PACE SOM Board.

The next step was to send data, decoded by JESD204, through the network. In order to test the sending with known data, a JESD204 data generator was also implemented and the PACE SOM was programmed to work in an internal loopback. The data path starts from the JESD204 generator, with a values from a 32-bit width counter at 50 MHz. This data is codified in JESD204 format (with ADC parameters K=9, F=2) and 8b/10b protocol, on a 40-bit width word at 50 MHz. This data is connected to the JESD204 receiver and sent to the STARE board through the 10 Gbps Aurora link. The data generated this way reached without errors the server as in the previous step and is represented on Step II of Fig. 6.16.

After the internal loopback, the testbench was configured to send the JESD204 in an external loopback through optical fibres, this scheme is represented on Fig. 6.16 as Step III. The 40-bit width data at 50 MHz is serialized and sent through a 2 Gbps link, simulating the AGATA ADC link. Although the ADC data is 20 bit at 100 MHz, once data is serialized the clock is recovered from the 2 Gbps link, so it is equivalent to the 40 bit at 50 MHz, that is the native frequency for Xilinx JESD204 IP core.

The data is decoded as in the previous step to obtain a 32-bit word at 50 MHz, packaged and sent to the Ethernet network through STARE. The data packets were received on the server at 1.6 Gbps (16bit at 100 MHz), which is the normal throughput for one AGATA ADC link. To study the capability of a higher bandwidth processing, the data was sent twice, reaching 3.2 Gbps in a stable link. To reach 9-10 Gbps data, the number of equivalent channels sent at one can be incremented to five and six; this would be the limit of raw data sent through one link on a trigger less system

To verify the integrity of data, the generated data by the PACE prototype SOM board was read by a ILA Xilinx probe and written to disk in the workstation server. The data correlation was check, as shown in Fig. 6.17, between lines 610 on the left and the last one in the right. The bandwidth for writing data on disk is not as large as for data sending, so the server had to skip several buffers. The counting from the server is little endian.

Fig. 6.17. The results of the first Proof-of-Concept, for the data writing test, presented on AGATA Week 2019. The left side is the data written to disk at the server. The right side is the data sent from the PACE prototype SOM and is a 28-bit sample.

Both tests, the IDM prototype board validation and the proof-of-concept for the Ethernet readout, combined serve as demonstration of the key solutions for the AGATA Phase 2 electronics. The PACE electronics for Phase 2 ensures the data readout from ADC by Ethernet and with a sizeable reduction of differential high speed lines coming from ADCs into the FPGA, improving the optimization of FPGA resources. This work has proven that the integration of the AGATA Phase 2 electronics is viable and sets the green light to start the pre-production version of the AGATA Phase 2 electronics.

Chapter 7:
Conclusions.

For any detector with digital readout, the physical characteristics define the sampling rate of the digitizers. In many cases the sampling rates are in the other of tens or hundreds of Msps, and the sampling rate limits the effective number of bits to 8 to 12. This sampling rates and number of bits transform, in case of using serialized data as it is common nowadays, in the order of 1-5 Gbps signals. It is necessary to consider a high number of signals in case of detector arrays and sizeable larger in segmented detector arrays. However, the sampling frequency and the number of bits per sample to be used in a particular case are characteristics to the type of detector due to the intrinsic signals they provide and the information needed for the discrimination of the events looked for. In the case of AGATA, the signals coming from the detector have a bandwidth of 30 MHz, limited by the preamplifiers used in the readout. This implies a minimum of 60 Msps of sampling which will not change over the years.

On the other side, the communication in the Pre-processing or readout, with FPGAs or high end processors with limited number of transceivers and PHYs but with higher bitrates, over 16Gbps, and increasing along the years set another problem. This issue is the non-optimized communication between both sides of the data path on the detector, that has no solution besides acquiring higher quantity of FPGAs or much more expensive ones. The problem is extensible not only to nuclear instrumentation, but also to instrumentation structures with similar digitizing characteristics.

The produced IDM prototype on this thesis is a solution to the transceiver optimization problem with the time multiplexing of the few-gigabit speed digital lines to optimize the input for modern high speed transceivers. This solution has been validated in the AGATA detector context with a JESD204 communication protocol, specific for analog-to-digital converters and with extensive use on the market, in a modern FPGA device. The IDM prototype is an optical input mezzanine with a 4:1 link line aggregation up to 2.5 Gbps or 2:1 up to 5 Gbsp. This hardware is associated to a specific IP (Intellectual Property) FPGA firmware core to retrieve the original data in the device, developed as well under this work.

As a second goal, this thesis has solved the bottleneck of the electronics integration with the design and manufacture of the IDM prototype. The whole AGATA Phase 2

electronics rely on the keystone of the data aggregation concept to achieve the critical requirement of integration which is now accomplished. In addition to the design and validation of the IDM prototype, the Ethernet readout proof-of-concept for the new electronics PACE in collaboration with the STARE board, firmware and electronics developed by CSNSM Orsay, was also carried out.

In order to conduct these tests, the CAP motherboard, hosting the IDM prototype and STARE, was emulated by evaluation boards, stablishing the requirements for its later production version. In addition, the proof of concept, developed with the colleagues of the collaboration, demonstrated the viability of Ethernet as readout for AGATA spectrometer.

This thesis has contributed actively on the design of the Phase 2 electronics inside the AGATA Collaboration, with strong interaction between all the members of the technical development group of Phase 2 electronics and the strong feedback on the AGATA scientific community. As the only thesis framed on Phase 2 development by the moment, it can be taken as well as a compilation of the knowledge and advances of the collaboration in the matter.

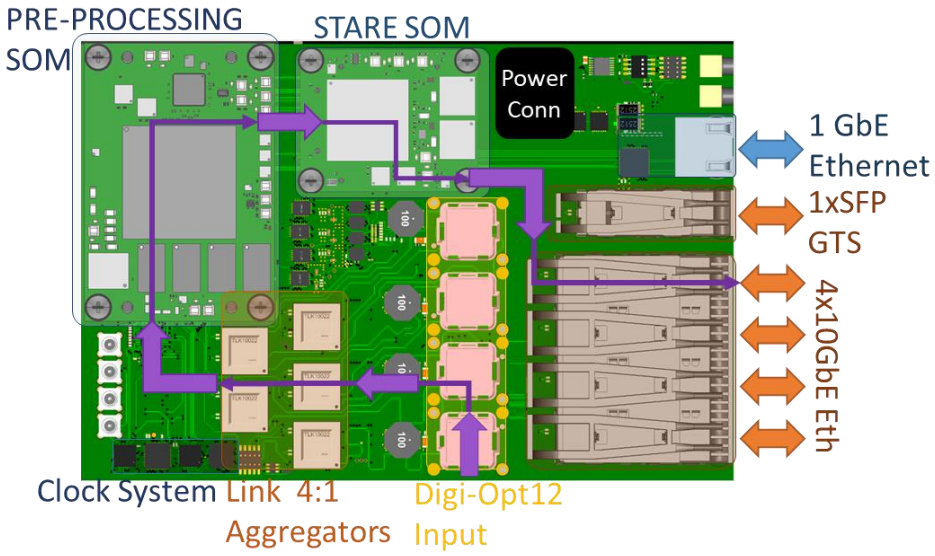

Fig. 7. 1. The PACE Motherboard design for production.

The whole new electronics for Phase 2 will open a new window of possibilities to upgrade the experimental nuclear physics research on AGATA. The increase on FPGA capabilities could be used as platform for new possible Pre-processing algorithms. The extra bandwidth will allow to extract longer length signal traces, to help to improve Pulse Shape Analysis, and possibly the quality of the energy spectra.

The development and validation of the IDM prototype is completed, and the most relevant part of the research for the production on phase 2 is accomplished, even though, there is still work to do. The next step is the production of CAP board based on the IDM prototype and STARE together and the introduction of the SOM concept. Fig. 7.1 shows the preview of the board outline for the 2020 pre-production and 2021 production. It is expected that these electronics will be working in the detector by 2022.

There is also interest non related to AGATA detector for the IDM prototype. This interest relies on the possibility to prepare the board for commercial production, as a solution for other detectors or instrumentation systems with similar issues with digitizer lines congestions. This will serve as technology transfer from developments in scientific research to the industry and sharing the results of this thesis with the worldwide electronic instrumentation community.

List of figures

Chapter 1

Fig. 1.1. Table of nuclides with the stable elements in black and for the other nuclides the colour indicates the type of decay (or radiation) happening in the unstable nuclei, i.e. red: β+, blue:β-, orange: proton-decay, yellow: α-decay, purple: neutron-emitters 2

Fig. 1.2. Level-Scheme of Ni60 populated in the β-decay of Co60. [6] 3

Fig. 1.3. AGATA calibration: Co60 β-decay radioactive source measured Spectra, with the 1.17 MeV gamma emitted in the de-excitation of the state 4+ to 2+ and 1.33 MeV emitted in the de-excitation of the state 2+ to 0+ of Ni60. ©2004 IEEE.[7] 4

Fig. 1.4. ***Left:*** *Attenuation coefficients for gamma ray in relation with atomic number Z of absorber material.* ***Right:*** *Image representing the different interactions of gamma ray with matter.* 5

Fig. 1.5. ***Left****: Scintillator and PMT diagram[8]. Center: Example diagram of a Camberra SEGe Coaxial Ge Detector.* ***Right****: Geiger Muller Counter diagram[9].* 7

Fig. 1.6. NaI(Tl) scintillator spectra (A) and Ge(Li) Semiconductor spectra (B) comparison. Greater energy resolutions on the gamma ray peaks are observed on semiconductor device.[10] 8

Fig. 1.7. A conceptual view of the possible results related to impact parameter B between beam and target nuclei. 11

Fig. 1.8. Representation of possible reactions in relation to energy beam and impact parameter. 12

Fig. 1.9. ***Left****: image representing the effect of suppression on Germanium arrays.[21].* ***Right****: Euroball cluster detector.* 15

Fig. 1.10. a: Example of a gamma ray impact on several segmented sectors of HPGe. b: representation of the signals on each of the segments. c: gamma tray path for tracking techniques. [21] d: AGATA P/T signal demonstration for each part of the tracking algorithm. 18

Fig. 1.11. Scheme showing the gamma-ray tracking concept differentiating between the hardware and software parts. 19

Fig. 1.12. The AGATA 180 detectors tiling of the Sphere and construction of the triple cluster. [32] 20

Fig. 1.13. Left: The AGATA detector cryostat. ***Right****: The AGATA detector segment distribution.[34]* 21

Fig. 1.14. AGATA sensitivity compared with previous arrays and AGATA design specifications. 21

Fig. 1.15. AGATA with 35 detectors coupled to NEDA, DIAMANT and NWall [30] 22

Fig. 1.16. ***Left****: Refractive index profiles of (a) step-index multimode fibers, (b) graded-index multimode fibers, (c) match-cladding single-mode fibers, (d, e) depressed-cladding single-mode*

fibers, (f–h) dispersion-shifted fibers, and (i, j) dispersion-flattened fibers.[42] ***Right Up:*** *Optical line attenuations loss comparison on spectra between polymer and silica.[43]* ***Right Down:*** *Silica SiO2 loss in relation to Wavelength.* _____ *24*

Fig. 1.17. ***Right****: types of optical mechanical connectors.* ***Left****: Example of an active transceiver part SFP+ connector from Finisar Corporation with a LC mechanical connector socket.* _____ *26*

*Fig. 1.18. Example of a differential strip line and the high speed transmission and reflexion analysis.[64]*_____ *27*

*Fig. 1.19. Diagram of an Array detector instrumentation.*_____ *27*

Fig. 1.20. ***Left****: IGLOO FPGA size reference.* ***Right****: Zynq Ultrascale+ MPSO processor multicore ARM + GPU + Cortex ARM Microcontroller + Xilinx FPGA fabric*_____ *30*

Chapter 2

Fig. 2.1. ***Up****: First generation of AGATA electronics and Read-Out. Down: Second generation of AGATA electronics, design in the Phase 1 of the array.* _____ *33*

Fig. 2.2. ***Left****: Preamplifier cold and warm part conceptual design on the AGATA cryostat.* ***Right****: Images of the AGATA preamplifiers.*_____ *34*

Fig. 2.3. ***Left****: Phase 0 digitizer crate for one crystal digitalizing with 38 channels.* ***Right****: Phase 1 digitizer crate, for a triple cluster detector digitalizing with 114 channels.* _____ *37*

Fig. 2.4. ***Left****: AGATA Digi-Opt 12 Digitizer boards from the Phase 1 staked.* ***Right****: AGATA LP1 Control Card.* _____ *38*

*Fig. 2.5. Digitizer box disassembly image and mounting schematics.*_____ *40*

Fig. 2.6. The conceptual block design of AGATA Pre-processing system. _____ *42*

Fig. 2.7. The moving window deconvolution steps. a) The original input detector pulses. b) Deconvolution signal from pulses. c) The m-step differentiation. d) The average applied to m-step pulses. _____ *44*

Fig. 2.8. ***Left****: The Phase 0 first generation Pre-processing ATCA carrier and Mezzanines.* ***Right****: the second generation Phase 1 GGP board for Pre-processing and readout.* _____ *46*

Fig. 2.9. ***Left****: Incoming data bit rate reduction effect and triggering scheme of AGATA.* ***Right****: A generic GTS tree representation.* _____ *49*

*Fig. 2.10. The AGATA GTS dataflow after a trigger request from the leaf and the response of the trigger processor.*_____ *50*

Fig. 2.11. Image of a GTS version 2 mezzanine for ATCA, it can be configured as FIFO, root or leaf. *51*

*Fig. 2.12. Scheme of the NARVAL AGATA Acquisition and processing system Data Flow*_____ *52*

Chapter 3

Fig. 3.1. The AGATA Phase 1 electronics Test-bench. The devices under test (DUT) are the Digitizer Box, the Power Supply Unit (PSU) and Pre-processing board inside Workstation (GGP). 58

Fig. 3.2. Test-bench general diagram with the responsible developers of each bloc INFN-LNL (Laboratori Nazionali di Legnaro, Italy) are the developers for de Pre-processing GGP and its acquisition software meanwhile Digitizer ADC is developed by INFN University of Milano. 60

Fig. 3.3. USB bridge update to read the temperatures and voltages of the Digitizer Box through USB. This method is useful as a laboratory debugging without the full electronics chain. 61

Fig. 3.4. Offset data analysis plot from a working system (up) and a falling Digitizer box (down), the software detects problems for offset value 140 with 13 non-working channels. 62

Fig. 3.5. Testbench software functionality diagram, displaying the Automatic Tests, outputs and the GUI interface. 63

Fig. 3.6. Two of the GUI panels with the digitizer system status. 64

Fig. 3.7. USB Bridge Update for accessing and programming the ADC to start up in a standalone mode. 65

Fig. 3.8. Example of histograms output for 3.3V (left) and 2V(right) of PSU in voltage (up) and current(down). 66

Chapter 4

Fig. 4.1. Original proposal methodology plan map. 69

Fig. 4.2. The preliminary PACE system main design. 71

Fig. 4.3. Final Path Selected from original map. 73

Fig. 4.4. PACE 2.0 for AGATA phase 2.0 electronic final design. ***Up****: the mechanical assembly.* ***Down****: The conceptual block design.* 75

Fig. 4.5. PACE 2.0 CAP motherboard conceptual design. 76

Fig. 4.6. The Input Data Mezzanine original conceptual design. 77

Fig. 4.7. The Serial Transfer Acquisition over Ethernet mezzanine conceptual design. Based on the last version presented at 20th AGATA Week 2019 (LNL-INFN) by CSNSM Orsay. 78

Fig. 4.8. PACE and CAP motherboard production conceptual design. 79

Chapter 5

Fig. 5.1. The IDM Optic input concept and connection to Digi-Opt12 for 38 channels. There is a mechanical adaptor to change the PRIZM® LightTurn® to MPO mechanical connection. _____ 85

Fig. 5.2. The Flex-Rigid board PCB design for the Copper connection option._____ 86

Fig. 5.3. The TLK10022 structure and behaviour as is presented don the datasheet for transmission (Up) and reception (Down)._____ 87

Fig. 5.4. The mid and high speed links from channel flow for IDM._____ 88

Fig. 5.5. The ANSI Vita 57.1 standard design regions and the associated dimensions. _____ 91

Fig. 5.6. Size of the ICE40LP4k in relation to a 10 cent coin_____ 92

Fig. 5.7. The conceptual design a firmware module from the IDM Firmware. _____ 95

Fig. 5.8. The global conceptual design of the IDM firmware. _____ 96

Fig. 5.9. The clocking network for the IDM, controlled through the Optic & Clock Module registers of the FPGA._____ 99

Fig. 5.10. The miniPod power filter implemented in IDM and recommended by AVAGO. _____ 101

Fig. 5.11. Power distribution scheme for IDM motherboard. _____ 103

Fig. 5.12. The final design IDM stack-up and vias distribution. _____ 104

Fig. 5.13. Microstrip space and width values calculations for L2 and L9 for the selected stack up configuration. _____ 106

*Fig. 5.14. **Left**: Some of the HSL lines layout with the minimum separation between lines. **Right**: Output from the Top TLK10022 differential line to the L2 microvia bridge and the 0 Ohm resistor 107*

Fig. 5.15. Analysis of the Microvia rhombic bridge._____ 107

Fig. 5.16. The IDM power simulation schematic and plot, the first 7 are the generated supplies, the resting are from taken from the FMC connector._____ 109

Fig. 5.17. Example of the power on system with a delay of 300 us and soft start._____ 110

Fig. 5.18. The step 3D mechanical model of IDM. _____ 110

Fig. 5.19. The selected differential line HSL_4 (Fig. 5.4) for 3D EM simulation with its environment. _____ 112

*Fig. 5.20. **Left**: Calculated impedance of HSL_4 with 3D Electromagnetic simulation. **Right**: The S parameters of HSL_4 in 3D EM simulation. _____ 112*

Fig. 5.21. The TOP, L1 and L2 of the IDM in the FPGA area, on the top we find the recommended layout on the bottom the final design. _____ 113

Fig. 5.22. The IDM prototype v1.2, TOP and BOTTOM view respectively._____ 114

Chapter 6

Fig. 6.1. The Phase 2.0 PACE SOM Firmware blocks for AGATA Pre-processing. _____121

Fig. 6.2. The PACE firmware receiver module. The clock domains are referenced with different colours, red is the 200 MHz from link aggregator, blue is the 50 MHz for the JESD204 decoding and black is the 100 MHz common reference clock. _____123

Fig. 6.3. Representation of the JESD204 pattern for CGS, ILAS and User Data. On the AGATA case the K would be 9 frames._____126

Fig. 6.4. ***Left****: The connection conceptual design of the K-800 IDM prototype testbench.* ***Right****: The connected IDM prototype and SFP+ output board to the K-800 evaluation board. _____128*

Fig. 6.5. ***Left****: Image of the testbench, at the bottom right it is placed the TEBF0808 evaluation board with the TE0808 Zynq, the blue FMC-FMC cable extension is connected to the board on one end and to the IDM on the other. The Digi-Opt12, the Control Card and its power supply are on the centre of the image.* ***Right****: Conceptual design of the IDM testbench, data path is represented on purple. _____130*

Fig. 6.6. The IDM server reading of the IDM register 13 and the TLK10022 register table. All Channels from TLK0 to TLK2 are connected, TLK3 has no Rx optical transceiver attached in this example (LOS signal High) and TLK4 is powered off. There are two lines for each TLK representing input 1 of channel A and B respectively._____132

Fig. 6. 7. The Oscilloscope data path A measurement, the data decoding of the 8B/10B along with the Real-Time Eye. Image granted by Keysight Technologies Spain collaboration from a UXR0334A Oscilloscope. _____133

Fig. 6.8. The Xilinx Vivado VIO controlling the PRBS signals and some of the GTH transceiver controls. The rxprbslocked_out indicates all 7 channels on the example are receiving data from TLK. _____134

Fig. 6.9. The bathtub (up) and the Eye diagram (Down) of the channel 5 from the GTH X1Y9 from data path B HSL 0 corresponding to TLK10022 1 (IC6) channel B for 2Gbps. _____135

Fig. 6.10. The bathtub (up) and the Eye diagram (Down) of the channel 5 from the GTH X1Y9 from data path B HSL 0 corresponding to TLK10022 1 (IC6) channel B with normal data link at 8Gbps. 135

Fig. 6.11. Lane alignment preamble for the TLK10022 to FPGA link (up) and link pattern (Down). 137

Fig. 6. 12. The data path B signal of 8Gbps connected with a differential contact to the HSP_2 parallel differential line decoupling capacitors. The signal is triggered on 8b/10b pattern and decoded to symbols on the right side of the screen. Image granted by Keysight Technologies Spain collaboration from a UXR0334A Oscilloscope._____137

Fig. 6. 13. The comma reception on the FPGA from the HSL_4 combining four lines from Optical Link 2. _____ *138*

Fig. 6. 14. ***Up:*** *The data coming from the ADC on the FPGA from the HSL_4 combining four lines from Optical Link 2.* ***Down:*** *The data received for one channel.* _____ *139*

Fig. 6.15. The proof of concept with the IDM and PACE prototypes (Upper panel) and the STARE prototype (lower panel). _____ *140*

Fig. 6.16. The three steps on the Proof of Concept firmware for the PACE SOM Board. _____ *141*

Fig. 6.17. The results of the first Proof-of-Concept, for the data writing test, presented on AGATA Week 2019. The left side is the data written to disk at the server. The right side is the data sent from the PACE prototype SOM and is a 28-bit sample. _____ *142*

Chapter 7

Fig. 7. 1. The PACE Motherboard design for production. _____ *146*

List of tables

Chapter 2

Table 2.1. Comparative of the Phase 0 and Phase 1 digitizer electronics. _____ *41*

Table 2.2. Comparative of the Phase 0 and Phase 1 Pre-processing electronics. _____ *48*

Chapter 5

Table 5.1 Line Rate and Reference Clock Frequency Ranges for the Low and High Speed Sides of SERDES. _____ *89*

Table 5.2 Optimal Computed reference clock with selected Half rate on the Low Speed Side and Full rate on the High Speed Side. _____ *89*

Table 5.3. Frequency calculation for 4:1 in 2GHz input and 8GHz output and configuration of TLK10022. _____ *89*

Table 5.4. Programming area switch configuration possibilities. _____ *93*

Table 5.5. Sensors and power control devices configuration. _____ *94*

Table 5.6. Modules memory and command address relations and their controlled devices. _____ *97*

Table 5.7. Reduced part of the memory table on IDM. _____ *98*

Table 5.8. Power supply connections for FPGA, needs, description and connections _____ *101*

Table 5.9. Power lines names, feed devices and consumption current. _____ *102*

Table 5.10. The Isola FR408HR properties in relation to the frequency of the signals. _____ *105*

Table 5.11. The possible type of vias for IDM prototype and size limitations. _____ *105*

Table 5.12. Full interconnection path from the Optical input to the FMC output. _____ *108*

Table 5.13. excerpt of the Sigrity SI report with the table of the differential impedance variations for some of the MSL lines. _____ *111*

Chapter 6

Table 6.1. JESD204 special characters meaning and values. The 10bit RD=-1 and RD+1 corresponds to the table with previous polarity -2 and +2 respectively. _____ *125*

Table 6.2. Table of the MiniPod Rx Optical transceivers link, the LOS signal 0 indicates the link is stablished with the Tx device and the Op. Power is the received light power measurement. When the ADC are powered down LOS becomes 1 for al channels and Op. Power is 0 µW. _____ *132*

Table 6. 3. IDM data path A link Jitter value table. _____ *133*

Table 6.4. The TLK10022 line alignment pattern in 8b/10b coding. _____ *136*

Table 6. 5. IDM data path B link Jitter value table. _____ *138*

Table 6. 6. JESD204 decoded data from ADC on CAP FPGA receiver module ready to Pre-processing.

_____ *139*

References

[1] O. Glasser, *Wilhelm Conrad Röntgen And The Early History Of The Roentgen Rays*. Norman Publishing, 1993., 1934.

[2] H. F. Walton, "The Curie-Becquerel story," *J. Chem. Educ.*, vol. 69, no. 1, p. 10, 2009.

[3] K. S. Krane, *Introductory Nuclear Physics*. John Wiley & Sons, Inc., 1988.

[4] IAEA - Nuclear Data Section, "Live Chart of Nuclides," 2019. [Online]. Available: www-nds.iaea.org. [Accessed: 06-Aug-2019].

[5] G. F. Knoll, *Radiation Detection and Measurement*, 4th ed. John Wiley and Sons Ltd, 2010.

[6] Nucleonica GmbH, "Nucleonica." [Online]. Available: https://www.nucleonica.com. [Accessed: 26-Mar-2019].

[7] C. Boiano, R. Bassini, M. Petcu, G. Pascovici, B. Cahan, F. Zocca, A. Pullia, and D. Weisshaar, "The AGATA charge-sensitive preamplifiers with built-in active-reset device and pulser," no. May 2014, pp. 1411–1414, 2005.

[8] Deutsches Elektronen Synchrotron; Université de Genève; Max-Planck-Gesellschaft; Max-Planck-Gesellschaft, "SENSE." [Online]. Available: https://www.sense-pro.org/. [Accessed: 01-Aug-2019].

[9] J. Verplancke, P. F. Fettweis, R. Venkataraman, B. M. Young, and H. Schwenn, *Handbook of Radioactivity Analysis*, 3rd ed. Elsevier, 2012.

[10] S. R. Cherry, J. E. Phelps, and M. A. Sorenson, *Physics in Nuclear Medicine (Fourth Edition)*. Elsevier, 2012.

[11] Canberra Industries Inc., "Germanium Detectors - User Manual," 2008.

[12] G. F. Knoll, *Radiation Detection and Measurement*, 4th ed. John Wiley & Sons., 2010.

[13] E. M. Pell, "Ion Drift in an n-p Junction," *J. Appl. Phys.*, vol. 31, no. 2, pp. 291–302, 1960.

[14] J. Eberth and J. Simpson, "From Ge(Li) detectors to gamma-ray tracking arrays-50 years of gamma spectroscopy with germanium detectors," *Prog. Part. Nucl. Phys.*, vol. 60, no. 2, pp. 283–337, 2008.

[15] W. L. Hansen, "High-purity germanium crystal growing," *Nucl. Instruments Methods*, vol. 94, no. 2, pp. 377–380, 1971.

[16] R. H. Pehl, R. C. Cordi, and F. S. Goulding, "High-purity germanium: Detector fabrication and performance," *IEEE Trans. Nucl. Sci.*, vol. 19, no. 1, pp. 265–269, 1972.

[17] ORTEC, “Overview of Semiconductor Photon Detectors,” 2019.

[18] V. Zagrebaev, *Heavy Ion Reactions at Low Energies*, 1st ed. Springer International Publishing, 2019.

[19] M. Thoennessen, “Fusion-Evaporation Reactions,” in *The Discovery of Isotopes*, Springer, Cham, 2016.

[20] M. Thoennessen, “Projectile Fragmentation and Fission,” in *The Discovery of Isotopes*, Springer, Cham, 2016.

[21] M. A. Riley, J. Simpson, and E. S. Paul, “High resolution gamma-ray spectroscopy and the fascinating angular momentum realm of the atomic nucleus,” *Phys. Scr.*, vol. 91, no. 12, 2016.

[22] J. Simpson, “The Euroball Spectrometer,” *Zeitschrift für Phys. A Hadron. Nucl.*, vol. 358, no. 2, pp. 139–143, 1997.

[23] I.-Y. Lee, “The GAMMASPHERE,” *Nucl. Phys. A*, vol. 520, pp. 641–655, 1990.

[24] R. M. Lieder et al., “The TMR network project ‘Development of γ-ray tracking detectors,’” *Nucl. Phys. A*, vol. 682, no. 1–4, pp. 279–285, 2001.

[25] J. Hellmig and H. V. Klapdor-Kleingrothaus, “Identification of single-site events in germanium detectors by digital pulse shape analysis,” *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip.*, vol. 455, no. 3, pp. 638–644, 2000.

[26] A. Lopez-Martens, K. Hauschild, A. Korichi, J. Roccaz, and J.-P. Thibaud, “g-ray tracking algorithms: a comparison,” *Nucl. Instruments Methods Phys. Res. Sect. A*, vol. 89, no. 6, p. 904, 2004.

[27] I. Y. Lee et al., “GRETINA: A gamma ray energy tracking array,” *Nucl. Phys. A*, vol. 746, no. 1–4 SPEC.ISS., 2004.

[28] E. Gatti, G. Padovini, and V. Radeka, “Signal evaluation in multielectrode radiation detectors by means of a time dependent weighting vector,” *Nucl. Instruments Methods Phys. Res.*, vol. 193, no. 3, pp. 651–653, 1982.

[29] L. Mihailescu, W. Gast, R. M. Lieder, H. Brands, and H. Jäger, “Influence of anisotropic electron drift velocity on the signal shapes of closed-end HPGe detectors,” *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip.*, vol. 447, no. 3, pp. 350–360, 2000.

[30] AGATA Colaboration, “AGATA Colaboration Web.” [Online]. Available: https://www.agata.org/about. [Accessed: 01-Sep-2019].

[31] E. Farnea, F. Recchia, D. Bazzacco, T. Kröll, Z. Podolyák, B. Quintana, and A. Gadea, “Conceptual design and Monte Carlo simulations of the AGATA array,” *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip.*, vol. 621, no. 1–3, pp. 331–343, 2010.

[32] S. Akkoyun et al., “AGATA - Advanced GAmma Tracking Array,” *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip.*, vol. 668, pp. 26–58, Mar. 2012.

[33] G. Pascovici, A. Pullia, F. Zocca, B. Bruyneel, and D. Bazzacco, “Low noise, dual gain preamplifier with built in spectroscopic pulser for highly segmented high-purity germanium detectors,” *WSEAS Trans. Circuits Syst.*, vol. 7, no. 6, pp. 470–481, 2008.

[34] J. Simpson, “The AGATA Spectrometer: Next generation gamma-ray spectroscopy,” *J. Phys. Conf. Ser.*, vol. 606, no. 1, 2015.

[35] E. Clément et al., “Conceptual design of the AGATA 1π array at GANIL,” *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip.*, vol. 855, no. February, pp. 1–12, 2017.

[36] N. Lalović et al., “Performance of the AGATA γ-ray spectrometer in the PreSPEC set-up at GSI,” *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip.*, vol. 806, pp. 258–266, 2016.

[37] A. Gadea et al., “Conceptual design and infrastructure for the installation of the first AGATA sub-array at LNL,” *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip.*, vol. 654, no. 1, pp. 88–96, 2011.

[38] G. Balamurugan, B. Casper, J. E. Jaussi, M. Mansuri, F. O. Mahony, and J. Kennedy, “Modeling and Analysis of High-Speed I / O Links,” vol. 32, no. 2, pp. 237–247, 2009.

[39] IEEE, *IEEE Standard for Ethernet*, vol. 2012, no. December. 2012.

[40] Cortina Systems and Cisco Systems, “Interlaken Protocol Definition,” 2008.

[41] M. S. Sharawi, “Practical Issues in high speed PCB design,” *IEEE Potentials*, vol. 23, no. 2, pp. 24–27, 2004.

[42] C. DeCusatis, *Handbook of Fiber Optic Data Communication - A Practical Guide to Optical Networking*, Fourth Edi. Elsevier.

[43] K. Peters, “Polymer optical fiber sensors - A review,” *Smart Mater. Struct.*, vol. 20, no. 1, 2011.

[44] D. C. Tran, G. H. Sigel, and B. Bendow, “Heavy Metal Fluoride Glasses and Fibers: A Review,” *J. Light. Technol.*, vol. 2, no. 5, pp. 566–586, 1984.

[45] M. Karabulut, E. Melnik, R. Stefan, G. K. Marasinghe, C. S. Ray, C. R. Kurkjian, and D. E. Day, “Mechanical and structural properties of phosphate glasses,” *J. Non. Cryst. Solids*, vol. 288, no. 1–3, pp. 8–17, 2001.

[46] P. Mathias, E. Gramlich, G. De, and S. Warncke, “MULTICORE OPTICAL FIBRE,” US 6,301,420 B1, 2001.

[47] A. Macho and R. Llorente, “Multi-Core Optical Fibers: Theory, Applications and Opportunities,” *Sel. Top. Opt. Fiber Technol. Appl.*, p. 13, 2017.

[48] Y. Furukawa, “Application of InGaAsP and AlGaAsSb for optical fiber transmission,” *Jpn. J. Appl. Phys.*, vol. 19, pp. 295–303, 1980.

[49] M. A. Othman, S. N. Taib, M. N. Husain, and Z. A. F. M. Napiah, “Reviews on avalanche photodiode for optical communication technology,” *ARPN J. Eng. Appl. Sci.*, vol. 9, no. 1, pp. 35–44, 2014.

[50] W. Diels, M. Steyaert, and F. Tavernier, “Schottky diodes in 40nm bulk CMNOS for 1310nm high-speed optical receivers,” *Opt. Soc. Am.*, 2017.

[51] M. Bayindir, F. Sorin, A. F. Abouraddy, J. Viens, S. D. Har, J. D. Joannopoulos, and Y. Fink, “Metal – insulator – semiconductor optoelectronic fibres,” vol. 431, no. October, 2004.

[52] SFF Committee, “SFF-8431 Specifications for Enhanced Small Form Factor Pluggable Module SFP +,” 2009.

[53] 4-Wavelength WDM MSA, “4WDM-40 MSA Technical Specifications,” 2017.

[54] Avago Technologies, “AFBR-776BxxxZ and AFBR-786BxxxZ,” 2013.

[55] Avago Technolgies, “MiniPOD™ AFBR-812VxyZ, AFBR-822VxyZ Product Brief,” 2013.

[56] Samtec, “Firefly application design guide,” 2019.

[57] Infiniband, “120 Gb/s 12x Small Form-factor Pluggable (CXP),” 2009.

[58] AGC - nelco, “AGC Nelco PCB Materials Products,” 2018.

[59] “Rogers webpage,” 2019. [Online]. Available: https://www.rogerscorp.com. [Accessed: 08-Aug-2019].

[60] Isola, “FR408HR Dataasheet - High Performance Laminate and Prepreg,” 2019.

[61] A. Weiler, A. Pakosta, and A. Verma, “High-Speed Layout Guidelines Application Report High-Speed Layout Guidelines,” 2017.

[62] Texas Instruments, “High-Speed Interface Layout Guidelines - SPRAAR7H,” 2018.

[63] S. Chen, C. Chen, C. Liao, J. Chen, T. Wu, and B. Mutnury, “Via Optimization for Next Generation Speeds,” in *IEEE 26th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)*, 2017, pp. 3–5.

[64] T. Reuschel, M. Kotzev, D. Dahl, and C. Schuster, “Modeling of differential striplines in segmented simulation of printed circuit board links,” in *IEEE International Symposium on Electromagnetic Compatibility (EMC)}*, 2016, pp. 911–916.

[65] W. Beckenbaugh and J. K. Vrtis, “High-Density Interconnects : Enabling the

Intelligence of Things," *The PCB Magazine*, 2015.

[66] Würth Electronik, "DESIGN GUIDE HDI," pp. 1–8, 2018.

[67] S. H. Fuller and L. I. Millett, "Computing performance: Game over or next level?," *Computer (Long. Beach. Calif).*, vol. 44, no. 1, pp. 31–38, 2011.

[68] Xilinx Inc., "UltraScale Architecture and Product Data Sheet: Overview - DS890," 2019.

[69] Intel, "Intel Stratix 10 GX / SX Product Table," 2019.

[70] Lattice Semiconductor, "iCE40 LP / HX Family Data Sheet," 2015.

[71] Microsemi Corporation, "IGLOO nano Low Power Flash FPGAs with Flash * Freeze Technology Features and Benefits," 2015.

[72] J. Simpson, J. Nyberg, and W. Korten, Eds., "Advanced Gamma Tracking Array Technical Design Report," 2008.

[73] F. Zocca, A. Pullia, C. Boiano, and R. Bassini, "A smart reset circuit for low-noise preamplifiers of X-γ ray sensor signals," *IEEE Trans. Nucl. Sci.*, vol. 54, no. 1, pp. 197–201, 2007.

[74] 3M, "3M ™ Mini D Ribbon (MDR) Cable Assembly - E86982," 2011.

[75] A. Pullia, D. Barrientos, D. Bazzacco, M. Bellato, D. Bortolato, and R. Isocrate, "Digi-opt12: 12-channel 14/16-bit 100/125-MS/s digitizer with optical output for GALILEO/AGATA," in *Proc. IEEE Nuclear Science Symp. and Medical Imaging Conf. Rec*, 2012.

[76] D. Barrientos et al., "Development of the control card for the digitizers of the second generation electronics of AGATA," *2012 18th IEEE-NPSS Real Time Conf. RT 2012*, pp. 1–3, 2012.

[77] IDT, "ADC1413D series - Product Datasheet," 2012.

[78] JEDEC STANDARD, "Serial Interface for Data Converters - JESD204B," South Arlington, 2012.

[79] D. Barrientos et al., "Multiple register synchronization with a high-speed serial link using the aurora protocol," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 5, pp. 3521–3525, 2013.

[80] D. Barrientos, "Contributions to the new electronics of the AGATA gamma tracking detector. Design, implementation, test and integration of the digitizers control card," University of Valencia, 2013.

[81] A. Georgiev, W. Gast, and R. M. Lieder, "An Analog-to-Digital Conversion Based on a Moving Window Deconvolution," *IEEE Trans. Nucl. Sci.*, vol. 41, no. 4, pp. 1116–1124, 1994.

[82] A. Georgiev and W. Gast, “Digital Pulse Processing in High Resolution, High Throughput Gamma-Ray Spectroscopy,” *IEEE Trans. Nucl. Sci.*, vol. 40, no. 4, pp. 770–779, 1993.

[83] PICMG - Open Modular Computing Systems, “AdvancedTCA ® Base Specification - Revision 3.0,” 2015.

[84] A. Triossi, D. Barrientos, M. Bellato, D. Bortolato, R. Isocrate, G. Rampazzo, and S. Ventura, “A PCI express optical link based on low-cost transceivers qualified for radiation hardness,” in *Journal of Instrumentation*, 2013, vol. 8, no. 2.

[85] X. Grave, R. Canedo, J. F. Clavelin, S. Du, and E. Legay, “NARVAL a modular distributed data acquisition system with Ada 95 and RTAI,” in *14th IEEE-NPSS Real Time Conference, 2005.*, 2005, p. 5 pp.-pp.

[86] Rittal, “Chiller TopTherm 1 - 6 kW – SK 3318.610 Datasheet,” p. 4, 2017.

[87] Maxim Integrated, “MAX11606–MAX11611 Datasheet,” 2013.

[88] Lattice Semiconductor, “DS1015 - ispPAC POWR1220AT8 Data Sheet,” 2012.

[89] Maxim Integrated, “MAX6625/MAX6626 Datasheet,” 2016.

[90] Analog Devices, “AD5251/AD5252 Potentiometer Datasheet,” 2012.

[91] D. Barrientos et al., “Graphical user interface for serial protocols through a USB link,” *2012 18th IEEE-NPSS Real Time Conf. RT 2012*, pp. 0–3, 2012.

[92] National Instruments, “Installation Guide - Bnc-2110,” 2007.

[93] National Instruments, “NI 6115/6120 Specifications,” 2018.

[94] J. Collado et al., “A New Preprocessing and Control Board for the Phase 2 Electronics of AGATA Experiment,” in *Real Time Conference (RT), 2016 IEEE-NPSS*, 2016.

[95] J. Collado, V. González, S. Member, J. M. Blasco, E. Sanchis, and S. Member, “Design of a mezzanine card with bandwidth aggregation for HPGe gamma spectroscopy,” in *2016 IEEE Nuclear Science Symposium, Medical Imaging Conference and Room-Temperature Semiconductor Detector Workshop (NSS/MIC/RTSD), Strasbourg, 2016*, 2016, pp. 1–2.

[96] Amphenol ICC, “MEG-Array. Proven BGA connector for reliabilityand high data rates.,” 2019.

[97] Vme. I. T. Association / American National Standards Institute., “American National Standard for FPGA Mezzanine Card (FMC) Standard, ANSI Standard ANSI/VITA 57.1-2008,” 2008.

[98] Xilinx Inc., “UltraScale Architecture and Product Overview Summary of Features Processing System. Specification, Preliminary Product Resources, Device,” 2015.

[99] R. Frazier, “The IPbus Protocol: An IP-based control protocol for ATCA/pTCA,” *Cern. Switz.*, 2013.

[100] D. Sidler, G. Alonso, M. Blott, K. Karras, K. Vissers, and R. Carley, “Scalable 10Gbps TCP/IP stack architecture for reconfigurable hardware,” in *Proceedings - 2015 IEEE 23rd Annual International Symposium on Field-Programmable Custom Computing Machines, FCCM 2015*, 2015, pp. 36–43.

[101] Xilinx Inc., “Aurora 64B/66B v12.0 - PG074,” 2019.

[102] Trenz Electronic, “TE0808 Technical Reference Manual v.32,” 2019.

[103] US Conec, “PRIZM ® LightTurn ® Solutions,” 2019.

[104] Texas Intruments, “TLK10022 datasheet.” [Online]. Available: http://www.ti.com/product/TLK10022. [Accessed: 07-Dec-2016].

[105] A. P. M. . Moelands and H. Schutte, “Two-Wire bus-system comprising a clock wire and a data wire for interconnecting a number of stations.,” 1987.

[106] Cadence, “Cadence Schematic Capture Datasheet,” 2013.

[107] Cadence, “Allegro PCB Design Solution Datasheet.”

[108] Lattice Semiconductor, “8b/10b Encoder/Decoder - RD1012,” 2015.

[109] J. Harris, “Understanding layers in the JESD204B specification : A high speed ADC perspective - MS-2714,” 2017.

[110] Xilinx Inc., “JESD204 v7.1 LogiCore IP Product Guide - PG066,” 2016.

[111] Hitech Global, “HiTech Global Kintex ® UltraScale ™ PCI Express Development Platform HTG-K800 User Manual,” 2015.

[112] Xilinx Inc., “Zynq UltraScale + MPSoC Data Sheet : Overview - DS891 v1.7,” 2018.

[113] R. Stephens, “Jitter 360º Knowledge Series.”

[114] Xilinx, “PG173 - IBERT for UltraScale GTH Transceivers v1.4,” 2018.

[115] Q. Dou and J. A. Abraham, “Jitter decomposition in high-speed communication systems,” *Proc. - 13th IEEE Eur. Test Symp. ETS 2008*, pp. 157–162, 2008.

Appendix A

The IDM FMC pinout and signal connection.

The Vita 57.1 signal names for ASP-134488-01

N	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
29	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK (JTAG)	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI (JTAG)	SCL (TWI)	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO (JTAG)	SDA (TWI)	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS (JTAG)	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L (JTAG)	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

High Speed Differential Signals (<10Gbps) From Motherboard	High Speed Differential Signals (<10G) From FMC (IDM)	High Speed Signals GBT Clocks
Low Speed Differential Signals (<2Gbps) LA port user data – 34 lines (User) Low Pin Count (LPC) Compatibility	Low Speed Differential Signals (<2Gbps) HB port user data – 22 lines (User) High Pin Count (HPC) Exclusive	Low Speed Differential Signals (<2Gbps) HA port user data – 24 lines (User) High Pin Count (HPC) Exclusive
Common Signals: Serial TWI, enable, reset, JTAG, VIO	Common clocks – 4: 0 and 1 are mezzanine to motherboard, 2 and 3 bidirectional (Select with CLK_DIR)	Power Supply Voltage: 1.8 V
Power Supply Voltage: 12V	Power Supply Voltage: 3,3V	Ground Plane Connection (GND)

Legend

Signals from the IDM to the ASP-134488-01

N	K	J	H	G	F	E	D	C	B	A
1	NC	GND	NC	GND	NC	GND	NC	GND	FPGA_CLK_DIR	GND
2	GND	FMC_CLK_B_1_P	PRSNT_L	CLK_AUX_FMC_P	GND	NC	GND	NC	GND	HSL_9_P
3	GND	FMC_CLK_B_1_N	GND	CLK_AUX_FMC_N	GND	NC	GND	NC	GND	HSL_9_N
4	FMC_CLK_B_0_P	GND	CLK_FMC_P	GND	NC	GND	GBTCLK _P	GND	HSL_8_P	GND
5	FMC_CLK_B_0_N	GND	CLK_FMC_N	GND	NC	GND	GBTCLK_N	GND	HSL_8_N	GND
6	GND	NC	GND	FMC_SDO	GND	NC	GND	HSL_7_P	GND	HSL_6_P
7	NC	NC	FMC_I2C_SEL	FMC_SDK	NC	NC	GND	HSL_7_N	GND	HSL_6_N
8	NC	GND	LA02_N	GND	NC	GND	FMC_SS	GND	HSL_5_P	GND
9	GND	NC	GND	NC	GND	NC	FMC_SDI	GND	HSL_5_N	GND
10	NC	NC	NC	NC	NC	NC	GND	NC	GND	HSL_4_P
11	NC	GND	NC	GND	NC	GND	NC	NC	GND	HSL_4_N
12	GND	NC	NC	NC	GND	NC	NC	GND	HSL_3_P	GND
13	NC	NC	NC	NC	NC	NC	GND	GND	HSL_3_N	GND
14	NC	GND	NC	GND	NC	GND	NC	NC	GND	HSL_2_P
15	GND	NC	NC	NC	GND	NC	NC	NC	GND	HSL_2_N
16	NC	NC	NC	NC	NC	NC	GND	GND	HSL_1_P	GND
17	NC	GND	NC	GND	NC	GND	NC	GND	HSL_1_N	GND
18	GND	NC	GND	NC	GND	NC	NC	NC	GND	HSL_0_P
29	NC	NC	NC	NC	NC	NC	GND	NC	GND	HSL_0_N
20	NC	GND	NC	GND	NC	GND	NC	GND	NC	GND
21	GND	NC	GND	NC	GND	NC	NC	GND	NC	GND
22	NC	NC	NC	NC	FPGA_DS02_P	NC	GND	NC	GND	NC
23	NC	GND	NC	GND	FPGA_DS02_N	GND	NC	NC	GND	NC
24	GND	NC	GND	NC	GND	NC	NC	GND	NC	GND
25	NC	NC	NC	NC	NC	NC	GND	GND	NC	GND
26	NC	GND	NC	GND	NC	GND	NC	NC	GND	NC
27	GND	NC	GND	NC	GND	NC	NC	NC	GND	NC
28	NC	NC	NC	NC	NC	NC	GND	GND	NC	GND
29	NC	GND	NC	GND	NC	GND	NC	GND	NC	GND
30	GND	NC	GND	NC	GND	NC	NC	FMC_I2C_SCL	GND	NC
31	NC	NC	NC	NC	NC	NC	NC	FMC_I2C_SDA	GND	NC
32	NC	GND	NC	GND	NC	GND	fmc3p3vaux	GND	NC	GND
33	GND	NC	GND	NC	GND	NC	NC	GND	NC	GND
34	NC	NC	NC	NC	NC	NC	NC	GA0	GND	NC
35	NC	GND	NC	GND	NC	GND	NC	fmc12p0v	GND	NC
36	GND	NC	GND	NC	GND	NC	fmc3p3v	GND	NC	GND
37	NC	NC	NC	NC	NC	NC	GND	fmc12p0v	NC	GND
38	NC	GND	NC	GND	NC	GND	fmc3p3v	GND	GND	NC
39	GND	VIO_B_M2C	GND	fmcVadj	GND	fmcVadj	GND	fmc3p3v	GND	NC
40	VIO_B_M2C	GND	fmcVadj	GND	fmcVadj	GND	fmc3p3v	GND	NC	GND

Appendix B

The ICE40LP pinout connection to IDM

Ball Function	Pin Type	Bank	(CM121) Ball Number	Connection
IOL_2 (A,B)	DPIO	3	B1,B2	NC
IOL_4 (A,B)	DPIO	3	C4,C3	NC
IOL_5 (A,B)	DPIO	3	C2,C1	FMC_FPGA_DS02_N/_P
IOL_8 (A,B)	DPIO	3	E1,D1	INTPWR / PLL_REFSEL
IOL_9 (A,B)	DPIO	3	D2,D3	NC
IOL_10 (A,B)	DPIO	3	E2,E3	NC
IOL_12 (A,B)	DPIO	3	F1,F2	NC
IOL_13_GBIN7	GBIN	3	F3	CLK_FMC_P (Main Clk P)
IOL_14_GBIN6	GBIN	3	G1	CLK_FMC_N (Main Clk N)
IOL_13_A	GBIN	3	F3	PLL_GPIO [0]
IOL_14_B	GBIN	3	G1	PLL_GPIO [1]
IOL_17 (A,B)	DPIO	3	G3,H3	PLL_GPIO [2:3]
IOL_18 (A,B)	DPIO	3	H1,H2	PLL_GPIO [4:5]
IOL_23 (A,B)	DPIO	3	J1,K1	FPGA_CLK_REFIN_N/_P
IOL_25A	DPIO	3	K2	FPGA_CLK_REF_N
IOL_25B	DPIO	3	J2	FPGA_CLK_REF_P
IOB_56	PIO	2	L1	OPT_SDA – I2C/TWI data to optical transceivers (internal pull up)
IOB_57	PIO	2	J3	OPT_SCL– I2C/TWI clock to optical transceivers (internal pull up)
IOB_61	PIO	2	L2	OPTRST – optical transceivers reset signal (internal pull up)
IOB_63/64/71/72	PIO	2	K3,J4,L3,L4	INTL – optical transceivers alert interrupt 0-63 (IC2) 1-64 (IC3) 2-71(IC4) 3-72(IC5) (internal pull up)
IOB_73	PIO	2	K4	PLL_PDN (Power Down PLL)
IOB_78	PIO	2	J5	NC
IOB_79	PIO	2	K5	SEN_SDA – Temperature and voltage sensor I2C channel - Data
IOB_81_GBIN5	GBIN	2	L5	PLL_STATUS[1]
IOB_82_GBIN4	GBIN	2	K6	PLL_STATUS[0]

Ball Function	Pin Type	Bank	(CM121) Ball Number	Connection
IOB_86	PIO	2	J7	SEN_SCL – Temperature and voltage sensor I2C channel - Clock
IOB_87	PIO	2	H7	FMC_SDA – Master FPGA I2C channel - Data
IOB_89	PIO	2	K7	FMC_SDA – Master FPGA I2C channel - Clock
IOB_91	PIO	2	J8	FMC_SDA – Master FPGA I2C Selector – On: Master Control Off: Autonomous Mezzanine
IOB_94	PIO	2	L7	FPGA_CLK_DIR
IOB_103_CBSEL0	PIO	2	L8	NC
IOB_104_CBSEL1	PIO	2	H9	NC
IOB_105_SDO	SPI	SPI	K9	To FPGA Programming Region
IOB_106_SDI	SPI	SPI	J9	To FPGA Programming Region
IOB_107_SCK	SPI	SPI	L10	To FPGA Programming Region
IOB_108_SS	SPI	SPI	K10	To FPGA Programming Region
IOR_114	PIO	1	J11	SEL0_LOAD (Clock Selector 0)
IOR_115	PIO	1	K11	SEL0_MODE (Clock Selector 0)
IOR_116	PIO	1	H10	SEL0_SISEL (Clock Selector 0)
IOR_117	PIO	1	J10	SEL0_SCLK (Clock Selector 0)
IOR_118	PIO	1	G8	SEL1_LOAD (Clock Selector 1)
IOR_119	PIO	1	H11	SEL1_MODE (Clock Selector 1)
IOR_120	PIO	1	G10	SEL1_SISEL (Clock Selector 1)
IOR_128	PIO	1	G9	SEL1_SEL0 (Clock Selector 1)
IOR_129	PIO	1	G11	SEL1_CLK (Clock Selector 1)
IOR_136	PIO	1	F10	NC
IOR_137	PIO	1	F9	LED8(Green)
IOR_140_GBIN3	GBIN	1	F11	SEL0_SEL0 (Clock Selector 0)
IOR_141_GBIN2	GBIN	1	E10	NC
IOR_144	PIO	1	E9	LED7(Green)
IOR_146	PIO	1	E8	NC
IOR_147	PIO	1	D9	LED6(Green)
IOR_148	PIO	1	E11	LED5(Yellow)
IOR_152	PIO	1	D11	LED4 (Yellow(
IOR_154	PIO	1	D10	LED3 (Red)
IOR_160	PIO	1	C11	LED2 (Red)
IOR_161	PIO	1	B11	LED1 (Red)

Ball Function	Pin Type	Bank	(CM121) Ball Number	Connection
IOT_168/170/172/ 174/177/178/179/ 181/190/191	PIO	0	A11, A10, C9, B9, B8, A9, C8, D7, A8, C7	LOS [9:0] – connected to each channel LOS link aggregator signal. If some problem on data turns 1.
IOT_192	PIO	0	A7	MDC (TLK10022 Serial Clock)
IOT_197_GBIN1	GBIN	0	B7	PBE0 (TLK10022 4 port B enable)
IOT_198_GBIN0	GBIN	0	B6	LARST (TLK10022 reset)
IOT_206	PIO	0	A6	MDIO (TLK10022 Serial Data)
IOT_207	PIO	0	A5	PAE0 (TLK10022 0 port A enable)
IOT_208	PIO	0	B5	PAE1 (TLK10022 1 port A enable)
IOT_211	PIO	0	A4	PAE2 (TLK10022 2 port A enable)
IOT_212	PIO	0	D5	PAE3 (TLK10022 3 port A enable)
IOT_219	PIO	0	B4	PAE4 (TLK10022 4 port A enable)
IOT_221	PIO	0	B3	PBE0 (TLK10022 0 port B enable)
IOT_222	PIO	0	A2	PBE1 (TLK10022 1 port B enable)
IOT_223	PIO	0	A3	PBE2 (TLK10022 2 port B enable)
IOT_225	PIO	0	A1	PBE3 (TLK10022 3 port B enable)
GND	GND	GND	H5,G7,G6,G5, F7,F6, F5, E7, E6, E5	DGND
VCC	VCC	VCC	D4, D8,H4,H8	P1V2core (1.2 V)
VCCPLL0,VCCPLL1	VCCPLL	VCCPLL	J6,C6	P1V2pll (1.2 V)
GNDPLL0,GNDPLL1	GNDPLL	GNDPLL	L6,C5	DGND
VCCIO_0-3	VCCIO	VCCIO	D6,F8,H6,E4,G4	0:P1V8Core – 1:P2V5 – 2/3: P3V3
VPP_FAST	VPP	VPP	B10	NC
VPP_2V5	VPP	VPP	C10	P2V5 (2.5V)
CRESET_B	CONFIG	2	L9	P3V3 (Always On)
CDONE	CONFIG	2	K8	LED: LD10 (3.3V with 4k7)
VCC_SPI	SPI	SPI	L11	P3V3 (3.3 V)

Appendix C

The IDM memory map table and commands

Appendix D

Resumen en Castellano.

Introducción

En el campo de la física nuclear, la espectroscopia de rayos gamma de alta resolución es un método preciso para estudiar la estructura del núcleo, extrayendo la energía y la distribución angular de los fotones gamma emitidos en las transiciones entre estados nucleares. Para obtener núcleos en un estado excitado y que, por tanto, emitan rayos gamma, hemos de hacer chocar la materia, produciendo reacciones nucleares (espectroscopia de haz) o recurrir a desintegraciones radiactivas (espectroscopia de desintegración). Los detectores de semiconductor de germanio de alta pureza (HPGe) han demostrado tener una buena respuesta interaccionando con rayos gamma. Al igual que otros detectores basados en semiconductores, cuando se los somete a alto voltaje, los detectores HPGe producen una alta corriente de medida proporcional a la energía de los rayos gamma incidentes.

El multi-detector HPGe AGATA (Advanced GAmma Tracking Array) es uno de los espectrómetros gamma más avanzados que existen dedicado al estudio de la física nuclear. Para maximizar la sensibilidad, los detectores HPGe de AGATA tienen los contactos exteriores divididos en 36 segmentos. De este modo se puede determinar la posición del fotón y la energía depositada en cada una de estas partes. Con la información sobre la posición y la energía de los fotones es posible reconstruir las interacciones de los rayos gamma a través de los algoritmos de tracking. Gracias a esta técnica, es posible maximizar la sensibilidad el detector (resolución energética y factor P/T) sin necesidad de utilizar parte del ángulo sólido de detección para otros detectores dedicados a la supresión del Compton. Además de los detectores en sí mismos, los arrays de detectores de HPGe sensibles al posicionamiento requieren una electrónica de muestreo con ratios señal a ruido de calidad espectroscópica que capturen y digitalicen las trazas para ser procesadas por los algoritmos de análisis de forma de pulso (Pulse Shape Analysis).

Para conseguir la máxima sensibilidad y eficiencia, el proyecto AGATA busca construir el multi-detector cubriendo una superficie total con 4π de ángulo sólido, optimizando la información obtenida, algo especialmente crítico en experimentos que usan costosos haces de iones radiactivos. Otro objetivo en la construcción de AGATA es su movilidad. AGATA se instalará en diferentes laboratorios para aprovechar la variedad de haces e instrumentación complementaria que existen en los diferentes centros europeos de Física Nuclear.

El proyecto AGATA se encuentra actualmente en su Fase 1, que busca cubrir hasta 1π de ángulo sólido y se encuentra con la segunda generación electrónica implementada. Esto implica instrumentar 45 detectores que actualmente utilizan, en parte, la anterior generación o Fase 0, que fue diseñada y producida entre 2005 y 2007. El principal objetivo a nivel de electrónica en la colaboración AGATA es el desarrollo de la nueva generación para la Fase 2, que busca instrumentar 180 detectores y la cual se ha desarrollado parcialmente en esta tesis. Los principales objetivos de la electrónica para la Fase 2 son la integración en un solo dispositivo, desde la digitalización hasta la salida de datos y el protocolo Ethernet como comunicación para dicha salida. La tecnología Ethernet permitirá una conexión multipunto y la posibilidad de leer los datos desde cualquier sitio de la granja de procesado de AGATA.

Uno de los grandes problemas que se encuentran en la integración de todo el Sistema es la optimización de los recursos en la FPGA por parte del Preprocesado. Con el avance de la tecnología, a pesar del aumento de la tasa de datos en los transceptores de alta velocidad de estos dispositivos (entre 16 y 32 Gbps), el número de ellos no se ha incrementado especialmente. Además, el coste las FPGA aumenta sustancialmente con el número de transceptores. Esto es un problema crítico en AGATA ya que requiere un gran número de canales digitalizados por dispositivo, pero no a una velocidad especialmente alta, en la práctica sobre 2 Gbps. Para reducir la complejidad del sistema, el coste y la potencia total, el número de líneas de alta velocidad se ha optimizado mediante agregación de datos por multiplexado en el tiempo, incrementando la velocidad de la tasa de datos, pero con una reducción en el número total de estas de 4 a 1. Esta solución se ha llevado a

cabo a través de la tarjeta Input Data Mezzanine, concebida y desarrollada enteramente en esta tesis.

El objetivo principal desde el punto de vista científico es demostrar la posibilidad de leer 40 canales mediante el protocolo JESD204 o uno equivalente, vía fibra óptica o por cable físico, únicamente con 10 transceptores de alta velocidad de una FPGA, gracias a la técnica de multiplexado por división en el tiempo. La base de la que se parte es la electrónica actual de AGATA y se apoya en tecnología del estado del arte sobre diseño hardware y software para FPGAs, diseño digital de alta velocidad y comunicaciones digitales. A pesar de que este diseño se ha realizado principalmente para el proyecto AGATA, consideramos que esta tecnología será de interés para otros instrumentos y aplicaciones.

Resumen

En el capítulo 1 se empieza definiendo los conceptos básicos de la física nuclear y se presenta una descripción de la espectroscopia gamma. La física nuclear se centra en el estudio del núcleo atómico y para ello hay entender que se trata de un problema de múltiples cuerpos. Los núcleos se conforman de protones y neutrones agrupados en capas, donde el número de protones define el elemento químico. El número total de neutrones puede variar dentro de un elemento generando lo que se conoce como isótopos. Bajo este concepto se evoluciona de la tabla periódica a la tabla de nucleídos (Fig. 1.1), donde existen núcleos más o menos inestables. Estos núcleos inestables se desintegran con emisión de partículas generando nuevos elementos.

Tanto los estados excitados poblados en la desintegración como los creados en reacciones nucleares, pueden desexcitarse emitiendo rayos gamma que pueden ser leídos a través de espectrómetros para determinar los estados del núcleo y sus propiedades.

La introducción continúa con la descripción de la interacción de la radiación gamma con la materia para entender el desarrollo de los detectores. En él se presentan los tres fenómenos importantes que ocurren para las energías relacionadas (0.1-20 MeV): absorción fotoeléctrica, dispersión Compton y producción de pares. Se continúa con una breve descripción de los tipos de detectores que se pueden encontrar, como pueden ser

cámaras de ionización de gases, centelladores y fotomultiplicadores, contadores Geiger y dispositivos basados en semiconductor (Fig. 1.5). El último caso es en el que se centra el trabajo debido a su mayor eficiencia energética.

A continuación, se profundiza en la detección de rayos gamma a través de dispositivos semiconductores basados en germanio, el elemento semiconductor que ha proporcionado detectores con la mejor resolución energética. Se introducen los conceptos de eficiencia del detector, Peak-to-Total y resolución energética, acompañado del desarrollo histórico que se ha producido en los detectores de germanio hasta llegar al HPGe (Germanio de alta pureza).

Una vez presentados los detectores de germanio se presenta el concepto de multi-detector (Detector Array) y se describe la evolución a lo largo de los años. También se introducen brevemente los diferentes conceptos de aceleradores que se utilizan en espectroscopia gamma para preparar reacciones nucleares y colisiones. Todo este desarrollo nos acerca al concepto de detectores de germanio con posicionamiento y a la idea del Tracking, ya que el conocimiento de las trazas por donde pasa el fotón (Fig. 1.9/ Fig. 1.8), mejora la sensibilidad del detector y la información que se puede extraer de cada interacción. Este concepto se encuentra actualmente en dos multi-detectores de HPGe, GRETA en los Estados Unidos de América y AGATA (Fig. 1.13) en Europa, el detector para el que se ha desarrollado la electrónica de esta tesis.

La segunda parte de la introducción se centra en la tecnología sobre la que se ha trabajado, el estado del arte en tecnología de enlaces de alta velocidad, comunicaciones ópticas, instrumentación, FPGAs y procesamiento paralelo.

En el capítulo 2, se presenta la electrónica de AGATA en cada una de sus etapas y generaciones. Partiendo del preamplificador que adapta la carga del detector a un pulso y lo transmite a los digitalizadores. Los digitalizadores adaptan las 38 señales analógicas que vienen del preamplificador y las transforman en señales digitales. La digitalización de la señal es un punto crítico para el tracking en detectores segmentados ya que se debe guardar y procesar posteriormente para obtener el punto de interacción.

Tras la digitalización se realiza un procesado previo (Pre-processing), implementado en FPGA, en el que se extrae la energía y se reduce la cantidad de datos entrantes a partir de un sistema de trigger. Solo interesan los datos de los cristales donde se ha producido interacción con los rayos gamma por lo que se realiza un trigger local para cada cristal cuando se recibe un pulso. Cada vez que se produce, este trigger se envía al sistema de trigger global GTS para que coteje el evento con el resto de cristales del detector y otros posibles detectores auxiliares. Si es un evento válido, entonces se envía a la granja de procesado. Respecto a la energía calculada, se consigue mediante el algoritmo de "Moving Window Deconvolution" para cada canal y se envía junto con las trazas de los eventos validados.

Estos datos se reciben en la granja de procesado donde se aplican los algoritmos de análisis de la forma del pulso (Pulse Shape Analysis, PSA), para extraer las trayectorias de los fotones y la energía depositada. Tras esto, los datos se compilan en eventos con los datos de todos los cristales del detector en el Event Builder y se combinan con los datos de los detectores auxiliares que se estén utilizando junto a AGATA. Estos resultados se guardan en disco para realizar los cálculos necesarios mediante los algoritmos de Tracking o aquellos particulares de cada experimento.

En el último punto del capítulo se definen los requerimientos y criterios que se exigirán a la electrónica para la Fase 2 del detector:

1- Completar la electrónica para los 180 detectores.

2- Incrementar el nivel de integración electrónica.

3- Deshacerse del enlace punto a punto PCI-E entre el pre procesado y el PSA a través de una conexión estándar 10 Gbps Ethernet, incrementar el ancho de banda de datos entre estos dos últimos elementos.

4- Incrementar el nivel de modularidad para ser compatible con generaciones previas y futuras.

5- Establecer contratos de mantenimiento de la electrónica con empresas que aseguren la producción hasta que termine la fase 2 en 2030.

6- Implementar un sistema de monitorización avanzado y de fácil manejo, para supervisión durante experimentos y mantenimiento entre ellos.

Existen dos generaciones de electrónica actualmente, la Fase 0 y la Fase 1. La funcionalidad es la misma en ambas, pero la Fase 1 mejora a la anterior en integración electrónica, reducción de costes, optimización del número de conexiones y simplificación del sistema.

La tesis se centra en el desarrollo de la tecnología para la Fase 2. Para ello se requiere entender bien la Fase 1 y sus problemas para tener un punto de partida para la siguiente generación. En el capítulo 3 se muestra el estudio y los trabajos realizados con la electrónica de la Fase 1 para entender los problemas que surgen y estudiar las posibles mejoras. Se presenta el entorno de test desarrollado para caracterizar la caja digitalizadora de la electrónica de la Fase 1, la tarjeta de procesado y la fuente de alimentación. Este entorno de test se compone de una cadena completa de la electrónica del detector, donde se puede sustituir uno de los elementos previamente mencionados para verificarlo. Además, se han desarrollado una serie de herramientas para realizar lecturas de temperaturas en varios puntos y de los voltajes de cada alimentación.

El capítulo 4 explica el diseño propuesto para la electrónica de Fase 2, con una mayor integración, salida de datos Ethernet e incremento de la capacidad de cómputo del preprocesado para poder añadir futuras funcionalidades. El elemento crítico en la integración que se plantea es el problema de optimización de las líneas de datos de alta velocidad, a través de los transceptores, en la FPGA de pre-procesado. Como se ha mencionado antes, las FPGA modernas disponen de un número limitado de transceptores en función de la gama que se elija, pero estos siempre disponen de una gran tasa de datos, entre 16 Gbps y 32 Gbps.

Los datos digitalizados en AGATA tiene una tasa de 2 Gbps y tenemos 38 señales por cristal; por tanto, no aprovechar el ancho de banda de los transceptores supone un problema por la falta de optimización de los recursos, ya que una sola FPGA podría realizar el preprocesado de las 38 señales. La solución a este problema se desarrolla en esta tesis como un multiplexado en el tiempo de las líneas de datos provenientes de los

digitalizadores. Para ello se ha desarrollado una tarjeta mezzanine llamada IDM (Input Data Mezzanine) que realiza la reducción de líneas en factor 4 a 1, dejando la necesidad de transceptores por FPGA en 10 líneas de 8 Gbps.

La electrónica de la Fase 2 incorpora una segunda parte además del pre-procesado. Se trata de la salida de datos Ethernet. Ésta se ha desarrollado en una versión prototipo con otra tarjeta mezzanine llamada STARE por compañeros de la colaboración AGATA en CSNSM Orsay (Francia). Esta tarjeta comunica con los servidores que realizan el cálculo del PSA a través de cuatro líneas de 10 Gbps Ethernet: dos destinadas a los datos, una exclusiva para la monitorización y una libre para futuras mejoras.

Todo el preprocesado se realiza en una FPGA implementada en un System On Module (SOM), una tarjeta acoplable a una placa madre a modo de mezzanine que incorpora: la FPGA, memoria DDR, alimentación y las conexiones de programación en muy poco espacio. En la SOM seleccionada se encuentra una FPGA de Xilinx Zynq Ultrascale+ con más de 700.000 bloques lógicos, 16 transceptores diferenciales de alta velocidad (16 Gbps), un procesador ARM Cortex A52 de cuatro núcleos y un microcontrolador ARM Cortex M4 de dos núcleos. Este dispositivo SOM se inserta en una motherboard basada en la IDM (Fig. 4.8) en combinación con STARE y con la electrónica necesaria para ser una hoja del árbol de trigger (GTS).

En el capítulo 5 se describe el diseño y los análisis de integridad de la señal realizados para crear el prototipo de la tarjeta. Se detallan los componentes seleccionados y el desarrollo del firmware local de control de la tarjeta IDM, que funciona de manera autónoma e inteligente. Para ello se le ha incorporado una FPGA Lattice ICE40LP de bajo coste y bajo consumo. En esta tarjeta se ha desarrollado un firmware que recopila la información de todos los integrados y permite controlarlos a como si de un único dispositivo TWI (o I2C) se tratara. Desde el punto de vista de la tarjeta madre, el dispositivo tiene un mapa de memoria con todos los componentes direccionados y con una serie de comandos para realizar un control cómodo.

La tarjeta tiene un coste de prototipo de alrededor 2500 € y se calcula que tendrá un coste final en producción de menos de 750 €. La tarjeta se basa en el integrado TLK10022

de Texas Instruments para realizar el multiplexado en tiempo. Dentro del capítulo se explican los relojes necesarios para que éste integrado trabaje correctamente y se describe la delicada alimentación que requiere. En el apartado 4 del capítulo se describen los test realizados con el software de simulación, para todas las señales de alta velocidad (8 Gbps y 2 Gbps) en condiciones de funcionamiento normal. También se presenta la simulación del sistema de alimentación y la representación en 3D para análisis mecánicos. Por último, se introducen las complejidades y los problemas que se han debido afrontar en el diseño y la producción, ya que se trata de un diseño de alta velocidad y de tamaño reducido.

Se realizaron dos producciones de prototipos para validar el concepto de la agregación de datos en este entorno. El capítulo 6 describe los test realizados para demostrar el método de multiplexado y la validación de la tarjeta IDM. En el mismo capítulo se describe también, ya que se ha realizado en el contexto de esta tesis, la prueba de concepto de la electrónica completa de la Fase 2, demostrando la viabilidad de leer los datos a través del protocolo estándar 10 Gbps Ethernet.

El capítulo 6 sirve además como descripción del firmware desarrollado en el preprocesado, centrándose en la parte desarrollada en la tesis que es el módulo de recepción de datos de los digitalizadores. En el módulo de recepción se realiza la deserialización de los datos a 8 Gbps y el desentrelazado para recuperar las cuatro líneas de datos originales por cada línea de alta velocidad. Tras el desentrelazado, se decodifica el protocolo JESD204 y se alinean los 38 canales mediante los buffers elásticos. La alineación de los 38 canales se realiza enviando un patrón conocido a los ADC y comparando la diferencia de tiempos entre las diferentes recepciones de datos. Los buffers elásticos ajustan la latencia de todas las líneas al valor mayor de todas ellas, de este modo todos los datos llegan a la vez.

La validación de la tarjeta IDM se aborda realizando el test de cada uno de los enlaces independientemente. El camino de datos A se define como la comunicación entre los digitalizadores y el agregador TLK10022 a través de fibra óptica. El camino de datos B se define como la comunicación entre el agregador y la FPGA de preprocesado que se encuentra en la placa madre. Se define también un último camino C que corresponde a la

comunicación entre la FPGA y la tarjeta STARE, ya que es el que se verifica en la prueba de concepto de la Fase 2. El camino A trabaja con de líneas de datos a 2 Gbps y se verifica a través de señales de test pseudoaleatorios PRBS recibidas y verificadas en el TLK10022.

El camino B emplea líneas de datos a 8 Gbps y permite realizar un número mayor de tests dado que en uno de los extremos se encuentra la FPGA. Para el camino B se han obtenido los diagramas de ojo (Fig. 6.10) y se ha validado la recepción con datos producidos en el agregador. El último paso del test de la tarjeta prototipo IDM es la validación conjunta de los caminos A y B.

Conclusiones

Para cualquier detector con lectura digital, las características físicas definen la tasa de muestreo de los digitalizadores, En muchos casos, estas tasas de muestreo se encuentran en el orden de decenas o centenares de Mega-muestras por segundo (Msps) con un número de bits efectivos entre 8 y 16. Estos datos se serializan en señales entre 1 y 5 Gbps, con un número alto de estas en multi-detectores y mucho más en el caso de ser detectores segmentados. De todos modos, la tasa de muestreo requerida es una característica intrínseca del detector, como es el caso de AGATA, con señales a digitalizar con anchos de banda en frecuencia de hasta 30 MHz que requieren 60 Msps como mínimo, hecho que es improbable que cambie en el tiempo. En el otro lado de esta comunicación está el preprocesado y la lectura, con FPGAs o procesadores de alta capacidad con números de transceptores de alta velocidad limitados, pero con tasas de datos de orden de 16-32 Gbps y en aumento con los años. Esto representa un problema, la comunicación entre ambas partes no está optimizada, sin ninguna solución existente más que aumentar el número de FPGAs o el coste de estas. Este problema no se encuentra únicamente en instrumentación nuclear, sino que afecta a otros entornos de instrumentación con características similares.

El prototipo de tarjeta producida en esta tesis, la IDM, es una solución a este problema de optimización, con un multiplexado en tiempo de varias líneas de datos con unos pocos Gbps a la entrada de los modernos transceptores de alta velocidad de una FPGA. La tarjeta se ha validado en el contexto del detector AGATA, con un protocolo de

comunicación estándar JESD204, específico de convertidores analógico a digital y de uso común en el sector. El prototipo IDM es una tarjeta de 40 entradas ópticas en formato mezzanine estándar Vita 57.1 con una agregación de líneas de datos 4:1 de hasta 2.5 Gbps de entrada o 2:1 de hasta 5 Gbps. Esta tarjeta se basa en un chip TLK10022 de Texas Instruments para realizar el multiplexado. Acompañando el hardware, se ha desarrollado en la tesis, un código encapsulado o IP (Intellectual Property) para instanciar en la FPGA de recepción y recuperar los datos de los digitalizadores.

Como segundo objetivo de la tesis, el diseño y la producción del prototipo IDM es uno de los puntos más críticos para el desarrollo de la electrónica de AGATA para la Fase 2, ya que el problema que se ha presentado es un cuello de botella en la integración. Dentro del desarrollo de esta tesis se encuentra también la validación del concepto de Ethernet como salida de datos, para confirmar con ambas soluciones la viabilidad de esta generación electrónica.

La tesis ha contribuido activamente en el desarrollo de la nueva electrónica en la colaboración AGATA, con gran interacción entre los miembros del equipo técnico de desarrollo y feedback por parte de la comunidad científica. Este desarrollo abre un nuevo mundo de posibilidades para mejorar la investigación en física nuclear a través de AGATA. El incremento de la capacidad de la FPGA puede ser aprovechado para implementar nuevos algoritmos extracción de la energía. El extra en el ancho de banda de lectura se puede utilizar para extraer trazas de la señal más largas por evento para mejorar los algoritmos de Pulse Shape Analysis y Tracking.

El desarrollo de la IDM y su validación se han completado y, por tanto, se ha finalizado una gran parte de la investigación de la tecnología para la fase 2. No obstante, aún queda mucho trabajo. El siguiente paso es la producción de la motherboard (Fig. 7.1), basada en una combinación entre IDM y la tarjeta STARE, así como la introducción de los SOM (System On Module). Esta motherboard se espera que esté producida para el año 2021 y en funcionamiento en el detector en 2022.

Además, existe otra posible aplicación para la IDM. La tarjeta se puede preparar para producción comercial, como solución para otros detectores o sistemas de

instrumentación con digitalizadores similares y congestión en el número de líneas de datos. Esto serviría como transferencia tecnológica entre desarrollos realizados para la investigación científica hacia la industria, así como para compartir los resultados de esta tesis con la comunidad de instrumentación electrónica en todo el mundo.