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ORIGINAL RESEARCH

Enhanced asymmetrical modulation for half-bridge series resonant inverters in induction heating applications

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Abstract

This paper presents a method that improves the reliability of half-bridge (HB) series resonant inverters (SRI) for high-frequency induction heating applications. Many industrial processes, like induction heat treatments, are very repetitive. This cyclical operation represents a strong limitation of the inverter's reliability, mainly due to the accelerated stress of the power semiconductors. This method consists in an enhanced asymmetrical pulse width modulation (EAPWM) that allows distributing the losses across the components, thereby reducing the cyclic increase in junction temperature of the power devices, and thus achieves a reliability that is more than twice as high as that achieved using traditional modulation methods. The work methodology includes a theoretical study of the HB inverter and a complete analysis of losses. The presented design rules have been used to implement a 25 kW, 100 kHz inverter. The use of silicon carbide (SiC) MOSFET transistors allows reaching an efficiency greater than 99%. The analytical results obtained have been experimentally validated by testing the inverter on an induction heating test bench.

1 | INTRODUCTION

INDUCTION heating is being increasingly used in both domestic and industrial applications. In the industry it is mainly used to carry out heat treatments that require high precision, efficient energy utilization and good reliability. In this way, highly profitable industrial processes can be achieved.

Lately there has been substantial increase in the use of high-frequency converters for the heat treatment of metals in processes such as surface hardening, brazing and soldering. Most of the increases in operating frequency have been made thanks to the appearance of new semiconductor devices with improved technology and the reduction of switching losses by means of soft switching techniques [1, 2].

HB SRI topology is the most widely employed in domestic applications due to its simplicity, efficiency and cost effectiveness [3]. The use of SiC MOSFET transistors allows obtaining higher powers and frequencies, making it easier to adapt this topology to soft and medium industrial heating applications [4, 5] with good efficiency. This is crucial for ensuring reliability, maximizing output power capabilities and minimizing the size and cost of the heatsink.

Traditional square wave (SW) modulation is often used in these types of converters. Power regulation is achieved through pulse frequency modulation (PFM) always above the resonance frequency to ensure zero voltage switching (ZVS) commutation conditions [6, 7]. As the frequency and phase of the turn-off transition are raised to reduce power, the efficiency of the inverter is reduced. In the past, pulse density modulation (PDM) has been proposed to improve efficiency [8, 9, 10], but this method presents problems especially at medium and low powers.

Variable frequency asymmetrical pulse with modulation (APWM) control is a generalization of SW and classical asymmetrical duty cycle [11, 12] controls. Its modulation parameters are switching frequency and duty cycle. This control method can be regarded as an equivalent to the PS modulation normally used in full bridge inverters which cannot be used in HB inverters [13]. With this modulation it is possible to regulate the power with a reduced frequency variation achieving lower power losses.

On the other hand, the long-term reliability of semiconductor devices holds great significance in power converter as it significantly influences the product warranty cost and the

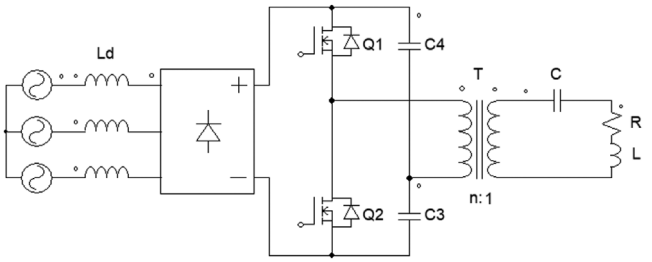

FIGURE 1 System configuration.

system reliability. The end of the life period of power modules is often defined by the thermomechanical failure mechanisms [14, 15]. One of the most important failures is the power cycling that defines the wear-out mechanisms of the bond wire on the chip. It is closely related to the temperature cycling of the die during the working condition. This effect limits the expected number of on–off cycles of the device in the function of its junction temperature swing. Since numerous industrial applications of induction heat treatment involve repetitive cycles lasting only a few seconds, this phenomenon can significantly impact the reliability of the system. This work presents a novel modulation method called EAPWM based on the variable frequency APWM. With the proposed modulation, the operating conditions of low losses and high efficiency will be maintained, maximizing the number of safe work cycles and, consequently, the reliability of the system.

The paper is structured as follows: Section 2 focuses on the configuration of the HB SRI converter. In Section 3, an analysis of the converter is conducted, followed by the design considerations for the proposed application in Section 4. Section 5 presents the analysis of power losses in the converter. In Section 6, the proposed EAPWM control method is introduced, while Section 7 compares the power cycling capability of the converter with and without the proposed method. The validation of results using experimental data is presented in Section 8. Finally, the conclusions are drawn.

2 | CONVERTER CONFIGURATION

Figure 1 shows the simplified schematic of the converter. The output power stage consists of voltage fed HB inverter using two SiC MOSFET transistors Q_1–Q_2 and two high-frequency capacitors C_3–C_4. A series resonant circuit is connected to the inverter output. This resonant circuit is composed by the resonant capacitor C, the induction heating coil L and the equivalent series resistance R [16]. Since the heating inductor in industrial induction applications requires high current, the converter uses a matching transformer T to boost the current and to adapt the impedance of the load circuit. The dc power supply for the inverter is a three-phase diode bridge rectifier connected to the 400 V, 50 Hz facility through the inductances L_d of 100 μH that improve the line current distortion [17, 18]. The nominal output power is 25 kW and the working frequency is 100 kHz. The required heating coil for the application is a three-turn inductor of 2 μH and a quality factor Q of 13.5. The transformer ratio n is 5. Table 1 shows a resume of main specifications.

TABLE 1 Converter specifications.

Component	Symbol	Value	Unit
Nominal output power	P_o	25	kW
Nominal frequency	f_o	100	kHz
DC input voltage	V_d	540	V
Resonant inductor	L	2	μH
Output quality factor	Q	13.5	
Transformer ratio	n	5	
Resonant capacitor	C	1.25	μF
Equivalent series resistor	R	9.4	mΩ

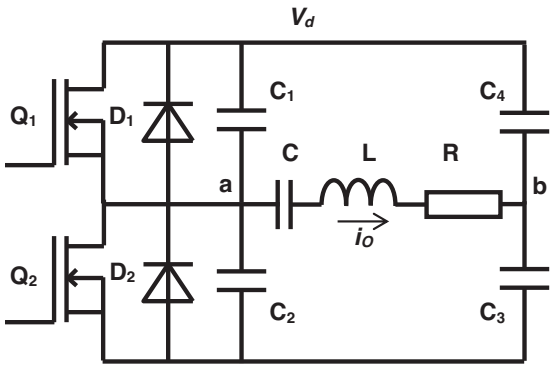

FIGURE 2 HB SRI circuit. HB, half-bridge; SRI, series resonant inverters.

The design of the resonant circuit is based in specifications mentioned above. Operating close to the series resonant frequency ($f \approx f_o$), C is determinate by

$$C = \frac{1}{\omega_o^2 L} \tag{1}$$

where $\omega_o = 2\pi f_o$. The equivalent series resonant resistor R is calculated with

$$R = \frac{L\omega_o}{Q} \tag{2}$$

Table 1 shows a resume of the main specifications of the converter and its components.

3 | ANALYSIS OF THE INVERTER

Figure 2 shows a HB SRI composed by the MOSFET transistors Q_1–Q_2, their free-wheeling diodes D_1–D_2 and two high-frequency capacitors C_3–C_4 that allow the flow of circulating current. C_1–C_2 represent the equivalent capacitance of the inverter switches including the snubber capacitor and the output capacitance of the MOSFETs. Note that the transformer T has been removed and, hence, the impedances have been

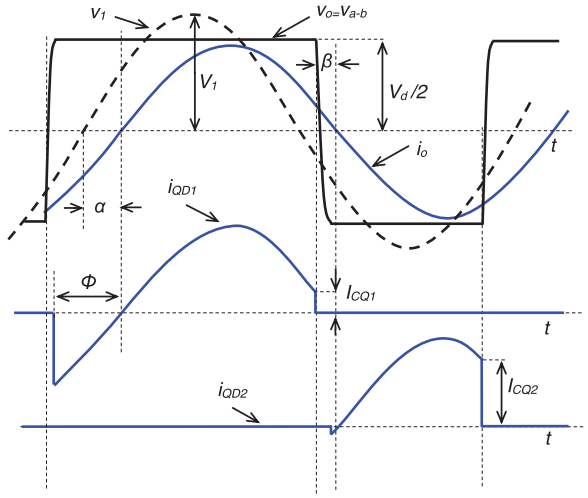

FIGURE 3 Simplified output voltage and current waveforms.

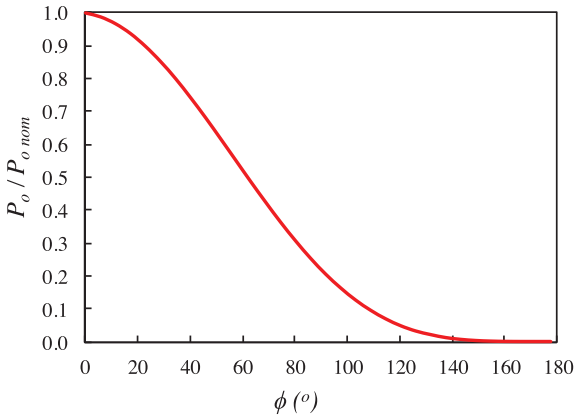

FIGURE 4 Normalized output power in front of change of phase ϕ.

transformed by the turns ratio n. The inverter is fed with the direct voltage V_d that comes from the input rectifier.

Figure 3 shows the simplified output voltage and current waveforms of the inverter. When an asymmetrical complementary pulse width modulation [19] is used, transistors Q_1 and Q_2 operate with a quasi-complementary duty cycle with the exception of dead times.

Q_1 is the high-side transistors of the inverter that switch off before the zero crossing of the output current. Q_2 is the low-side transistor and the conduction cycle of both transistors is complementary. Output power of the inverter is regulated by varying the phase-shift ϕ between switches Q_1 and Q_2. The resulting voltage across the resonant circuit is a rectangular wave. The current of the high-side and low-side transistors and diodes is i_{QD1} and i_{QD2} respectively. Note that only i_{QD2} presents a high value of the switching current I_{CQ2} (collector current being turned off).

We call v_o the voltage between points a and b (Figure 2). It represents the output voltage of the inverter and v_1 is its corresponding first harmonic whose amplitude is

$$V_1 = \frac{4V_d}{\pi\beta}\cos\left(\frac{\varphi+\beta}{2}\right)\sin\left(\frac{\beta}{2}\right) \tag{3}$$

where V_d is the average value of the dc-link voltage.

The phase between output current and output voltage and, hence, the phase of the resonant circuit impedance at the working frequency is α and the module of this impedance in the primary side of the transformer can be expressed by

$$|Z(j\omega)| = n^2\left|R + jL\omega + \frac{1}{jC\omega}\right| = \frac{n^2R}{\cos\alpha} \tag{4}$$

As the value of α is approximately equal to $(\phi+\beta)/2$ and then the amplitude of the output current is given by

$$I_o = \frac{4V_d}{\pi\beta\, n^2R}\cos^2\left(\frac{\varphi+\beta}{2}\right)\sin\left(\frac{\beta}{2}\right) \tag{5}$$

Therefore, the output power is

$$P = \frac{8V_d^2}{(\pi\beta)^2 n^2R}\cos^4\left(\frac{\varphi+\beta}{2}\right)\sin^2\left(\frac{\beta}{2}\right) \tag{6}$$

Figure 4 shows a graphic representation of the normalized output current in front of change of phase ϕ.

The phase β where the output voltage is changing from positive to negative and the output current is still positive, it is essential to determine the ZVS operation. A mathematical expression for the minimum values of β required to achieve ZVS is obtained from the following charge analysis [10]: the current in the resonant circuit must be large enough to change the voltage in the switching capacitor $C_S = C_1 + C_2$ up to $V_d/2$ (or $-V_d/2$) in the time β_{min}/ω just before the output current crosses zero. From these charge relations, β_{min} can be calculated as

$$\beta_{min} = \cos^{-1}\left(1 - \frac{\omega\, C_S V_d}{I_C}\right) \tag{7}$$

where I_C is the switching current. The phase β_{min} determines the minimum dead time between the transistors of the HB inverter. The dead time must be calculated continuously using (7) with enough safety margin. In practice it is adjusted by $\beta = 1.1\beta_{min}$.

On the other hand, the phase-shift regulation implies a change of switching frequency ω above the resonant frequency ω_o as a function of phase-shift angle as shown in the following expression [10]:

$$\omega = \omega_0\frac{\tan\left(\frac{\varphi+\beta}{2}\right) + \sqrt{\tan^2\left(\frac{\varphi+\beta}{2}\right) + 4Q^2}}{2Q} \tag{8}$$

where ω_o and Q are the resonant frequency and the quality factor of the series resonant circuit respectively:

$$\omega_o = \frac{1}{\sqrt{LC}}; \qquad Q = \frac{L\omega_o}{R} \tag{9}$$

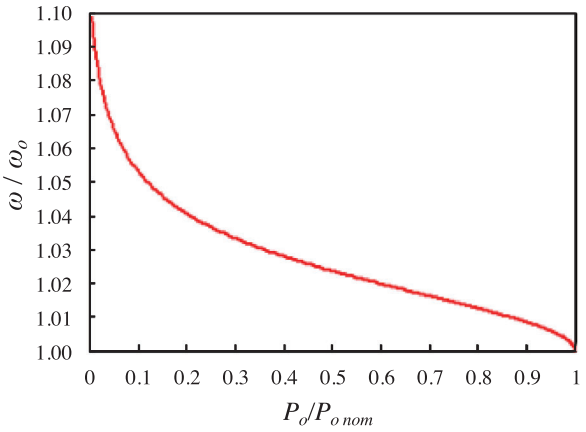

FIGURE 5 Normalized switching frequency versus normalized output power.

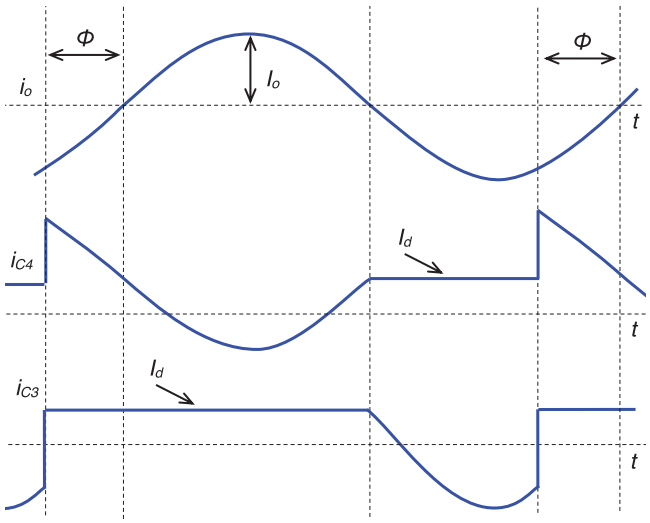

FIGURE 6 Simplified output and capacitors current waveforms.

Figure 5 shows the variations of normalized switching frequency as a function of the normalized output power.

4 | DESIGN OF THE INVERTER CAPACITORS

The design of inverter capacitors must take into account mainly the circulating high-frequency current of the inverter. Figure 6 shows the waveforms of capacitors current where the phase β has been omitted and the turn off of Q_1 is at zero current to simplify the calculations.

The root mean square (rms) of the capacitor current can be obtained from the next equations.

$$I_{C3} = \sqrt{\frac{1}{2\pi}\left(\int_0^{\pi-\varphi} (I_o \sin(\theta) - I_d)^2 d\theta + (\pi+\varphi) I_d^2\right)} \quad (10)$$

TABLE 2 Capacitor specifications.

Magnitude	Symbol	Value	Unit
Reference	C4AF1BW5330T3NK		
Rated dc voltage	V_{NDC}	500	V
Capacitance	Cap	33	μF
Equivalent series resistance	R_S	3.4	mΩ
Equivalent series inductance	ESL	15	nH
Maximum rms current	I_{rms}	26.1	A
Thermal resistance (hot spot)	R_{th}	10	K/W

$$I_{C4} = \sqrt{\frac{1}{2\pi}\left(\int_{-\varphi}^{\pi} (I_o \sin(\theta) - I_d)^2 d\theta + (\pi-\varphi) I_d^2\right)} \quad (11)$$

where I_d is the dc inverter input current that is given by (12) with enough accuracy if the efficiency η of the inverter is close to the unity:

$$I_d = \frac{P_o}{\eta V_d} \approx \frac{P_o}{V_d} \quad (12)$$

Based on the specifications provided in Table 1 for the inverter, two pieces in parallel of power film capacitors have been selected for both C_3 and C_4. The characteristic parameters are listed in Table 2.

To check the viability of the design, the temperature of the capacitor hot spot must be calculated, which must not exceed the ambient temperature by more than 30 K. This can be calculated from the losses P_{C3} and P_{C4} of each capacitor with the following expressions:

$$P_{C3} = I_{C3}^2 \frac{R_S}{2};\ P_{C4} = I_{C4}^2 \frac{R_S}{2} \quad (13)$$

$$(\Delta T_{hs})_{\max} = \frac{(P_{C3orC4})_{\max}}{2} R_{th} = 27.1\ \text{K} \quad (14)$$

5 | POWER LOSSES ANALYSIS

A power losses analysis has been carried out, considering only the contribution of conduction (P_{cd}) and switching losses (P_{sw}) of the transistors, as well as the losses of the inverter capacitor (P_C) [11, 20]. The analysis of P_{sw} focuses solely on the turn-off losses of the inverter bridge transistors, as the turn-on switching losses are negligible due to ZVS condition.

The inverter is a HB that uses only one unit for each switch. The transistors chosen are the SiC MOSFET C3M0016120K of $V_{DS} = 1200$ V and $R_{DSon} = 16$ mΩ.

Considering that both positive and negative currents flow through the resistive channel of the transistor, there are not significant losses in the diodes and the conduction losses for each transistor can be calculated only using (15).

$$P_{CD} = I_Q^2 R_{DSon} \quad (15)$$

Since the rms current of each transistor is different, the I_Q value assumes following values.

$$I_{Q1} = \sqrt{\frac{1}{2\pi}\left(\int_{-\varphi}^{\pi} (I_o \sin(\theta))^2 d\theta\right)} \quad (16)$$

$$I_{Q2} = \sqrt{\frac{1}{2\pi}\left(\int_{0}^{\pi-\varphi} (I_o \sin(\theta))^2 d\theta\right)} \quad (17)$$

On the other hand, the switching power losses of each transistor can be calculated using the graphs of the turn-off switching energy E_{off} provided by the manufacturer using the following polynomial function:

$$E_{off} = a\, I_{CQ}^2 + b\, I_{CQ} + c \quad (18)$$

where a, b and c take the following values:

$a = 0.048\ \mu J\ A^{-2}$
$b = 1.064\ \mu J\ A^{-1}$
$c = 10\ \mu J$

In (18), I_{CQ} represents the switch current of each transistor taking different values I_{CQ1} and I_{CQ2}:

$$I_{CQ1} = I_o \sin\beta \quad (19)$$

$$I_{CQ2} = I_o \sin(\pi - \varphi - \beta) \quad (20)$$

Therefore, the switching turn-off losses of each transistor can be calculated with

$$P_{SW} = E_{off} f \quad (21)$$

Since the inverter consists of two transistors and two pairs of capacitors, the total power losses are calculated using the following equation:

$$P_{tot} = P_{CD1} + P_{SW1} + P_{CD2} + P_{SW2} + P_{C3} + P_{C4} \quad (22)$$

The efficiency of the inverter can be calculated using (23).

$$\eta = \frac{P_o}{P_o + P_{tot}} \quad (23)$$

Table 3 shows the numerical results of the loss analysis for the converter specified in Table 1 operating at maximum output power.

The distribution of power losses varies significantly at different output power levels. Figure 7 shows the results of the calculation of conduction and switching losses for high- and low-side transistors and capacitors plotted against the normalized output power.

Red curves (continuous, dashed and dotted) represent the power losses of high-side components (Q_1 and C_4) while blue curves represent the power losses of low-side components (Q_2 and C_3). Note that as the output power regulation decreases, the power losses in the low-side components become larger than the losses in the high-side components. This is attributed to the increase in switching current and operating frequency.

TABLE 3 Power losses analysis.

Magnitude	Sym.	*Value*	Unit
Total transistor conduction losses	$P_{CD1} + P_{CD2}$	172	W
Total transistor switching losses	$P_{SW1} + P_{SW2}$	13.2	W
Total inverter capacitors losses	$P_{C3} + P_{C4}$	10.8	W
Total inverter power losses	P_{tot}	196	W
Efficiency	η	99.2	%

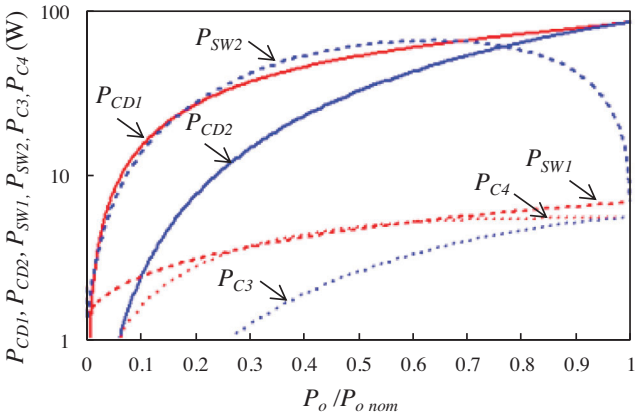

FIGURE 7 HB inverter power losses versus normalized output power. HB, half-bridge.

6 | SWITCHING SEQUENCE AND CONTROL STRATEGY

The results depicted in Figure 7 are pivotal for the development of the new switching sequence for the HB inverter, as presented in this paper. For full output power regulation, the switching and conduction losses are equal in both high and low sides of the inverter. This situation can be considered optimal for standard HB inverters. However, in other circumstances such as operating at 60% of the full power, the switching losses in the low side experience a relatively significant increase. This situation is common in industrial applications, like induction heating, in order to increase the flexibility of the whole installation. However, for a classic APWM power control HB inverter, this situation is unfavourable as it leads to a substantial increase in the temperature of the junction of Q_2, consequently causing issues with low power cycling capacity.

The problem would be solved by equally distributing the losses between the two sides of the inverter. Thus the total power losses of the inverter would remain unchanged, while the maximum junction temperature of the MOSFETs would decrease. To achieve this solution, it is necessary to extend the

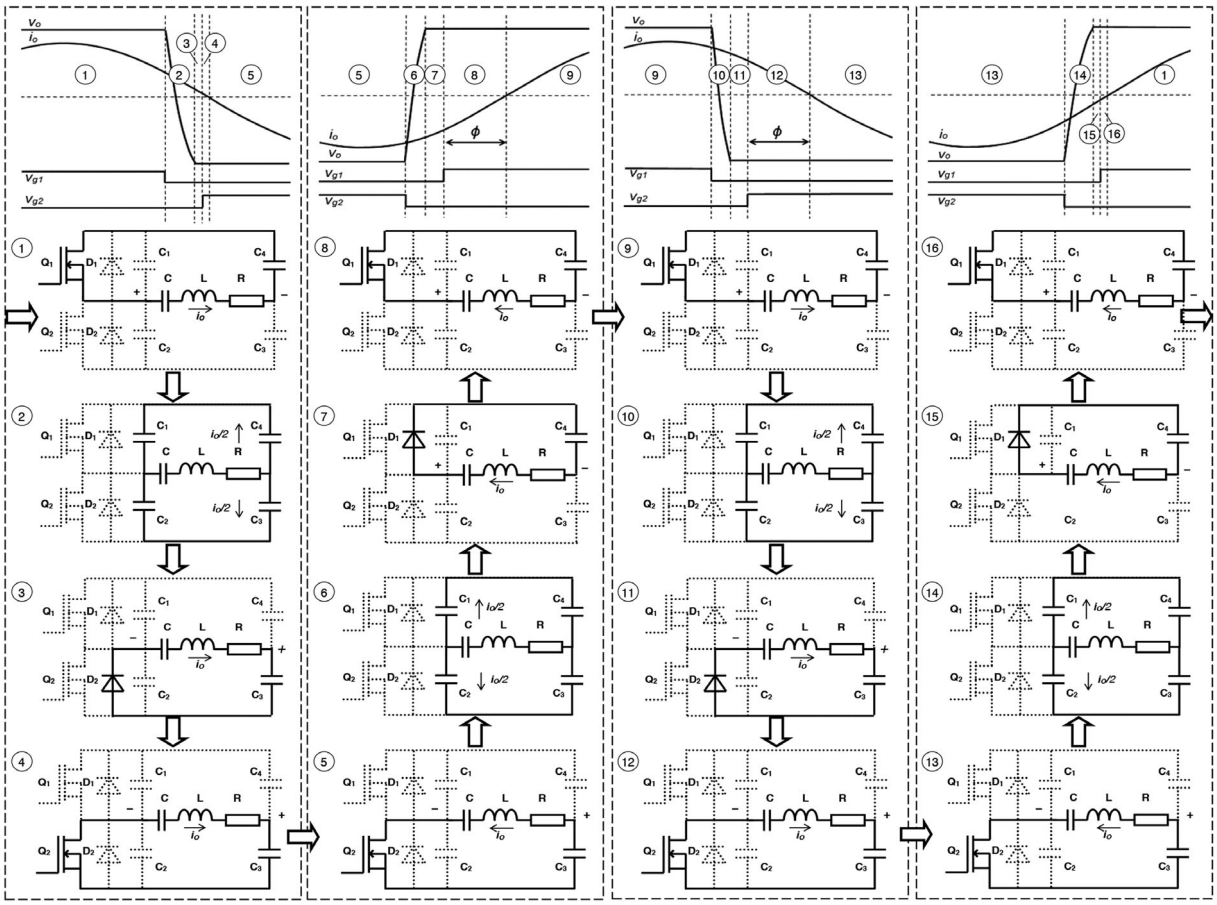

FIGURE 8 Complete switching sequence of the HB with EAPWM.

switching cycle of the standard APWM control. By doing so, the higher power losses can be alternately dissipated by Q_1 in one cycle, and by Q_2 in the next cycle.

Figure 8 shows the complete switching sequence of the enhanced asymmetrical pulse width modulation EAPWM applied to an HB inverter organized in four columns. The top of each column shows the simulated waveforms of the inverter output voltage v_o, the output current i_o and the two gate trigger signals of the transistors v_{g1} and v_{g2}. The switching sequence steps are identified by numbers, and the corresponding inverter schematics for each step are presented below. The current-carrying devices are drawn with solid lines, and the voltage-blocking devices are drawn with dotted lines. The direction of the current and the polarity of the voltage obtained at the end of each step have been expressed using arrows and $\pm$ signs.

The first full period of the oscillation corresponds to the first two columns on the left of Figure 8. Here the first switching process, in the time interval 2, is the turn-off of Q_1, which is carried out with a relatively small switching current determined by the phase β that ensures the ZVS condition. Next switching, in the time interval 6, is the turn-off of Q_2 which is done with a much larger switching current determined by phase ϕ. This is the normal situation with APWM modulation where the losses of Q_2 are greater than those of Q_1. The second oscillation period corresponds to the two columns on the right of the figure. Now, in the time interval 10, the turn-off of Q_1 is done with a large switching current determined by phase ϕ and, in the time interval 14, is the turn-off of Q_2, which is carried out with smaller switching current. If this switching scheme is repeated it is observed that using the EAPWM modulation the losses of the two transistors are equalized.

The control circuit designed to implement the EAPWM is a load-adaptive variable frequency system [21, 22] that must be able to perform ZVS under all operating conditions and to generate the switching sequence discussed above. Figure 9 shows the block diagram of the proposed control circuit. Since the phase detector and the VCO act like a phase-locked loop, the signal Q will be in phase with the inverter output current io. This square signal determines the rising slope of the trigger signal of the high side of the inverter near the zero crossing of the current. The block TD1 delays the Q signal to ensure the ZVS condition. The signal Vc inputs the EAPWM modulator to generate the rectangular signal that defines the phase ϕ that allows the power regulation. The dead time indicates the time interval between the turn-off and turn-on switching of the transistors. Dead time control circuit has two programmable delayers, TD2 and TD3, which generate the signal that references the turn-off switching of all transistors of the inverter taken into account for the calculation of (7).

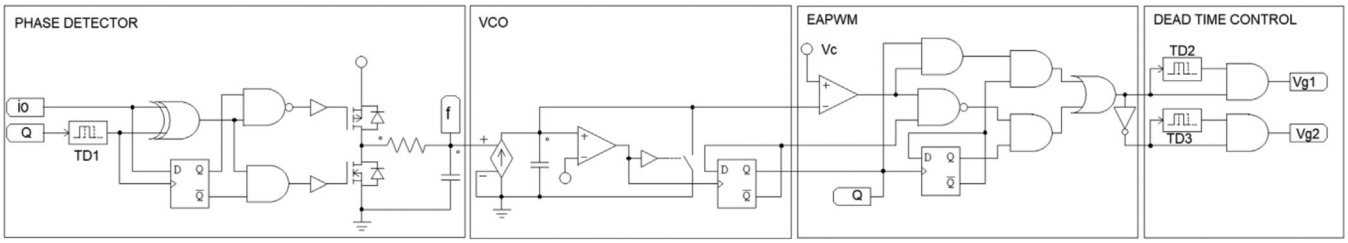

FIGURE 9 EAPWM block diagram.

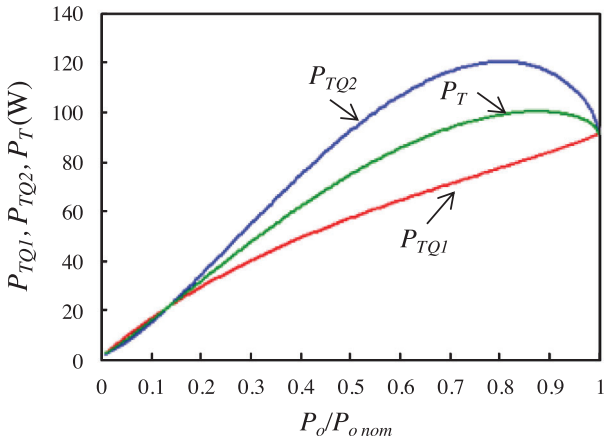

FIGURE 10 Power losses of the transistors of the high (red) and low side (blue) of the classic APWM HB. Green curve represents the power losses of any transistor if the EAPWM is used. Horizontal axis represents the normalized output power.

7 | COMPARATIVE STUDY

This section shows the significant impact of the results obtained with the EAPWM HB inverter in the reliability of the system compared with those obtained with the standard APWM control. Figure 10 illustrates the power losses of the transistors of the high and low sides of the HB.

The blue and red traces represent the power losses of the MOSFET transistor of the low and high sides respectively in a standard APWM HB inverter. The green trace indicates the losses of the transistor of any side of the EAPWM HB inverter.

In order to know the impact of these result on the reliability of the inverter, it is necessary to incorporate this data into the 'power cycling curve' of the SIC MOSFETs [23]. This curve provides information on the expected number of on–off cycles of the device in function of its junction temperature swing. The junction temperature can be calculated using the following expression.

$$\Delta T_J = P_T\,(R_{thJC} + R_{thCH} + R_{thHA}) \tag{24}$$

where P_T is the power loss of a transistor and different values of thermal resistances in the inverter are shown in Table 4.

Figure 11 shows, in left axis, the power cycling capability of each transistor of the standard APWM control (blues and red traces) and of the EAPWM (green trace) in the function of the normalized output power. The right axis represents the ratio of improvement n in reliability terms when the EAPWM control is used that is defined by

TABLE 4 Thermal resistances.

Magnitude	Sym.	*Value*	Unit
Thermal resistance junction to case	R_{thJC}	0.27	K/W
Thermal resistance case to heatsink	R_{thCH}	0.3	K/W
Thermal resistance heatsink to ambient	R_{thHA}	0.4	K/W

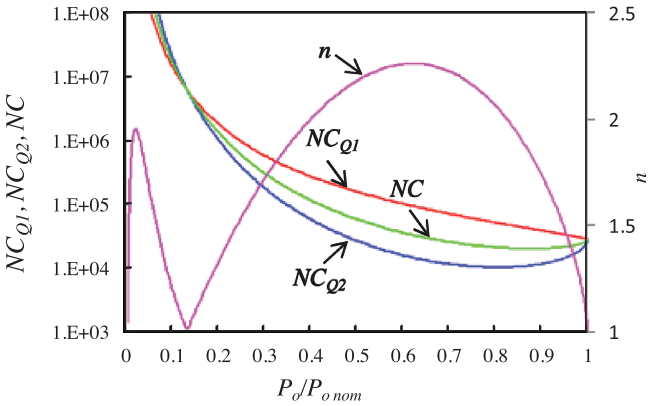

FIGURE 11 Expected power cycling capability of the standard APWM high-side transistor (red), low-side transistor inverter (blue) and any transistor of the EAPWM HB inverter (green). Pink curve represents the improvement ratio n. Horizontal axis represents the normalized output power.

$$n = \frac{NC}{\min(NC_{Q1}, NC_{Q2})} \tag{25}$$

If the output power is in the range from 40% to 80% of maximum power, the expected life of the EAPWM HB inverter is more than twice that of the standard APWM.

8 | EXPERIMENTAL RESULTS

This section shows the experimental results obtained from testing a 25-kW power prototype operating at a frequency of

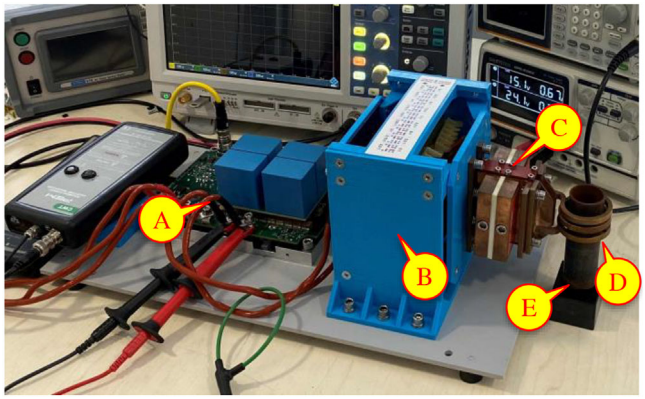

FIGURE 12 HB inverter test bed. Labels indicate items listed above.

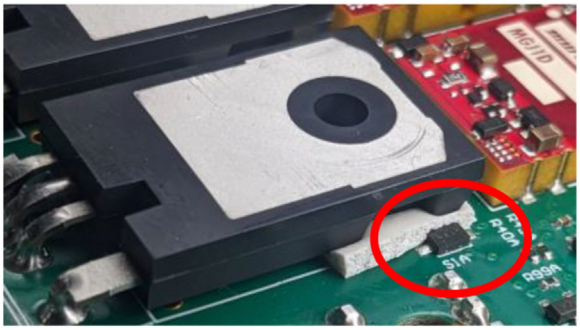

FIGURE 14 Detailed image of the bottom of the converter showing the transistor temperature sensor.

100 kHz. The inverter was powered by a 540-V DC voltage source. The values of the components of the resonant circuit are those obtained in previous sections. For the experimental verification, a test bed was constructed, consisting of the following elements:

A. A complete induction heating converter that contains a HB inverter with two C3M0016120K SiC MOSFETs and four film capacitors of 33 μF, an input three-phase rectifier and an integrated digital electronic control on an FPGA-based system mounted on a water cooling heatsink.
B. An output transformer with $n = 5{:}1$
C. Two high-power capacitors of 2.5 μF connected in series usable for induction the heating.
D. A solenoidal heating inductor of 2 μH.
E. A test load.

Figure 12 shows a picture of the test bed used to obtain the following experimental results.

Figure 13 shows digital storage oscilloscope (DSO) measurements of the main waveforms of the HB inverter with EAPWM control for 60% of nominal output power. The expected output voltage and current, power and frequency values have been obtained with sufficient accuracy despite the dispersion of the real values of the components used.

To check the correct temperature distribution of the transistors, measurements were made with a temperature sensor integrated into the bottom side of the PCB of the converter. Figure 14 shows a detailed picture of transistor temperature sensor. This sensor is thermally coupled to the transistor package via a thermal pad. A specific calibration allows calculating the temperature of the junction of the transistor.

Figure 15 shows the results of the measurements of the junction temperature T_{JQ1} of the transistor Q_1 and the junction temperature T_{JQ2} of the transistor Q_2 as a function of the

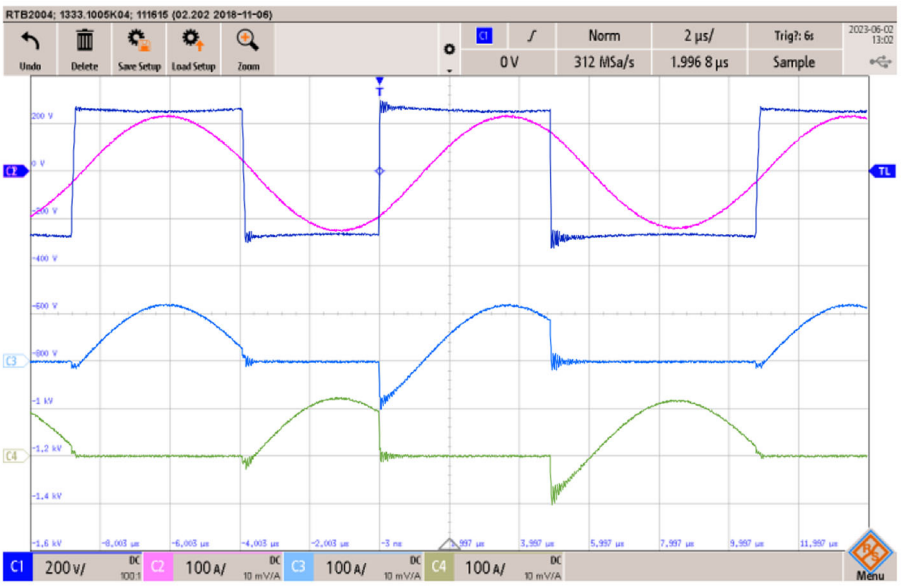

FIGURE 13 3 Experimental waveforms of the EAPWM HB inverter with a phase-shift of 55° (Po ≈ 15 kW). C1 (dark blue) is the output voltage (200 V/div), C2 (magenta) is the output current (100 A/div), C3 (light blue) is the current trough Q_1 (100 A/div) and C4 (green) is the current trough Q_2 (100 A/div). Time base is 2 μs/div.

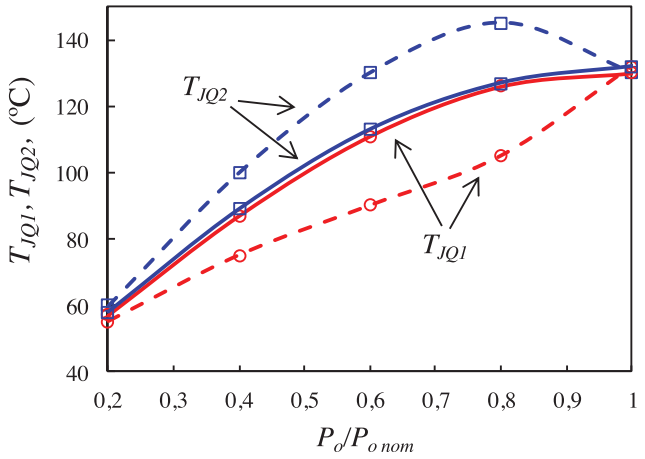

FIGURE 15 Experimental measurements of the junction temperature T_{JQ1} of the transistor Q_1 and the junction temperature T_{JQ2} of the transistor Q_2 as a function of the output power normalized to its maximum value.

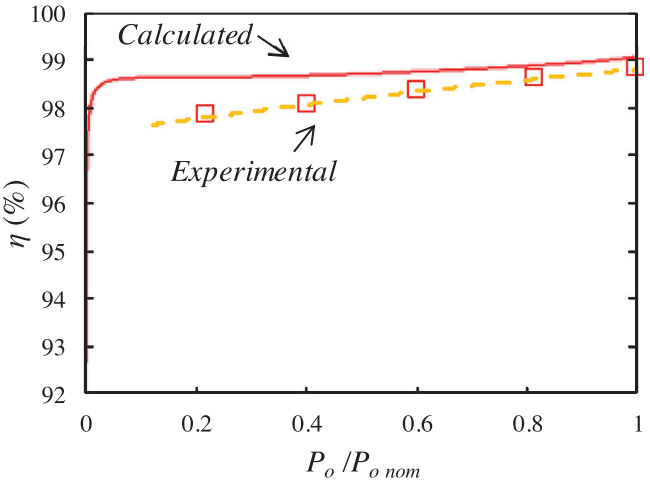

FIGURE 16 Calculated and experimental efficiency of EAPWM HB inverter in function of normalized output power. Dashed line and marking symbols represent the experimental measurements.

output power normalized to its maximum value. The experimental points are shown with a red circular symbol for transistor Q_1 and with a blue square symbol for transistor Q_2. A series of measurements have been made with the classic APWM modulation that corresponds to dashed lines, and another series of measurements with the EAPWM modulation that corresponds to solid lines.

It can be verified that the results obtained agree with those presented in Section 7. Before using the new modulation, the reliability of the system is limited by the high temperatures reached in the Q_2 junction. Using EAPWM, temperatures of the junctions of Q_1 and Q_2 are almost equalized and thus the power cycling capability of the converter is improved.

Figure 16 shows the experimental measurements of the efficiency which is bigger than 98% for nominal output power. Note that there are some differences between the experimental and calculated results that may be due to the modelling method used, the existence of losses of other elements not taken into account in the calculation (conductors, parasitic components, voltage and current sensors, etc.) and also to the measurement process.

9 | CONCLUSIONS

The purpose of this work was to develop a 25 kW, 100 kHz SiC MOSFET HB inverter with a modified switching sequence to improve its reliability in industrial applications, like induction heating, where a large number of cycles are required. A complete design procedure and power losses analysis have been presented, enabling the design of an HB resonant inverter for a given application. A comparative study allowed to determinate that the EAPWM HB inverter is a cost-effective solution that incorporates the following improvements:

- The output power is regulated by varying the phase-shift between switches that compose the HB.
- The control circuit was designed to perform ZVS condition.
- The swing of temperature of the SiC MOSFETs junctions was minimized by the use of this novel switching sequence of the transistors.
- The power cycling capability of the inverter was significantly improved in comparison with the standard APWM HB inverter.
- The lifetime of the inverter can be incremented for applications of a large number of cycles like induction hardening and others.

The viability of this design has been verified with the construction and test of a 25 kW, 100 kHz HB inverter using SiC MOSFET transistors in a high-frequency induction heating application.

AUTHOR CONTRIBUTIONS

Vicente Esteve: Conceptualization, Formal analysis, Methodology, Supervision, Writing—original draft, Writing—review & editing. José Jordán: Formal analysis, Validation. Enrique Dede: Conceptualization, Funding acquisition, Project administration. Juan Bellido: Software, Validation.

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CONFLICT OF INTEREST STATEMENT

The authors declare no conflict of interest.

DATA AVAILABILITY STATEMENT

Data sharing not applicable—no new data generated, or the article describes entirely theoretical research.

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