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Temperature-Dependent Dynamic on Resistance in Gamma-Irradiated AlGaN/GaN Power HEMTs

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Abstract: Dynamic R_{ON} is a key parameter in terms of device reliability and the efficiency of power-switching converters. In this study, commercial off-the-shelf GaN-on-Si power high-electron-mobility transistors (HEMTs) were irradiated using different regimes of accumulative gamma rays with a ^{60}Co source of photon energy (1.33 MeV), while a base temperature of 53 °C and 133 °C during the irradiation test was applied. This test campaign had the objective of investigating how the combination of gamma irradiation and temperature affects dynamic on-resistance (R_{ON}) behaviour. The results indicated that gate voltage bias stress affected the degradation of dynamic on-resistance when irradiation was applied, and that temperature was an accelerating factor in dynamic on-resistance degradation. Finally, we obtained a partial reduction in dynamic R_{ON} when a total ionising dose of around 140 krad(SiO_2) was applied and the base temperature during the irradiation test was not high.

Keywords: high-electron-mobility transistor (HEMT); gallium nitride (GaN); radiation hardness; assurance testing; radiation effects; total ionising dose (TID)

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1. Introduction

GaN high-electron-mobility transistors (HEMTs) are promising next-generation power devices that can be used in numerous applications [1–3]. In space applications, extreme environments due to radiation are among the main reasons for the reduced reliability of semiconductor components. When GaN HEMTs are used in space, they suffer from fluxes in high-energy protons and electrons during low Earth orbits, as well as neutrons and gamma rays in nuclear applications. Therefore, the effects of high-energy particle irradiation should be considered when HEMT devices are proposed for applications in these extreme environments [4,5]. The effects of total ionising dose (TID) radiation on AlGaN/GaN HEMTs have been studied in the past but have focused on theoretical studies, simulations, and the effects on experimentally static electrical characteristic metrics (e.g., transconductance, threshold gate voltage, leakage current) [6–11]. GaN devices have been demonstrated to be robust materials for the development of high-power radiation-hardened electronics for satellites and space probes, as well as to support electronics in high-energy and nuclear experiments. Many radiation tests have been performed to determine the reliability of GaN HEMTs under different radiation conditions, and they have always shown high stability and inappreciable DC parameter drifts for total ionising doses around 2 Mrad.

However, the measurement of GaN HEMT sensitivity to radiation depends on the biased conditions during the radiation tests. Usually, the components are biased at room temperature in DCs at low power dissipation or they are short-circuited. These testing conditions are valid most of the time, but our objective was to analyse the sensitivity of GaN technology when radiation tests were performed under real operating conditions (high power and temperature). Additionally, the failure mechanisms of compound semiconductor

devices have frequently shown high values of activation energy at higher temperatures; therefore, the combined effects of temperature and radiation were the focus of this study.

In particular, the use of GaN transistors could represent a potential breakthrough for aerospace applications as it would allow the switching frequency to be increased from 100 kHz to more than 1 MHz using devices that are capable of blocking high voltages (>600 V) with very low channel resistance. This would represent a very considerable reduction in the size and weight of converters in power sector satellites since the size of the converter coils and their capacitors would be reduced, as well as the cooling system because they would be able to work in higher junction temperatures than their silicon transistor counterparts.

However, some commercial off-the-shelf GaN HEMTs still have problems with completely removing charge trapping effects, which implies the presence of higher on-state resistance during switched power converter operation and may also result in the instability of positive or negative threshold voltages. The existence of dynamic R_{ON} is a critical issue among GaN-based HEMTs in terms of the reliability of achieving high power densities in future aerospace power electronic converters.

In this paper, we define the test campaign that we carried out in which types of commercial p-GaN HEMTs were irradiated with ^{60}Co gamma rays under different bias and temperature conditions. This campaign had the purpose of simulating the real thermal and radiation conditions that occur simultaneously during low Earth orbit (LEO) satellite missions.

Finally, the experimental results that were obtained and the conclusions that were reached are presented. The objective of this study was to establish whether gamma irradiation could affect switching and conduction losses due to changes in dynamic resistance (R_{DSON}) as a function of device temperature during irradiation tests. In terms of reliability and DC–DC converter design, the transient behaviour of R_{DSON} during switching could reduce the future application of GaN HEMTs as power switches in space applications.

2. Materials and Methods

The analysis was carried out using commercial 650 V Schottky-type p-GaN gate AlGaN/GaN power transistors (part reference: GS-065-011-1-L [12]). In total, 12 devices were used and different bias conditions and base temperatures were applied during the irradiation tests. The goal was to evaluate the influence of the combination of gamma irradiation, stress voltage and temperature on dynamic on-resistance (R_{ON}). In addition, two samples were selected as references (control devices) to confirm the proper operation of the measurement system, i.e., unirradiated devices that were only subjected to electrical measurements after each step of irradiation, without any bias or radiation conditions being applied. Table 1 shows the test conditions that were applied during the irradiation tests.

Table 1. Bias conditions that were applied during the irradiation tests.

Condition	Sample Serial Number	Temperature	Units	Radiation	Gate Bias [1]	Drain Bias [1]
Control	A10, A11	Room Temp.	2	No	N/A	N/A
Drain Bias	G8–G10	53 °C	3	Yes	0 V	500 V
Drain Bias	G3–G4	133 °C	2	Yes	0 V	500 V
Drain–Gate Bias	G5–G7	53 °C	3	Yes	−5 V	500 V
Drain–Gate Bias	G1–G2	133 °C	2	Yes	−5 V	500 V

[1] Bias conditions during irradiation exposure: N/A: not applicable to unirradiated control samples.

The test campaign was carried out in the CNA's RADLAB facility at the National Accelerator Centre in Seville, Spain. The gamma irradiation contained a ^{60}Co gamma source with associated photon energies of 1.17 and 1.33 MeV (mean value = 1.25 MeV). The selected dose rate was 2.8 krad(Si)/h, which was within the "standard rate" window (0.36–180 krad(Si)/h) of the European Space Agency, according to the TID Test Method [13],

and achieved a total dose of 374 krad(Si). The dose rate was obtained by measuring the charge in two TM30013 ionisation chambers (PTW-FREIBURG, Freiburg im Breisgau, Germany) and one MultiDOS multichannel electrometer (PTW-FREIBURG, Freiburg im Breisgau, Germany) and considering the environmental correction factor. The dose rate uniformity in the filter box was 98.5%. The devices under test (DUTs) were mounted on a printed circuit board, which was placed into a sample holder inside the thermal vacuum radiation chamber. This chamber was described in [14] and was composed of a structure that supported a vacuum chamber, in which the sample holder was connected to a temperature-controlled external system. Figure 1 shows the devices that were inside the chamber.

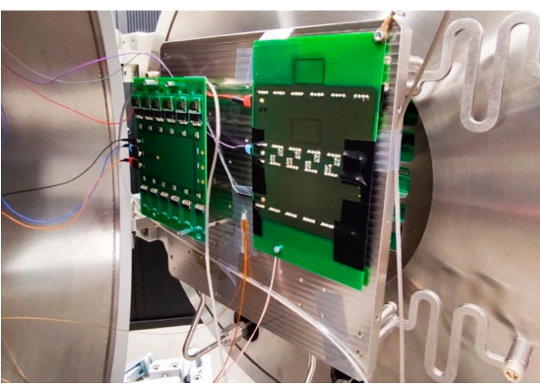

Figure 1. The sample holder inside the thermal vacuum radiation chamber, which was developed at the National Accelerator Centre (CAN) in Spain.

Overall, five irradiation steps were carried out during the test campaign. During the pristine stage and after each irradiation step, all devices were measured using a Keysight B1505A semiconductor device power analyser to obtain the electrical characteristic metrics. The V-I characteristics were measured at 25 °C after irradiation for 30 min.

Figure 2 shows a block diagram of the test procedure. The static electrical measurements (transfer (Ids-Vgs), gate Schottky diode (Ig-Vgs), drain to source leakage current (Idss-Vds), and gate leakage current (Igss-Vds)) were performed after each exposure step for all devices, including the control devices.

At the end of the total irradiation, two annealing steps were implemented. The first annealing step consisted of room temperature annealing under bias conditions for 24 h. Afterwards, accelerated ageing was carried out, in which the devices were baked at 100 ± 5 °C under bias conditions for 168 h. In both annealing steps, the bias voltage that was applied to each DUT was the same as that applied during the irradiation steps.

During irradiation, the devices were biased under two different conditions with two different controlled temperatures: (1) OFF with voltage stress in the drain and the gate (Vds = 500 V and Vgs = −5 V); (2) OFF with voltage stress in drain (Vds = 500 V and Vgs = 0 V). The devices that were irradiated under these two different bias conditions were also subjected to two different temperatures: half of the devices were irradiated at 53 °C and the other half of the devices were irradiated at 133 °C.

Concerning the measurements, two types were performed: the I–V measurements were conducted using a power device analyser (B1505A) and the R_{ON} measurements were conducted using a custom double pulse circuit (Figure 3) [15]. The implemented switching circuit had the benefit of being able to fully control the time that the voltage stress was applied to the GaN HEMT. Basically, it consisted of two transistors that were connected in series between the drain and the source with a resistive load in between.

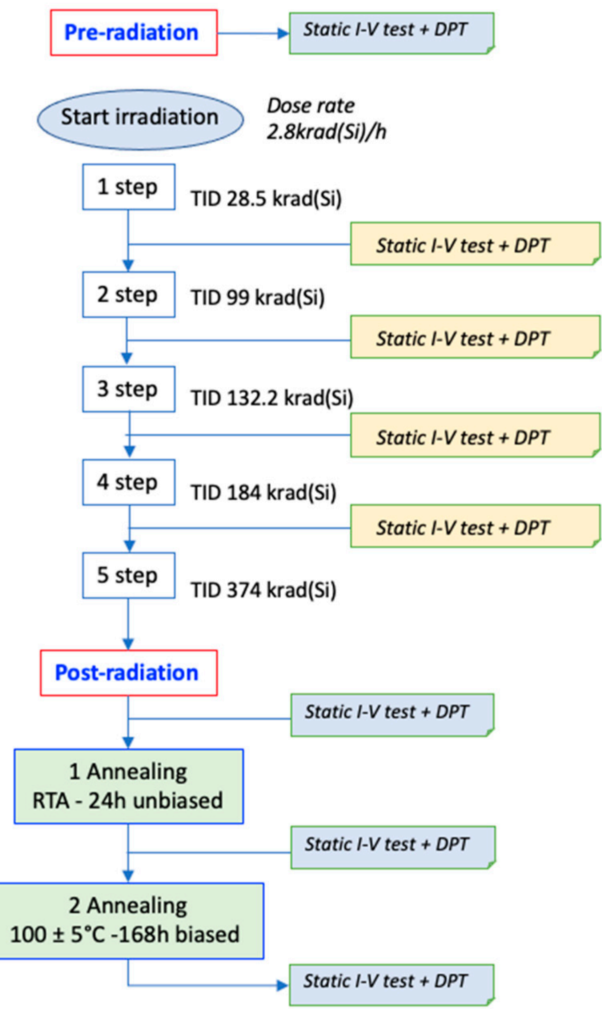

Figure 2. A schematic diagram of the experimental procedure of the gamma test campaign.

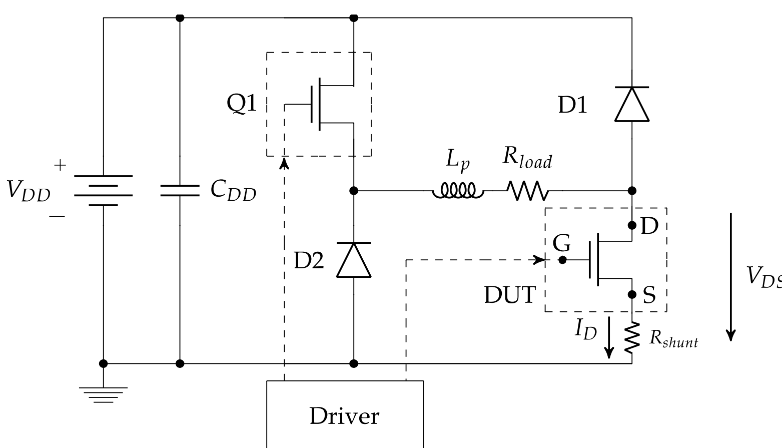

Figure 3. The circuit diagram that was used to measure the dynamic R_{ON}.

Transistor Q1 was used to control the stress/trapping time. A resistive load (R_{load}) was used to set the current level when the DUT was in the on state. Due to the inherent parasitic inductance (L_p) of the power R_{load}, two SiC diodes (D1 and D2) offered a freewheeling path for the current when either Q1 or the DUT was switched from on to off. The test sequence of the double pulse measurement is shown in Figure 4. This sequence consisted of stressing the device with a drain voltage for 60 s while it was in the off state and then switching the

device to the on state for two pulses of 200 µs, which were separated by an off state of 20 µs. These consecutive pulses that followed the voltage stress provided information about the main trappings, which were the trappings that were induced by the voltage stress and hot electron effects during the switching events [16,17]. For all tests, the drain voltage stress was 500 V, which represented a derating of 80% as it was fixed [18].

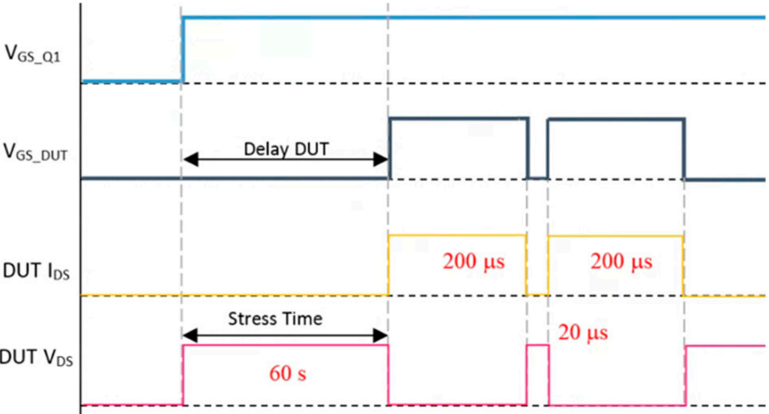

Figure 4. The gate voltage sequence for the double pulse tests.

For the electrical measurements, we used a 98 mΩ shunt resistor (SDN-414-10) to measure the current and a passive voltage probe (300 V and 500 MHz PP018, Teledyne-Lecroy, CA, USA) to measure the voltage. Owing to the high voltage that was applied to the DUTs, the voltage across the devices had a large dynamic range that could overload the oscilloscope input amplifier, so the on-state voltage could not be determined accurately. To avoid this problem, a voltage clamp circuit was used together with the passive voltage probe. A commercial voltage clamp (clp1500V15A1, Springburo GmbH, Emmendingen, Germany) was used. A low range (2 V) was selected in the voltage clipper to obtain a fast response of 100 ns, which was affected by the passive voltage probe and the voltage clipper. Precise frequency response compensation was applied to the passive voltage probe to compensate for the whole measurement chain of the clipper and voltage probe.

3. Results and Discussion

The effects of gamma radiation on voltage and temperature stress conditions were different. In this section, we analyse the changes in the static and dynamic characteristics by considering the combinations of stress bias conditions and base temperatures that were applied.

3.1. Irradiation at a High Temperature (133 °C)

The devices that were irradiated at 133 °C, regardless of the stress bias voltage conditions, suffered from degradation due to the monotonous increase in drain leakage current (Id), which mostly originated from the increase in gate leakage current (Ig) while the source and substrate currents only offered minor contributions when the total dose was progressively increased. Figure 5 presents the drain leakage current that was measured at 25 °C after each step of irradiation for 30 min using a B1505A semiconductor power parameter analyser. We observed a fourfold increase in the gate current of the G3 device and a sevenfold increase in that of the G4 device, both of which were measured at 600 V.

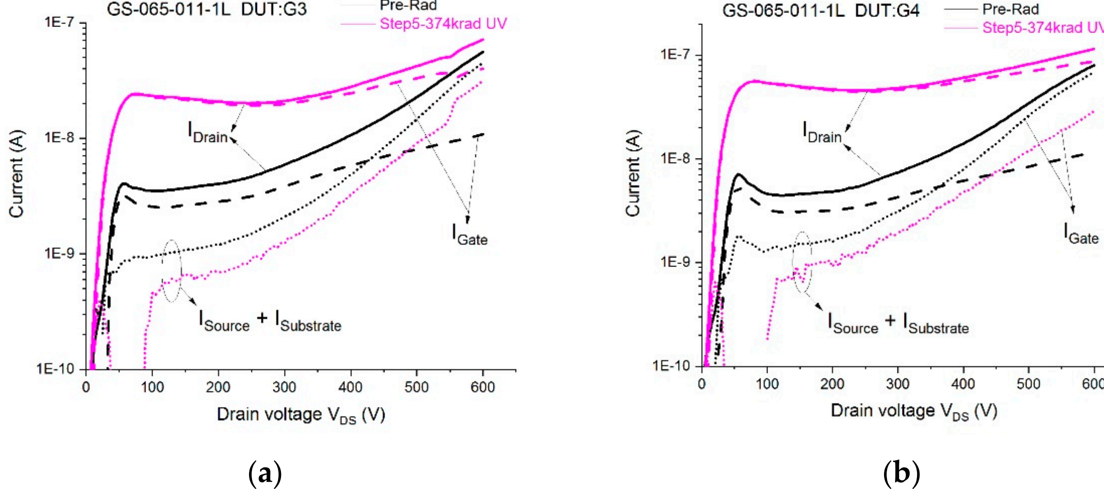

Figure 5. The leakage currents versus drain voltages in the off state (V_{GS} = 0 V) before (black lines) and after (magenta lines) gamma radiation with a total ionising dose of 374 krad(SiO_2) which were stressed during irradiation with V_{DS} = 500 V and V_{GS} = 0 at a base temperature of 133 °C. (**a**) Device G3 (**b**) Device G4.

With higher temperatures, the trapping process became faster and the time constants decreased. Additionally, in the off-state condition, when a high drain bias was applied to the device, the drain leakage increased and was favoured by the injection of electrons from the substrate into the GaN layer, which was also strongly dependent on the temperature [19,20].

Figure 6 shows a schematic representation of the trapping processes for two different bias conditions that were used. In the figure, we present the two drain leakage paths that appeared during the GaN HEMT reverse condition tests. In the off state, the trapping processes could occur both at the gate–drain surface (due to the high electric fields between the gate and the drain terminal) and the buffer (due to the large vertical field under the drain).

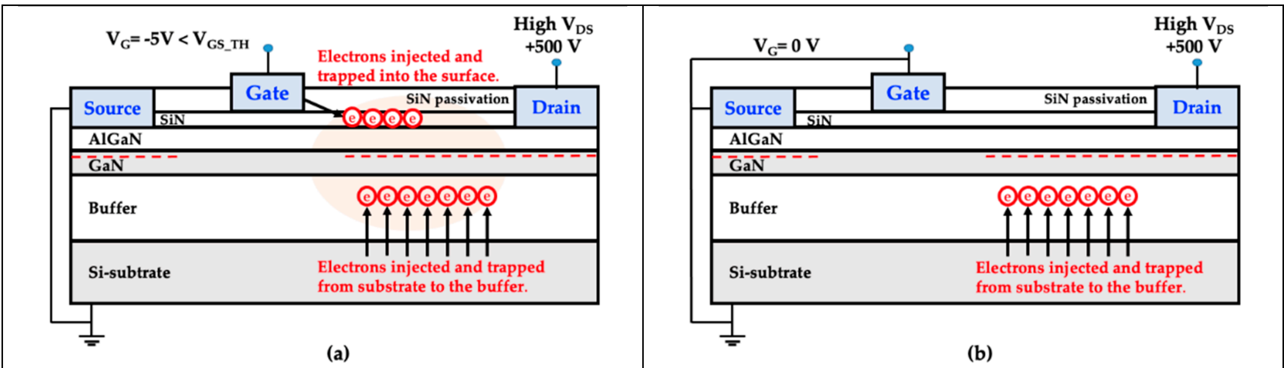

Figure 6. A schematic representation of the trapping processes in the analysed GaN HEMTs during the two off-state stresses. (**a**) Whit negative gate voltage. (**b**) Whit zero gate voltage.

The drain–source current path was established across the silicon substrate and the silicon/nucleation layer interface due to inefficient isolation between the GaN buffer and the Si substrate. It has been reported [21] that the reverse drain leakage of GaN-on-Si HEMTs is due to the injection of electrons into the GaN buffer layer and the tunnelling leakage current of the Schottky gate reverse bias. Therefore, the accumulation of negative charge in the buffer, which is favoured by the positive drain voltage, originates from the increase in dynamic on-resistance (R_{ON}). This vertical leakage that fills the buffer traps is interrelated between the trapping rate and the vertical drain–substrate current [22].

During the process of reverse gate bias, the AlGaN/GaN interface trap captured electrons in the channel and caused a negative shift of the threshold voltage. Additionally, the Schottky contact of the gate electrode began to irreversibly degenerate under both the high temperature that was applied during radiation and the high electric field that decreased the height of the Schottky barrier.

Considering the voltage stress that was applied during radiation, it was also observed that when a negative voltage (Vgs = −5 V) was applied to the gate together with a positive drain voltage (sample G2), the increase in the leakage gate current was lower (or even decreased) compared to samples that only had voltage stress in the drain and gates that were shorted to the source terminals (sample G4). Negative gate-to-source voltages induced lateral trappings due to the injection of electrons at the gate–drain surface. This injection of electrons could help to reduce the number of holes that were created by the gamma irradiation and, therefore, helped to reduce the increases in gate leakage current (Figure 7).

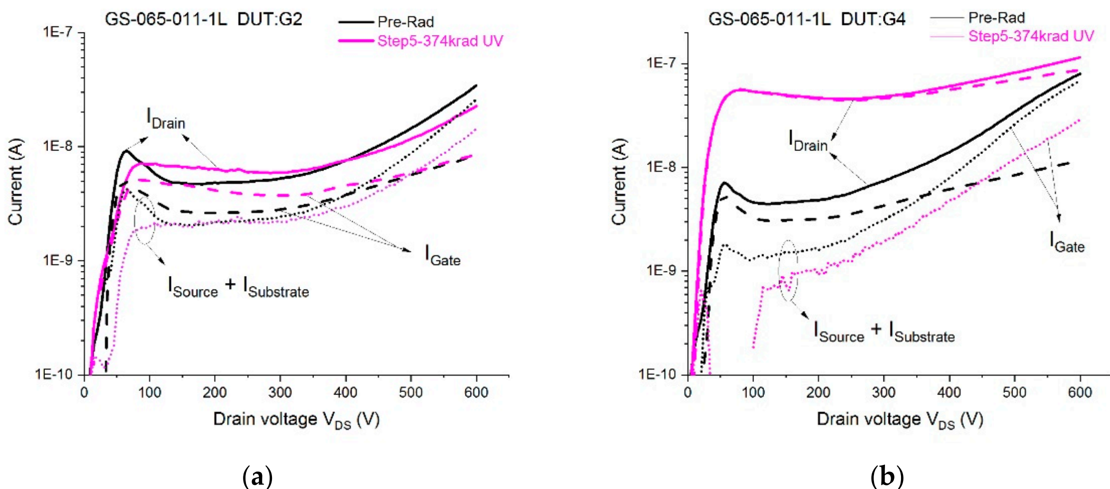

Figure 7. The leakage currents versus drain voltages in the off state (V_{GS} = 0 V) before (black lines) and after (magenta lines) gamma radiation with a total ionising dose of 374 krad(SiO_2) at a base temperature of 133 °C. (**a**) Device G2 stressed during irradiation with V_{DS} = 500 V and V_{GS} = −5 V. (**b**) Device G4 stressed during irradiation with V_{DS} = 500 V and V_{GS} = 0.

The dynamic on-resistance is a parameter that is dependent on the trapping or detrapping rate. Thus, we needed to consider the influence of gamma radiation on the trapping processes to establish the relationships between the obtained results and the dynamic on-resistance. The effects of irradiation depend on the structures, temperatures, pre-existing trap densities, dose rates, total accumulated doses, and experimental bias conditions that are applied during irradiation. The improvement or degradation of the electrical characteristics (e.g., gm, I_D, R_{ON}, Vth) have been discussed in the literature [23–25].

When gamma rays are focused on matter, a process of matter ionisation occurs, primarily via indirect ionisation. Electrons interact and may become absorbed, scatter, or produce electron–positron pairs, depending on their energy. Overall, low doses of accumulated radiation result in improvements and when higher doses are applied, degradation begins. In our case, the rate that was achieved was not very high (374 krad) and we distinguished between improvement or degradation depending on the temperature that was applied during the irradiation tests.

In any case, the effects of gamma radiation together with the higher temperature created an increase in the gate leakage current and a shift in the threshold voltage to the left, which caused the degradation of the HEMT and an increase in the dynamic on-resistance, as we explain later.

3.2. Irradiation at a Low Temperature (53 °C)

In the case of irradiation with a lower temperature, regardless of the applied voltage stress, a decrease in the drain current was observed, which was mainly caused by a reduction in the source–substrate current of around 60%. There was no increase in the gate leakage current; however, differences were observed depending on whether the DUT was stressed with V_{DS} = 500 V and V_{GS} = −5 V or V_{DS} = 500 V and V_{GS} = 0. The devices that were stressed during irradiation with V_{DS} = 500 V and V_{GS} = −5 V (G6 and G7) showed a higher reduction (60%) in the drain leakage current than the devices (G8 and G10) that were only stressed with V_{DS} = 500 V (45%). With a negative gate voltage, there was an indicative reduction in the gate leakage current that was additional to the reduction in the source–substrate leakage current, which was due to the compensation of the hole traps by the existence of additional electron traps under the gate that were induced by the negative gate bias during irradiation (Figure 8).

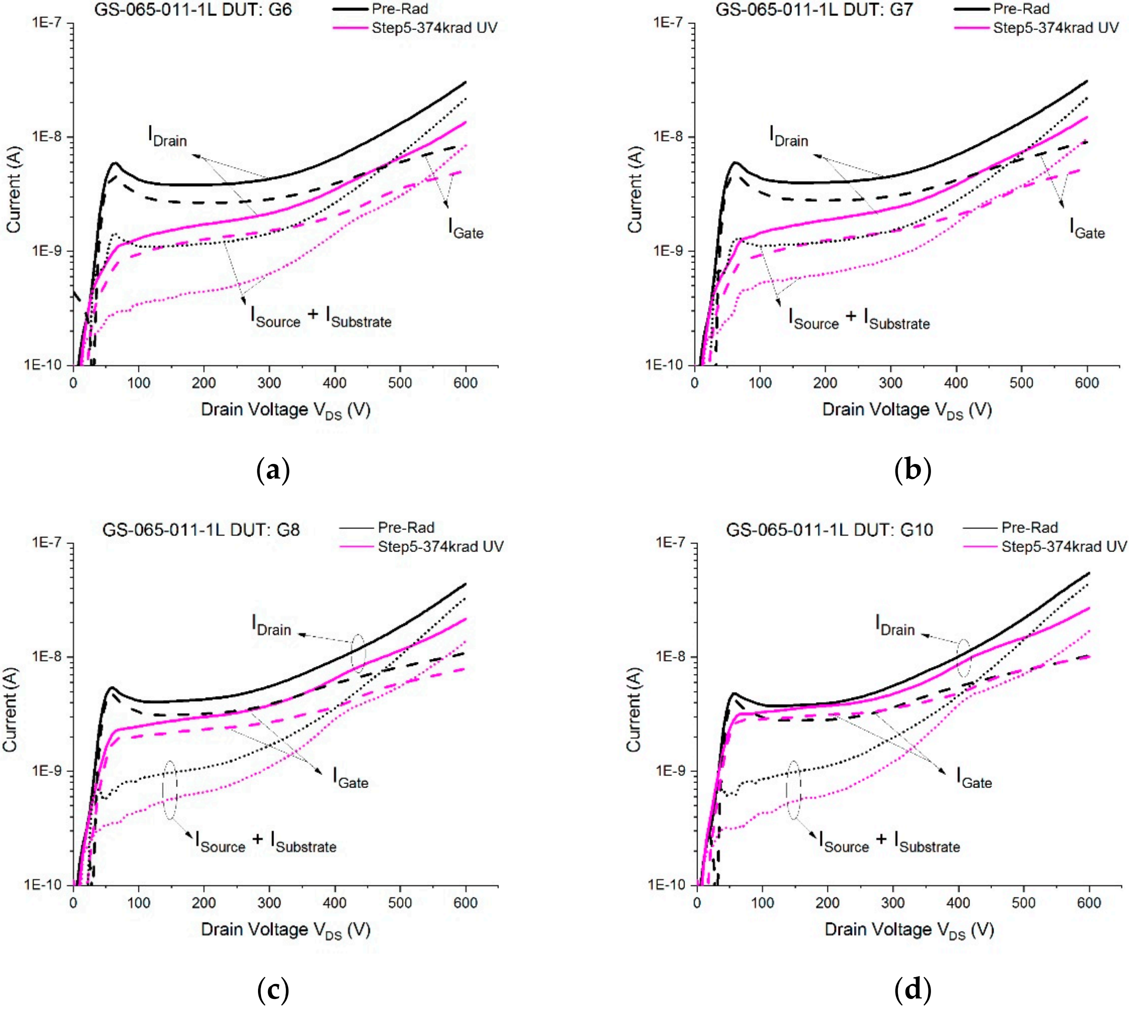

Figure 8. The leakage currents versus drain voltages in the off state (V_{GS} = 0 V) before (black lines) and after (magenta lines) gamma radiation with a total ionising dose of 374 krad(SiO_2) at a base temperature of 53 °C. (**a**) Device G6 stressed during irradiation with V_{DS} = 500 V and V_{GS} = −5 V. (**b**) Device G7 stressed during irradiation with V_{DS} = 500 V and V_{GS} = −5 V. (**c**) Device G8 stressed during irradiation with V_{DS} = 500 V and V_{GS} = 0. (**d**) Device G10 stressed during irradiation with V_{DS} = 500 V and V_{GS} = 0.

In off-state conditions, trapping could occur both at the gate–drain surface and the buffer. The increase in R_{ON} mainly originated from buffer traps. This process could be explained by two different mechanisms: an electrostatic effect of the high negative

gate–drain voltage that depleted the hole traps in the buffer and the flow of vertical drain current.

Our results, in concordance with previous investigations [25], showed an improvement in the electrical properties of the devices due to the decrease in leakage current when gamma irradiation was applied. This reduction could be attributed to the reduction in the density of traps, along with the ordering of native defects, but it needs to be verified by scanning transmission electron microscopy (STEM) to characterise the defects and elemental distributions. The reduction in the drain–substrate leakage helped to reduce on-state trapping in the device and, therefore, the dynamic R_{ON}.

3.3. Dynamic R_{ON}

The results of the dynamic on-resistance tests are shown in Figure 9. After a stress of V_{DS} = 500 V was applied to the GaN HEMTs in the off state, two pulses were applied (Figure 4) using a double pulse test (DPT) circuit to measure the dynamic on-resistance.

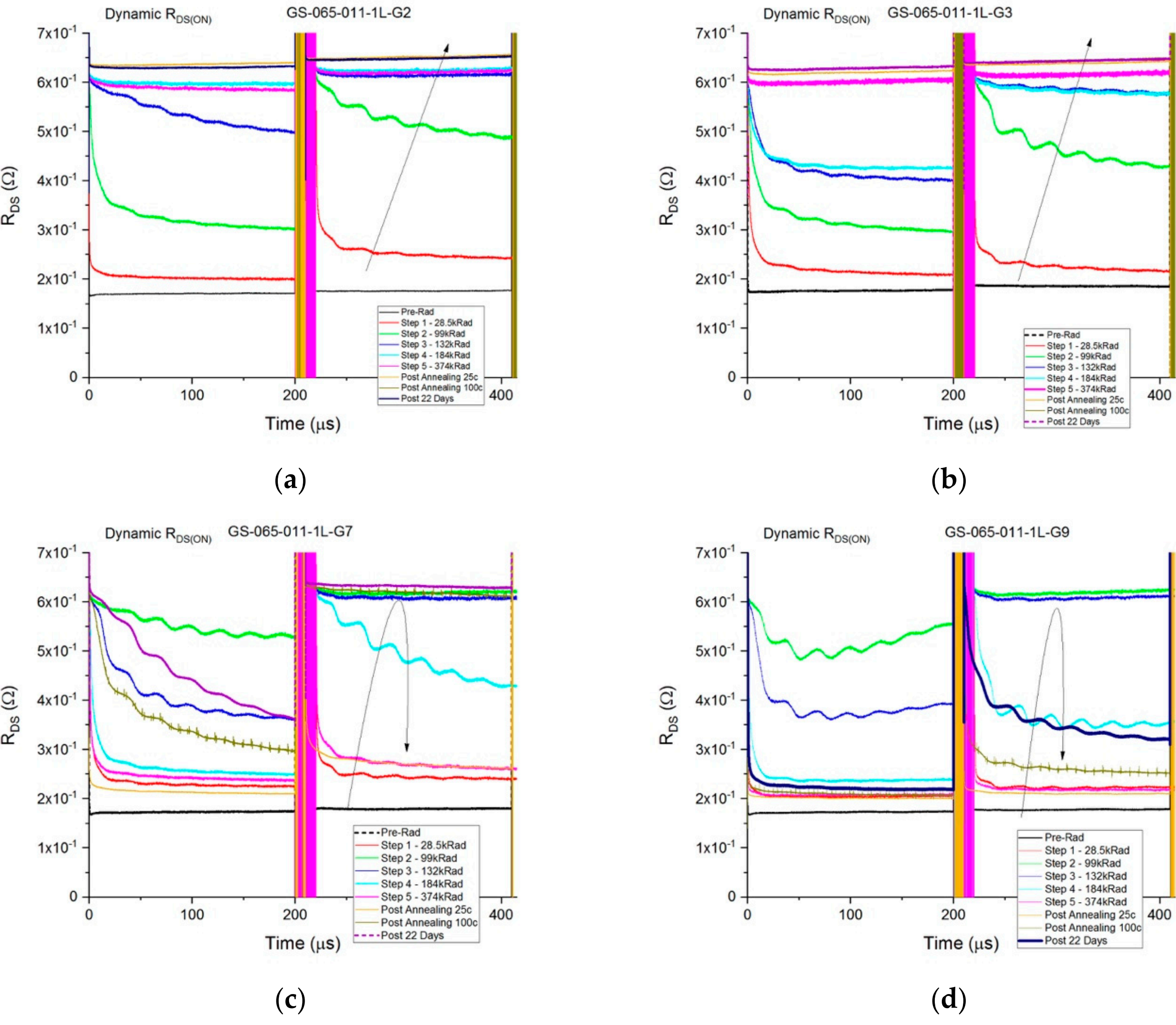

Figure 9. The dynamic R_{ON} double pulse measurements in the off state (V_{DS} = 500 V and V_{GS} = −5 V) and on state (V_{GS} = 3 V and I_{DS} = 2.5 A): (**a**) device G2, which was subjected to drain and gate voltage stress during irradiation at 133 °C; (**b**) device G3, which was subjected to drain voltage stress during irradiation at 133 °C; (**c**) device G7, which was subjected to drain and gate voltage stress during irradiation at 53 °C; (**d**) device G9, which was subjected to drain voltage stress during irradiation at 53 °C.

In all of the devices that were subjected to gamma radiation at the higher temperature (133 °C), regardless of the voltage stress that was applied (Table 1), a degradation of the dynamic R_{ON} was observed, which increased with the total ionising dose and was not recoverable after the two-step annealing process (Figure 9a,b). For the devices that were irradiated at the lower temperature (53 °C), the dynamic on-resistance increased with the accumulated dose until it reached step 4 (184 krad(SiO_2)) when the R_{ON} started to reduce in value and it only increased after the 100 °C annealing process, which was permanent (Figure 9c,d).

In Figure 9, increases in dynamic R_{ON} can be observed that were higher in the second pulse than in the first. This was evidence of a trapping process, which was induced by hot electrons during the semi-on state of the switching events. Under hard-switching conditions, the GaN HEMTs were simultaneously subjected to high drain voltages and a rising drain current. The electrons that were injected from the source to the drain were accelerated by the high electric field (usually called "hot electrons").

In order to quantify the evolution of dynamic R_{ON} during the irradiation process, we measured the average value of R_{ON} during an interval of 20 µs at the end of the second pulse. Figure 10 shows the evolution of the dynamic R_{ON} values for all of the devices during all of the radiation steps throughout the test campaign.

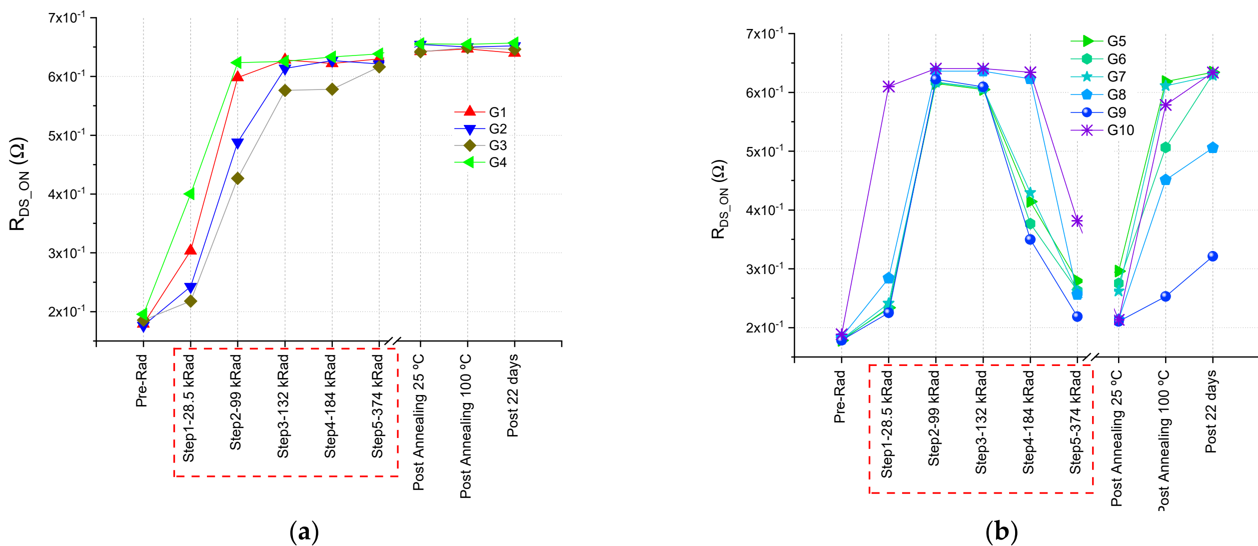

Figure 10. The R_{ON} double pulse measurements: (**a**) devices G1–G4, which were irradiated at 133 °C; (**b**) devices G5–G10, which were irradiated at 53 °C.

All of the devices that were irradiated at 133 °C suffered from an increase in R_{ON} that reached saturation at 99 krad(SiO_2) or 132 krad(SiO_2), which was indicative of the saturation of the electric charge traps in the devices that, in turn, limited the total ionising dose (TID) effects. However, in the devices that were irradiated at the lower temperature (53 °C), the resistance increased with the total accumulated dose and become saturated close to 99 krad(SiO_2) and began to decrease in the range of 132–184 krad(SiO_2). Finally, in the annealing step at 100 °C, a permanent degradation was observed.

It was also mandatory to investigate the behaviour of dynamic R_{ON} when multiple pulses were applied. The multi-pulse test (MPT) was conducted using the circuit setup that was shown in Figure 3, but with a driving signal test sequence of multiple pulses, a stress time of 500 ms, and an on-time of 6 us. The multi-pulse sequence finished once the stationary value of R_{ON} was found, using a mathematical function in the digital oscilloscope that was used to record the drain current and drain voltage waveforms [15]. The results are shown in Figures 11 and 12.

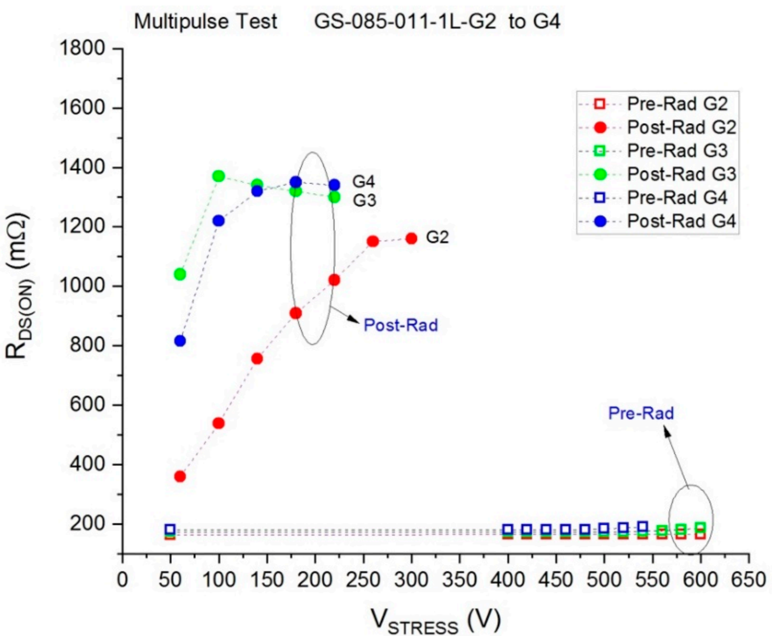

Figure 11. The results of the multi-pulse test for the R_{ON} values of devices G2–G4, which were irradiated at 133 °C.

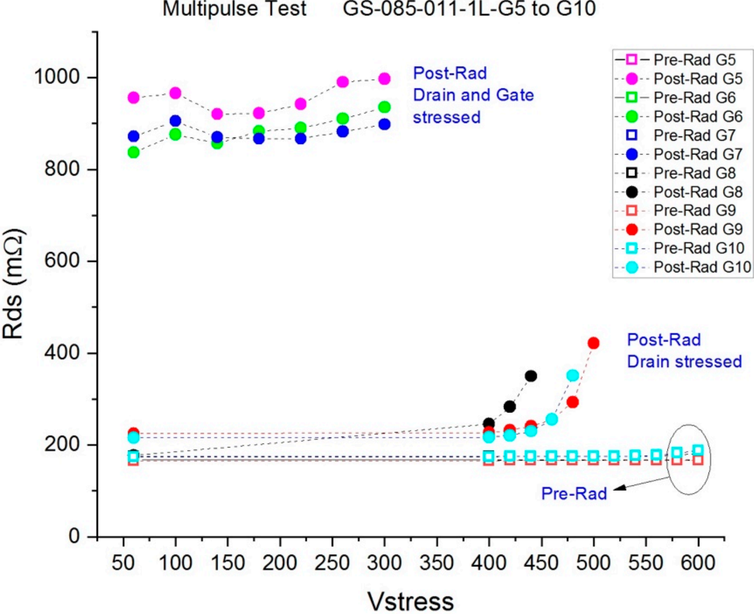

Figure 12. The results of the multi-pulse test for the R_{ON} values of devices G5–G10, which were irradiated at 53 °C.

Figure 11 confirms the irreversible increase in R_{ON} when the temperature during irradiation was 133 °C, regardless of the stress that was applied to the drain and/or gate.

Similarly, Figure 12 shows the influence of the negative voltage stress that was applied to the gate during irradiation. Despite being irradiated at a lower temperature (53 °C), the devices with stress at the drain and gate (V_{DS} = 500 V and V_{GS} = −5 V) demonstrated degradations in dynamic R_{ON} once the radiation accumulated. The R_{ON} value was five times higher, regardless of the applied stress voltage. It could be seen that, for V_{DS} = 500 V in the off state, the R_{ON} reached its maximum value and did not change when a higher stress voltage was applied.

In the devices to which voltage stress was applied to the drain and in which the gate was short-circuited with the source, the R_{ON} remained practically constant between 50 and 400 V of applied stress, and it started to increase almost exponentially from 500 V.

4. Conclusions

In this work, we investigated the impacts of gamma radiation on commercial off-the-shelf Schottky-type p-gate AlGaN/GaN HEMTs by considering temperature and voltage bias stress as influence variables. The acceleration of the trapping kinetics (due to the higher temperature) and the injection of electrons from the substrate into the trap sites (due to the high off-state voltage stress) caused an increase in R_{ON} that could seriously undermine the device's performance.

This trapping rate was higher than the accumulation rate of positive charges (holes or ionised donors). These positive charges, which resulted from electron–hole pairs that were created by radiation-induced ionisation, had lower mobilities at higher temperatures and, thus, did not allow the holes to migrate or recombine, thereby reducing the radiation impacts.

However, at lower temperatures, the trapping effects were less and as the rate of accumulated radiation increased, there was a partial recovery in dynamic R_{ON} that could be attributed to dispersion effects from the buffer traps, according to different explanations from the literature: trapped holes in C-related traps partially neutralise negative ionised acceptors [26]; the neutralisation of negative and positive buffer charge storage [27], which is induced by leakage paths between 2D electron gas (2DEG) and C-doped buffer; the generation of positive charges via the ionisation of donor traps in the unintentionally doped (UID) GaN channel layer [28].

From the point of view of the design of power converters for space applications, where silicon MOSFET technology is to be replaced by GaN HEMTs, reliability is an essential requirement due to the harsh environments. The multi-pulse test confirmed that R_{ON} could permanently degrade five times faster (for an accumulated dose of 374 krad(SiO_2)), depending on the temperature and the voltage stress that was applied during the off interval. The most favourable conditions were when the temperature of the device during irradiation was in the order of 60 °C (in accordance with the standard base temperature of power stages in satellites) and negative voltage stress was not applied to the gate of the device and the only stress was the voltage in the drain and the semi-on conditions during the switching operation. In that case, the degradation was lower and did not appear until a voltage stress of around 450 V was applied.

The impact of gamma radiation on the $R_{DS(ON)}$ performance of the device is an important issue due to an increase in this value will have a very significant impact on the power converter losses, especially in hard-switching mode, where the overlap between voltage and current favours the trapping effect. In addition, this increase in power losses will cause an increase in temperature and the effects of charge trapping can be favoured by this increase in temperature. This effect and temperature dependency lead to a difficult thermal design of the converter. Additionally, the increase in temperature can degrade the forward Schottky characteristic of the gate resulting in a positive shift of the gate to the source voltage threshold, affecting the driving requirements of the driver circuit.

Therefore, it would be necessary to control the temperature of GaN HEMTs in radiation environments in addition to the drain–source blocking voltage so that they can withstand the conditions during the off intervals and the passivation phases of satellites.

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