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Thermal Analysis of the Solar Orbiter PHI Electronics Unit

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***Abstract*—This work presents the thermal design of the electronics unit of the instrument PHI, onboard the ESA mission Solar Orbiter. The thermal design procedure, along with the problems encountered during this design phase, and the solutions found to fix them are described, proving in this way the thermal feasibility and robustness of the unit. Its final thermal behaviour, obtained from thermal analyses correlated with data from thermal tests performed in a vacuum environment, is presented.**

***Index Terms*—Thermal management of space electronics, Space thermal control, Testing, Space instrumentation, Integrated circuit thermal modeling, Thermal modeling, Scientific instrument electronics**

I. Introduction

The Polarimetric Helioseismic Imager Electronics Unit (PHI E-Unit) is one of the two units the instrument PHI consist of. PHI is a remote sensing instrument that will operate onboard the Solar Orbiter mission [1] of the European Space Agency (ESA). Its main task is to study the Sun. To do it the perihelion of the orbit will be at 0.28 AU and the spacecraft will reach a solar latitude of 34°. This will allow remote sensing observations of the Sun from a distance without precedents, with a view of the solar poles and co-rotation of the spacecraft with the Sun.

The instrument PHI is the result of an international cooperation led by the Max-Planck-Institut für Sonnensystemforschung (MPS), Göttingen, Germany, co-led by the Instituto de Astrofísica de Andalucía (IAA-CSIC), Granada, Spain and with participation of the Grupo de Astronomía y Ciencias del Espacio (GACE/UV), Universidad de Valencia, Spain; Instituto de Astrofísica de Canarias (IAC), Tenerife, Spain; Instituto Universitario de Microgravedad "Ignacio Da Riva" (IDR/UPM), Universidad Politécnica de Madrid, Spain; Instituto Nacional de Técnica Aerospacial (INTA), Madrid, Spain; Universidad de Barcelona (UB), Spain; Institut d'Astrophysique Spatiale (IAS), Paris, France; Institute of Computer and Communication Engineering (IDA), Braunschweig, Germany and Kiepenheuer-Institut für Sonnenphysik (KIS), Freiburg, Germany.

The instrument PHI is mounted internally in the spacecraft, its Optics Unit contains two telescopes (a high resolution telescope, HRT, and a full disk telescope, FDT), together with the detectors and the subsystems needed to ensure the correct behavior of the telescopes. PHI E-Unit is a separate unit that carries all the electronics that manage the data and the subsystems of the Optics Unit and provide it with the necessary power. Both units are linked by the corresponding harness, but their thermal and mechanical behavior are decoupled. PHI passed all the required reviews and was accepted for flight in April 2017, following ESA standards. It is already assembled on the spacecraft and is waiting for launch.

During the perihelion the Solar Orbiter spacecraft willl receive a solar load equivalent to 13 solar constants, what makes the the thermal design of both the platform and the payload a very challenging task. PHI is one of the most demanding instrument in therms of power, mass and data rate. In addiction, PHI E-Unit design was constrained by its electromagnetic compatibility (EMC) footprint. The radiated emissions level has to be very low to avoid damaging the extremely sensitive sensors of the in-situ instruments.

These peculiarities and constrains of the mission make the thermal control crucial as it has to guarantee that in all phases of the mission the electronics components are within the appropriate range of temperatures. In general, during the last decade, the thermal design and modelling of space electronics has become a growing problem due mainly to the growing compactness of the electronics components, which leads to higher power density dissipations and may cause undesirable hot spots. The necessity of accurate and realistic temperature predictions is currently a matter of interest [2], [3], [4], [5], [6], and some efforts are being made to define standardized procedures, as the one under development by RAL [7]. In this paper, the procedure followed for the thermal calculations is described. In addition, the paper describes the thermal design of the unit, the problems encountered and the solutions found to fix those problems. The final predicted temperature levels achieved by the main electronics components are also shown.

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This work was supported by the Spanish Ministerio de Economía y Competitividad under grants ESP2014-56169-C6-1-R, ESP2014-56169-C6-4-R, ESP2014-56169-C6-6-R, ESP2016-77548-C5-1-R, ESP2016-77548-C5-3-R & ESP2016-77548-C5-5-R

Manuscript received July 20, 2018; revised March 1, 2019.

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These results have been correlated with thermal vacuum tests data.

II. PHI E-Unit Description

PHI E-Unit is a modular assembly consisting of six horizontally stacked modules, each of 200 mm x 200 mm in width and with a height of between 23 mm and 33 mm. Each module consists of one or two very populated dissipating PCBs, a supporting frame, and the connectors (subD, uD and High Voltage types) needed to communicate with the Optics Unit, with the other boards through another PCB, the so-called EDS (Electrical Distribution System), or with the spacecraft platform. The E-Unit total mass is around 6 kg. All the frames, together with the upper lid and the bottom baseplate constitute the housing of the unit. This modular design allows an easy integration and gives independence to each subsystem since it permits the assembly of the unit just staking and screwing the individual modules together once each one has been independently assembled. The screws used are made of Titanium (Ti6Al4V).

The modules, from bottom to top, are 1) Power Converter Module Main (PCM), 2) PCM Redundant (PCMR), 3) Data Processing Unit (DPU), 4) Tip-Tilt Controller (TTC) and DPU memory board, 5) Analog, Mechanisms and Heaters Drivers (AMHD), and 6) High Voltage Power Supply (HVPS). An exploded view of a 3D model of PHI unit can be seen in Figure 1. The PCM is the only electronics board that is redundant (PCM & PCMR), and it is a cold redundancy. It is also important to note that PHI requires a high voltage of about ± 5 kV, which is provided by the HVPS. For this reason, this board needs to be shielded, and this also blocks thermal radiation.

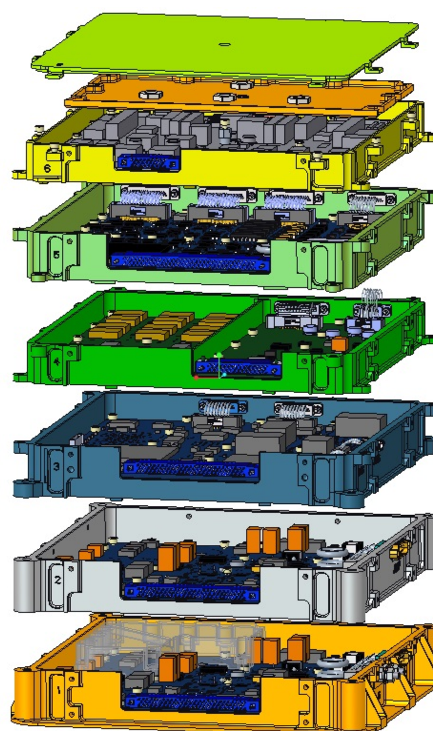

Fig. 1. PHI Electronics Unit exploded view.

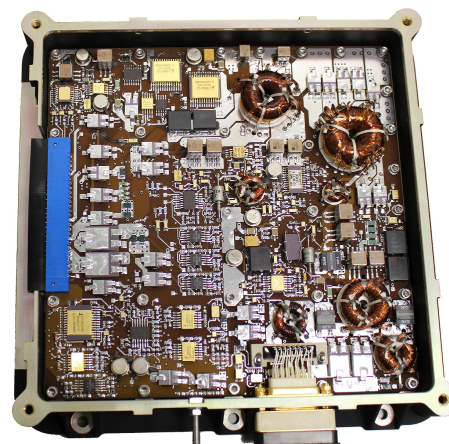

Fig. 2. PHI PCM board.

PHI E-Unit thermal design is driven by the stringent requirements of the components and the thermal environment, both described in Section III and IV. Furthermore, the design of this type of board is tailored on a case-by-case basis. Finding a configuration able to guarantee that all components are safe when operating at the most demanding conditions is a quite challenging task. Some facts that have driven the design are: a) the mass and power consumption have to be minimized in space applications; b) due to volume restrictions, these boards are more crowded than similar boards for other applications, for example, each PCM board contains more than 1200 components and 14 copper layers; c) the use of hard-rad components, able to cope with the radiation doses found in orbit, is mandatory; d) the electromagnetic noise generated has to be kept at very low limits. This makes it unsuitable for the thermal design to be treated separately, but on the contrary, as an important part of the systems engineering, with the need of trade-offs between thermal and other fields during the design process. A photograph of the PCM with its frame is shown in Figure 2.

The thermal control of the E-Unit was required to be fully passive. The use of heat pipes, widely used in both space and non-space applications, was also ruled out by the spacecraft main contractor as design baseline. For this reason, since the box is sitting on one of the panels of the spacecraft, it was designed to conduct most of the thermal power dissipated by the components to the baseplate. In this way, the design of the housing, the arrangement of the boards, and the arrangement of the electronics components on the boards were based taking into account, among other criteria, that it was necessary to provide an adequate thermal path to evacuate this dissipated power.

Furthermore, the location of each board in the unit was chosen on the basis of not only thermal but also mechanical criteria as, in addition to facilitate the heat rejection, it was necessary to keep the center of gravity centered and low, and to have access from each subsystem to the grounding and bonding connector. Thus, the most dissipating and heaviest modules (PCM main, PCM redundant and DPU) were placed at the bottom of the unit. The HVPS was located on the upper

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module due to the electrical requisites of the high voltage, even though the optocouplers temperature was higher than desired, as will be explained below.

Regarding the frames of the boards, they were provided with stiffeners and a local increase of thickness (thermal doublers) not only for structural reasons, but also to conduct the heat from the upper boards towards the base of the box. In addition, a thermal filler made of Choterm 1671 [8] was used to enhance conductive heat transfer between the unit baseplate and the spacecraft panel, helping this way to evacuate the heat dissipated within the unit.

The frames, baseplate and top lid of the box are made from Aluminum alloy 7075 T7351 with alodine protection, and are painted black on both sides with PUK black conductive coating from MAP [9]. The black external surface helps to maximize thermal radiation to the environment, whereas the internal black surfaces contribute to improve temperature homogeneity and avoid hot spots within the unit. Painting the internal surface of the unit is not a common practice in electronics, however, in this case, based on the analysis results it was completely necessary to meet the thermal requirements. The Aluminum alloy selected was also studied in depth. The thermal conductivity of the alloy selected is $\sim 155\,\mathrm{W\,m^{-1}\,K^{-1}}$. This is not optimal for thermal purposes, but the results are adequate for structural reasons and its machinability is acceptable. AlBeMet (an Aluminum Berylium composite material) was also considered as a good alternative, but was discarded after a trade-off study due to the difficulties of manipulation.

Regarding the EMC, the standard radiated emissions required in a space mission based on the ECSS [10] is about 60 dBuV/m up to $100\,\mathrm{MHz}$. But in Solar Orbiter, the E-Unit of PHI had to not pass 0 dBuV/m from $8\,\mathrm{kHz}$ up to $50\,\mathrm{MHz}$. To keep the radiated emissions as low as 0 dBuV/m additional aluminium plates were placed between the to DC/DC frames, special grounding measures were taken: the secondary ground was connected directly to chassis along all its planes in the PCB, and the DC/DC converter was covered by an aluminium hood. From the electronic point of view, the switching transistors were provided with a slower driving circuit to avoid too sharp switching edges.

Magnetic cleanliness was also a very strict requirement, forcing the use of titanium screws and other non-magnetic materials to keep the magnetic dipole below $20\,\mathrm{mA\,m^2}$ and the magnetic field transient below $24\,\mathrm{nT}$. The solution was to avoid the use of magnetic materials and current loops in the PCB design.

III. PHI E-Unit Thermal Requirements

PHI Electronics Unit thermal design is driven by the stringent requirements of the components and the thermal environment of the unit, both conductive and radiative. The nominal operational temperature range of the components given by the manufacturers in their data sheets must be derated following ECSS (European Cooperation for Space Standarization) standards [11], as required by ESA. In this regard, the derated temperature cannot be higher than $110\ ^{\circ}\mathrm{C}$ or $T_{junction} - 40\ ^{\circ}\mathrm{C}$, whichever is lower. In addition to the derating of the temperature range, ECSS standards also require a $\pm 10\ ^{\circ}\mathrm{C}$ margin to be applied to the results, in order to account for modeling and material properties uncertainties.

Critical issues as radiation hardening [12], export control approval (e.g. ITAR, EAR), long lead time (usually several months, and even a couple of years), components packaging limitation, soldering process qualification, etc. drive the space-qualified electronic components selection. Some of them are chosen from the European Preferred Parts List (EPPL).

The junction temperature allowable range of the most dissipating components of the different PCBs, once the derating rules are applied, are shown in Table I for both operating and non-operating conditions.

In addition to the electronic components internal requirements, the satellite main contractor imposes a thermal requirement in terms of the way the heat dissipated by the unit and is transferred to the spacecraft. In this way, the design must guarantee that not less than 80 % of the dissipated power is transferred via heat conduction to the spacecraft panel, dissipating the remaining power through thermal radiation to the spacecraft cavity.

IV. Thermal Loads and Boundary Conditions

The unit thermal loads are constituted by the power dissipated by the electronic components on the boards. The magnitude of these thermal loads depends on the working mode of the unit, which in turn depends on the system state and the orbital position. Since PHI is a set of two telescopes, two modes have been identified as design drivers for hot conditions: data acquisition (worst hot case for the PCM) and data processing (worst hot case for the DPU). For cold operational conditions, the instrument idle model is used. The total dissipation of each board for the three modes described above is shown in Table II. The dissipation on the PCM and the PCMR are identical as the PCMR is the redundant PCM, but these two boards never operates at the same time. For reasons of simplycity, only the total dissipation of each board has been included in the table. Nevertheless, for the numerical simulations described in the sections below, the power dissipation of the most dissipating components were considered individually (those listed in Table I), and the remaining power dissipation of each PCB was uniformly distributed on the board.

The values in the table were determined after an iterative process of temperature calculation and power consumption determination because the dissipation of some of the components depends in turn on their temperature levels. As described in section II the unit has a redundant power converter in case the main power converter fails. Each mode has been analyzed with nominal and redundant PCM boards on and off, respectively and vice-versa.

The distance of the spacecraft from the Sun together with the thermal management of the spacecraft, drive the boundary conditions. This is translated into the temperatures of the radiative and conductive interfaces. The worst hot and cold operational conditions are given at perihelion, 0.28 AU, and

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TABLE I
COMPONENTS JUNCTIONS ALLOWABLE TEMPERATURE RANGE

	Reference	Non Operational Range [°C] Min	Non Operational Range [°C] Max	Operational Range [°C] Min	Operational Range [°C] Max
PCM/R	Power MOSFET (IRHN9150)	-55	150	-55	110
	Common Mode Filter	-40	140	-40	100
	Differential Mode Filter	-40	140	-40	100
	Power MOSFET (IRHNJ57133SE)	-55	150	-55	110
	Transformer	-40	140	-40	100
	Schottky rectifier STPS1045CSHRB	-55	150	-55	110
	Coupled inductor	-40	140	-40	100
	Voltage regulator (ISL72991RHVF)	-55	150	-55	110
	Voltage regulator (RH1086BHK)	-55	150	-55	110
	Voltage regulator (LM2941GWRLQMLV)	-55	150	-55	110
DPU	LEON3-FT Processor	-65	150	-50	110
	RTAX FPGA	-60	150	-50	95
	Image Buffer SDRAM	-65	150	-40	105
	Power 1.2V	-65	150	-50	110
	Power 2.5V	-65	150	-50	110
	FPGA Xilinx V4-SX55	-65	150	-50	85
	FPA Drivers	-65	150	-50	110
	Working Memory SDRAM	-65	150	-40	105
	Power 1.5V	-65	150	-50	110
	Power 1.8V	-65	150	-50	95
	FPA Drivers	-65	150	-50	110
TTC	Voltage regulator (RHFL4913A)	-65	150	-65	110
	Operational amplifier (RHF484)	-65	150	-65	110
	Differential line receiver (DS90C032)	-65	150	-65	110
	Transistor (2N5666S)	-55	200	-55	110
	Power MOSFET (IRHF7130)	-55	150	-55	110
	Power MOSFET (IRHF9130)	-55	150	-55	110
AMHD	FPGA RTAX2000SL	-55	135	-45	95
	Operational amplifier (RH1499)	-55	150	-45	110
	Operational amplifier (ISL70417)	-65	150	-55	110
	Voltage regulator (RHFL4913A)	-55	150	-45	110
	Differential line driver (UT54LVDS031)	-55	150	-45	110
	Differential line receiver (UT54LVDS032)	-55	150	-45	110
	DC/DC (SMTR2812D)	-55	125	-45	85
HVPS	Operational amplifier (RH1014M)	-65	150	-65	85
	Power transistor (2N5666)	-65	200	-65	110
	Optocouplers (Micropak 66353)	-40	100	-40	60

TABLE II
POWER CONSUMPTION

	Dissipation [W]		
	Data Acquisition	**Data Processing**	**Instrument Idle**
PCM	13.45	11.38	8.29
PCMR	13.45	11.38	8.29
DPU	12.4	14.3	4.46
TTC	2.07	0.0	0.0
AMHD	2.48	1.76	1.45
HVPS	1.67	0.0	0.0
TOTAL	**31.9**	**27.5**	**14.2**

at the aphelion, 0.92 AU, of the science orbits, respectively. The conditions of the environment during operational phases are given in Table III. This table includes only the two environments presented in this paper, but more mission scenarios were studied.

TABLE III
EXTREME ENVIRONMENTAL CONDITIONS

	0.28 AU	**0.92 AU**
Radiative Environment	50 °C	-20 °C
Conductive IF (baseplate)	50 °C	-20 °C

V. GEOMETRICAL AND MATHEMATICAL MODEL

Following the common procedures used in space analysis, a geometrical mathematical model (GMM) and a thermal mathematical model (TMM) of the E-Unit were set up to compute temperatures and heat fluxes through the interfaces ([13], [14]). Although the heat equation is often solved by using finite elements methods (FEM) ([15], [16]) or analytical methods [17], in the space field the lumped-parameter method (LPM) is the most widely used ([13], [14]). In the LPM, the system is divided into a number of isothermal elements called thermal nodes, and the temperatures are obtained by solving the ordinary differential equations system shown in Eq. 1, which is in fact the energy equation applied to each node.

$$m_i c_i \frac{dT}{dt} = \dot{Q}_i + \sum_{j=1}^{n} GL_{ij} \left(T_j - T_i\right) + \sum_{j=1}^{n} GR_{ij} \sigma \left(T_j^4 - T_i^4\right) \tag{1}$$

In Eq. 1, m_i is the mass of the node i, c_i its specific thermal capacity, and $\dot{Q}_i$ its internal dissipation. Regarding the thermal couplings between nodes, GL_{ij} is the conductive (linear) thermal coupling between nodes i and j, with depends on the geometry, the thermal conductivity of the materials and the thermal contact conductance, and GR_{ij} the radiative exchange factor between nodes i and j, which depends on the geometry of the different surfaces involved in the infrared thermal radiation exchange, and on their infrared emissivity. The determination of these two couplings matrices is one of the most demanding tasks in thermal modeling, and requires the knowledge of a thermal engineer, even if a software tool is used.

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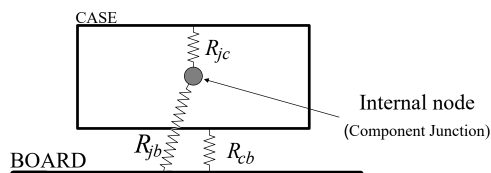

Fig. 3. Electronic components main thermal resistances model concept

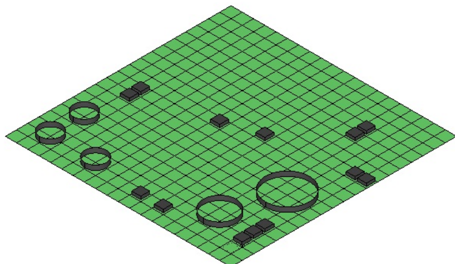

Fig. 4. GMM of the PCM board

The TMM of PHI E-Unit consists of 4570 thermal nodes. All the nodes have a geometrical representation to compute the thermal radiation exchange factor, with the exception of the electronic components junctions. The model includes the housing of the unit, the boards and the most significant electronic components in terms of power dissipation.

The electronic components are the most sensitive elements of the unit. Furthermore, it is in the electronic components where the fulfilment of the requirements has to be verified. For this reason, each electronic component with a significant dissipation was modeled by means of two thermal nodes: a non-geometrical junction node and a geometrical case node ([18], [19], [20], [21]), as shown in Figure 3. Thermal conduction between case and board, between junction and case, and between junction and board were considered through the thermal resistances junction-to-case R_{jc}, case-to-board R_{cb} and junction-to-board R_{jb}, respectively, obtained from the components datasheets and their mounting concept (for instance taking into account how the components were glued or soldered).

The boards were divided into elements of about 10 mm x 10 mm each. As example, the PCM GMM is shown in Figure 4. Even though the grid is uniform, the conductive thermal couplings between the elements of the boards are different, as they have been calculated on the basis of the number of copper layers of the board (between 6 and 18) and copper distribution on each layer [22], [23], [24]. The thermo-optical (infrared emissivity) and physical properties (thermal conductivity, density and specific heat capacity) used for the analysis are shown in Table IV and V, respectively. The values are given at room temperature but in the expected temperature range the variation of the physical properties are not significant. For this reason in the analyses they are considered constant.

TABLE IV
THERMO-OPTICAL PROPERTIES

Element	Surface finish	IR Emissivity
Box, Frames, Stiffeners	PUK black paint	0.88
PCBs	Conformal Coating	0.7

TABLE V
MATERIAL PROPERTIES

Material	k [W/mK]	ρ [kg/m^3]	c [J/kgK]
AA7075 T7351	155	2800	960
Copper	390	8964	393
Polyimide	0.25	1850	1200
Silicon Chip	105	2326	785

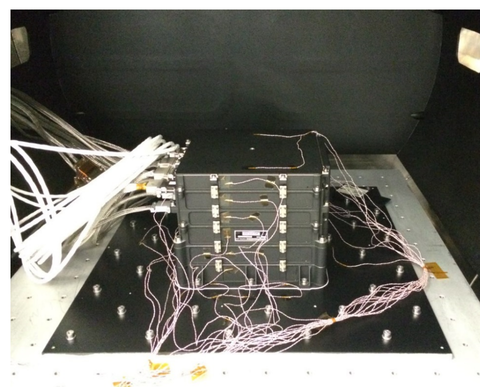

Fig. 5. PHI Electronics Unit QM on the mounting plate of the Thermal Vacuum Chamber

VI. THERMAL VACUUM TEST

Following the normal procedure in space projects defined by the standards ECSS, the design of the E-Unit was verified by means of thermal vacuum tests [25]. Three different tests were carried out during the different phases of the unit development. The first tests were performed on the so-called Structural Thermal Model (STM), a model representative of the flight unit in terms of physical properties, materials, centre of gravity (CoG), moment of inertia (MoI) and power dissipation. Second, a qualification test was carried out on the Qualification Model (QM). Finally, an acceptance test was performed on the Flight Model (FM), together with the Optics Unit and Harness, right before the delivery of the instrument for its integration on the spacecraft.

Figure 5 shows a picture of the E-Unit QM thermal test mounted on the Thermal Vacuum Chamber mounting plate. The unit was tested in the thermal vacuum chamber of the IDR/UPM [26].

The dissipation cases studied in the thermal mathematical model and previously shown in Table II were tested. The model was equipped with 30 temperature sensors to monitor the temperatures of the relevant parts of the unit. The QM test was a functional test, where the E-Unit was switched on and

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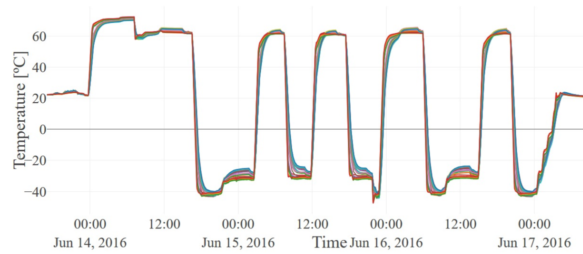

Fig. 6. PHI Electronics Unit QM temperature evolution during the qualification tests

off several times and the different modes were evaluated during the test to verify the proper functioning of the equipment.

A profile showing the temperature of the sensors and the pressure level during the test is shown in Figure 6 for one of the test campaigns. The temperatures read during the test were found to be within $\pm 4\,^{\circ}\mathrm{C}$ error for the structural parts and up to $\pm 8\,^{\circ}\mathrm{C}$ error for the components.

The thermal model described in Section V was correlated with the data measured during the test. The model-to-test correlation method based on the Jacobian matrix [27] was applied for this purpose. The correlation was done over the thermal contact conductances estimated during the design process. The average contact conductance between the PCBs and the frames was found to be around $200\,\mathrm{W\,m^{-2}\,K^{-1}}$.

VII. ANALYSES RESULTS

The thermal model was run for the extreme operational cases described in Table III. It was iterated and updated in different ways. First, as already said, the power dissipation was updated based on the model results to take into account the components temperature dependance. Second the model was updated with the results of the model-to-test correlation, and third, all along the design phase the design was iterated until reaching a solution adequate for most electronics components. During this iterative process, it was found that the most dissipating element, the FPGA, with the initial design, reached temperatures above its allowable limit. To solve this problem, the design of the DPU module was modified. First, it was necessary to move this highly dissipating element closer to the edge of the board, to ease heat conduction to the frame. Initially, the FPGAs were placed around the centre of the board, at almost $48\,\mathrm{mm}$ from the frame. In the final design, the distance, which is the minimum possible, is around $5\,\mathrm{mm}$. An additional copper layer of $35\,\mathrm{\mu m}$ was added in the areas in contact with the frame [28] in order to maximize the thermal contact conductance between board and frame. Furthermore, it was also necessary to locally increase the thickness of the frame stiffeners in the area of the FPGA in order to enhance heat conduction. This way, it acted as a thermal doubler. With all these modifications the operating temperature of the FPGA was reduced from $95\,^{\circ}\mathrm{C}$ to $85\,^{\circ}\mathrm{C}$, in its worst case (Table VII).

In the PCM and PCMR boards the copper layouts were also modified to achieve a better conduction of the heat to the frame. Special attention was paid in the area of the DC/DC converter, where the diodes and the MOSFETs temperatures

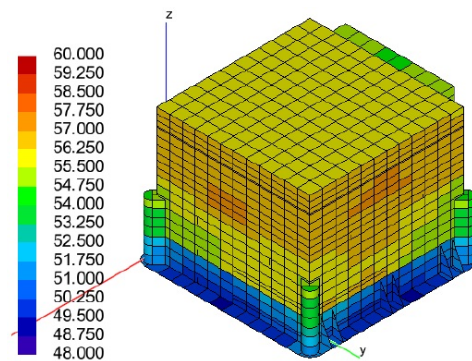

Fig. 7. PHI Electronic Unit. Data Processing redundant case.

were critical. Based on this fact, the layout of the PCB was designed taking into account the thermal results as well as the frame. The contact area with the frame around these components was increased to permit the correct evacuation of the heat. This modification decreased the temperature of the component from $84\,^{\circ}\mathrm{C}$ to $75\,^{\circ}\mathrm{C}$ (Table VI).

Another problem was found with the optocouplers of the HVPS board. In this case, the elements dissipate a negligible amount of power, and the violation of the requirement was due to the application of the de-rated margins. The maximum allowed temperature after the de-rating was below the environmental condition in the hot case. Due to the non-criticality of these elements, a request for deviation (RFD) was raised to ESA, who accepted this non-compliance.

The complete temperature maps were obtained for all boards and housing for the different modes defined in Table I with the nominal and redundant PCM. For brevity, only the results for the two most critical boards and load cases are presented in this paper: the PCMR during the Data Acquisition Mode and the DPU during the Data Processing Mode. The results correspond to the final configuration achieved after the design iterations and the correlation with the thermal vacuum tests. The temperature map of the unit housing for Data Processing Mode is shown in Figure 7.

Regarding the boards, Figure 8 shows the temperature map of the PCMR board, and Figure 9 the DPU, two of the most critical boards. Since the junction nodes of the components are not geometrically represented, Table VI and VII show the results obtained at this level. As can be seen, all the elements are within their appropriate working margins.

The results obtained from the thermal analysis were used for the thermo-elastic analysis of the unit. All deformations were within the allowable values and no major problem was found in this regard.

From the analyses, the heat rejection paths were evaluated. Thus, Table VIII shows the heat transferred through each interface in the data acquisition nominal case. It can be seen that in this mode most of the heat is conducted through the baseplate (83.7 %) whereas only 16.3 % is radiated to the spacecraft enclosure. This fact meets the thermal requirement imposed by the satellite main contractor described in Section III.

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TAES.2019.2911734, IEEE Transactions on Aerospace and Electronic Systems

TABLE VI
PCMR JUNCTION TEMPERATURES FOR DATA ACQUISITION MODE

Reference	Operational Range [°C]		Model Results [°C]	
	Cold	Hot	Nominal	Redundant
Power MOSFET #1 (IRHN9150)	-55	110	63	70
Power MOSFET #2 (IRHN9150)	-55	110	63	70
Common Mode Filter	-40	100	63	70
Differential Mode Filter #1	-40	100	63	69
Differential Mode Filter #2	-40	100	63	71
Power MOSFET #1 (IRHNJ57133SE)	-55	110	63	75
Power MOSFET #2 (IRHNJ57133SE)	-55	110	63	75
Transformer	-40	100	63	75
Schottky rectifier #1 (STPS1045CSHRB)	-55	110	63	75
Schottky rectifier #2 (STPS1045CSHRB)	-55	110	63	76
Schottky rectifier #3 (STPS1045CSHRB)	-55	110	63	72
Schottky rectifier #4 (STPS1045CSHRB)	-55	110	63	83
Schottky rectifier #5 (STPS1045CSHRB)	-55	110	63	82
Coupled inductor	-40	100	63	72
Voltage regulator #1 (ISL72991RHVF)	-55	110	64	83
Voltage regulator #1 (RH1086BHK)	-55	110	64	83
Voltage regulator #2 (RH1086BHK)	-55	110	64	86
Voltage regulator #3 (RH1086BHK)	-55	110	64	81
Voltage regulator #2 (ISL72991RHVF)	-55	110	63	85
Voltage regulator (LM2941GWRLQMLV)	-55	110	64	94

TABLE VII
DPU JUNCTION TEMPERATURES FOR DATA ACQUISITION MODE

Reference	Operational Range [°C]		Model Results [°C]	
	Cold	Hot	Nominal	Redundant
LEON3-FT Processor	-55	110	80	82
FPGA RTAX2000	-50	95	82	84
Image Buffer #1 SDRAM	-40	105	77	78
Image Buffer #2 SDRAM	-40	105	74	76
POL-Regulator 1.2 V	-50	110	82	84
POL-Regulator 2.5 V	-50	110	75	77
FPGA Xilinx V4SX55 #1	-50	85	84	85
FPGA Xilinx V4SX55 #2	-50	85	79	81
FPA Drivers	-55	110	69	71
SDRAM Memory	-40	105	78	80
LDO-Regulator 1.5 V	-50	110	86	88
LDO-Regulator 1.8 V	-50	95	76	78
Image Buffer #3 SDRAM	-40	105	76	78
Image Buffer #4 SDRAM	-40	105	74	76
FPA Drivers	-55	110	69	71

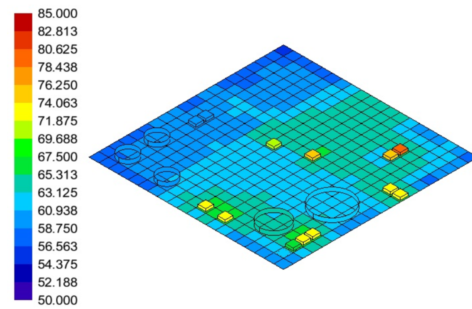

Fig. 8. PCMR. Hot Data Acquisition redundant case.

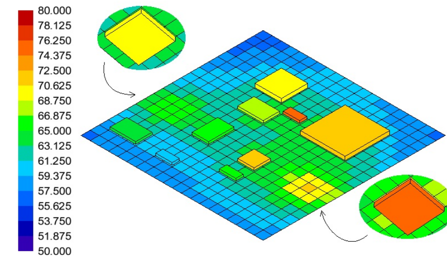

Fig. 9. DPU. Hot Data Processing case.

TABLE VIII
HEAT THROUGH THE INTERFACES

	[W]	**%**
Conductive	25.9	83.7
Radiative	5.0	16.3
Total	30.9	100.0

VIII. CONCLUSION

The thermal design and performance of ESA Solar Orbiter PHI Electronics Unit has been presented. The thermal mathematical model proved to be a reliable source for analyses. Many iterations were made involving both the thermal and electronics subsystems to fix the problems encountered during the design process.

The thermal vacuum test (section VI) showed that the thermal mathematical model was in line with the test data. Only small variations of the contact conductance between the frames and the boards were needed to update the mathematical model.

ACKNOWLEDGMENT

This work has been supported by the Spanish Ministerio de Economía y Competitividad, Projects ESP2014-56169-C6-1-R, ESP2014-56169-C6-4-R, ESP2014-56169-C6-6-R, ESP2016-77548-C5-1-R, ESP2016-77548-C5-3-R & ESP2016-77548-C5-5-R. The author Javier Piqueras is supported by the grant FPU15/05618 'Formación de Profesorado Universitario' from the Spanish Ministerio de Educación, Cultura y Deporte.

The authors thank all the members of the PHI team involved in the development of PHI electronics unit.

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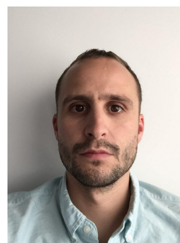

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