

Article

Optimized Design of 1 MHz Intermediate Bus Converter Using GaN HEMT for Aerospace Applications

Enrique Maset ^{1,*}, Juan Bta. Ejea ¹, Agustín Ferreres ¹, José Luis Lizán ¹, Jose Manuel Blanes ², Esteban Sanchis-Kilders ¹ and Ausias Garrigós ²

¹ Department Electronic Engineering, University of Valencia, 46100 Burjassot, Spain; juan.b.ejea@uv.es (J.B.E.); agustin.ferreres@uv.es (A.F.); J.L.Lizan@uv.es (J.L.L.); esteban.sanchis@uv.es (E.S.-K.)

² Industrial Electronics Group, Miguel Hernández University of Elche, 03202 Elche, Spain; jmblanes@umh.es (J.M.B.); augarsir@umh.es (A.G.)

* Correspondence: Enrique.maset@uv.es

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Abstract: This paper presents the possibility of using Gallium Nitride (GaN) high-electron-mobility transistors (HEMTs) instead of the conventional silicon metal oxide semiconductor field effect transistor (MOSFET) to implement a high-frequency intermediate bus converter (IBC) as part of a typical distributed power architecture used in a space power application. The results show that processing the power at greater frequencies is possible with a reduction in mass and without impacting the system efficiency. The proposed solution was experimentally validated by the implementation of a 1 MHz zero-voltage and zero-current switching (ZVZCS) current-fed half-bridge converter with synchronous rectification compared with the same converter using silicon as the standard technology on power switches and working at 100 kHz. In conclusion, the replacement of silicon (Si) transistors by GaN HEMTs is feasible, and GaN HEMTs are promising next-generation devices in the power electronics field and can coexist with silicon semiconductors, mainly in some radiation-intensive environments, such as power space converters. The best physical properties of GaN HEMTs, such as inherent radiation hardness, low on resistance and parasitic capacitances, allow them to switch at higher frequencies with high efficiency achieving higher power density. We present an optimized design procedure to guaranty the zero-voltage switching condition that enables the power density to be increased without a penalization of the efficiency.

Keywords: aerospace power buses; high-electron-mobility transistor (HEMT); gallium nitride (GaN); intermediate bus converter (IBC)

1. Introduction

Mass is one of the most critical parameters in aerospace applications due to the cost of launching and the need to accommodate increasing payloads. Therefore, the lower the weight of the platform, the larger the mass available for useful loads, like transponders in telecommunication satellites. Consequently, the mass reduction of the power systems is one of the main aims of advances in aerospace technology. This mass reduction is associated with (1) an increase of the efficiency of DC/DC power conversion units, which reduces the associated thermal dissipation and permits the use of smaller solar panels and batteries, and (2) a size reduction of the reactive components of power converters (inductors, transformers, and capacitors) when switching frequency is increased.

Currently DC/DC power converters used in the aerospace field are based on hard rad Si (Silicon) metal oxide semiconductor field effect transistor (MOSFETs) as switching devices. Si MOSFETs

have relatively high gate parasitic capacitance, jeopardising further efficiency improvement and switching frequency increase (i.e., converter size reduction) with respect to the present state of the art. This situation proves critical for Telecom applications as the respective spacecraft power level may be up to one order of magnitude larger than a typical scientific mission (20 kW against 2 kW). In this context, Telecom power converter unit (PCU) dissipation constitutes a strong platform design driver, while their payloads constituted by electronic power converters (EPC) for traveling wave tube amplifiers (TWTAs) demand higher power conversion efficiency especially in view of the hundreds of units on board of each spacecraft. Si MOSFETs behave robustly given the radiation received in the space environment and are efficient when working at switching frequencies in the order of 100 to 200 kHz. However, the switching frequency cannot be increased to the MHz range using silicon technology due to the large increase in power losses. Therefore, a semiconductor material is required to implement electronic switches that are able to process power at higher frequencies (in the MHz range) with higher efficiency, which would represent a revolution in switching power systems.

Semiconductor materials showing potential for this application are those with a wide band gap, particularly gallium nitride (GaN) and silicon carbide (SiC) [1]. These materials have exceptional physical properties that make them especially adapted for high-frequency and high-power electronic applications, offering high robustness against high temperatures and radiation [2]. GaN HEMTs devices were selected over SiC because SiC does not have adequate baseline radiation hardness assurance capability built into it like GaN does. Single event burnout (SEB) often occurs for 1.2 kV SiC MOSFETs at voltages 50% or lower than specified breakdown [3].

Over the past years, commercial normally OFF GaN HEMTs have been tested against irradiation and the results are published in recent papers. The design and analysis are often performed for normally OFF commercial GaN HEMTs giving a very high resistance to displacement damage and ionizing effects, far outdoing that of commercial Si and SiC MOSFETs [4–10]. Furthermore, the conduction resistance in these wide band gap semiconductor devices is an order of magnitude lower than in silicon materials, without the corresponding increase in the gate capacitance. This decreases the conduction losses, allowing an increase in the switching frequency and a size reduction of the reactive components.

The aim of this study was to explore the use of GaN high-electron-mobility transistors (HEMTs) in a real DC/DC converter for a space power application using commercial parts already available on the market. Only replacing the Si MOSFET with GaN HEMTs did not achieve true improvement. We need to perform soft switching transitions (ZVZCS) in the transistors, in order to reduce the switching losses and, thus, together with the low conduction losses that GaN offers, allow the frequency to be increased to the MHz range without penalizing performance. Several design studies are available in the literature for terrestrial applications as telecom servers or solar inverters [11,12] with similar converters, but they do not define an optimized design to achieve ZVZCS that allow an increase up to MHz for switching frequency. In our study, an optimized design procedure is explained. Similarly, there are some papers with GaN HEMTs in power converters for space applications, but without soft-switching techniques [13]

We show that using GaN technology is possible in space power conversions, considering all particularities of space application design, and silicon devices can be replaced by GaN devices in applications where their advantages are enhanced, as soon as they are available as space-qualified parts [14]. To achieve this objective, an intermediate bus converter working at 1 MHz was designed and implemented. The experimental results and performances were compared with the same converter using silicon as the standard technology on power switches and working at 100 kHz.

2. Distributed Power Architecture

At present, a distributed-type power architecture is used rather than a centralized one, due to the poor static and dynamic voltage regulation, and inferior fault tolerance, to feed low voltage loads. The satellite technology demand in digital and radio frequency (RF) applications presents a challenge

to power distribution systems. Digital and RF loads demand ever lower voltage levels to remain efficient with the ever-higher operating frequencies to increase power density.

These types of loads demand high performance from their power sources, with accurately regulated low voltages (1 to 3.3 V), high currents up to 20 A, and fast transient responses. The well-known and proven centralized power distribution architectures are incapable of meeting all these requirements while minimizing weight and space on board. Distributed power architectures (DPAs) with DC/DC point-of-load (POL) converters seem to be a promising solution [15–17]. Depending on the constraints and with a suitable design, these DPAs with POL architecture could provide an efficient solution for digital electronics loads and for general secondary power distribution purposes in aerospace systems.

Galvanic isolation, conversion, and voltage regulation are implemented using two cascaded converters in a distributed architecture. The first converter is an intermediate bus converter (IBC), which is responsible for galvanic isolation, and converts the main bus voltage to an intermediate voltage level. The second converter is a non-isolated POL converter, which transforms this intermediate voltage to the level required by the load voltage. The POL converters are physically near to the load circuits, where the DC distribution losses are minimized and parasitic inductance is reduced, thereby improving the performance and dynamic response [18]. Figure 1 shows a basic distributed power architecture (DPA).

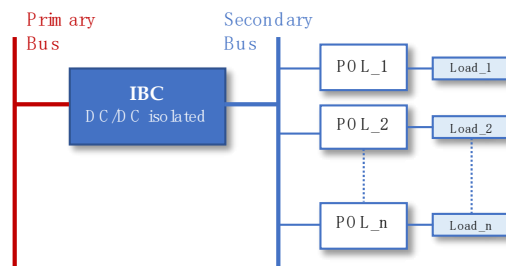


Figure 1. Intermediate bus converter (IBC) converter in a distributed power architecture. POL: point of load.

Some design restrictions must be considered to ensure the compatibility of the IBC and the POL impedance overlap. The selection of the IBC voltage level requires special attention because of its impact on the global system efficiency and the constraints implied for the POL design optimization. To validate the benefits of this power distribution system, the output voltage of the IBC was chosen to be compatible with the input of the POL, and a high output current for the required power level was chosen.

3. Intermediate Bus Converter

A suitable topology for the IBC was chosen considering parameters such as efficiency, power switch stress, manufacturing complexity, and cost. The result was a trade-off among three primary topologies: push-pull, half-bridge, or full-bridge. Regarding the output arrangement for these proposed converters, two secondary output schemes are available: the centre-tapped or the current doubler rectifier. The converter selected was a current-fed half-bridge topology with galvanic isolation and synchronous rectification in the secondary side. It is the best compromise considering efficiency, sizing of key parts and cost. This topology has been chosen because voltage stress of primary power mosfets cannot exceed power bus voltage, and synchronous rectification to reduce the conduction losses of secondary side. Figure 2 shows a simplified schematic of this configuration.

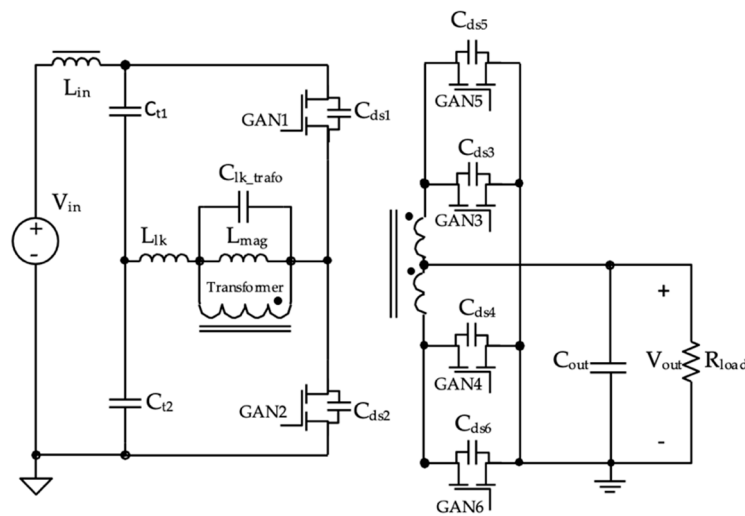


Figure 2. Simplified schematic of a zero-current and zero-voltage switching (ZVZCS) current-fed half-bridge converter considering the main parasitic elements.

In this topology, we take advantage of parasitic elements such as the leakage inductance of the transformer (L_{lk}) and the parasitic capacitance of the power transistors (C_{ds}) (Figure 2) to obtain a resonant switching behaviour, which provides higher performance than the conventional hard switching half-bridge. With a proper design, we can obtain zero-voltage and zero-current switching (ZVZCS) commutations [19].

In the next section, we show that the value of the tuning capacitors (C_{t1} , C_{t2}) has to be adjusted to achieve zero-current switching. This value has to guarantee that the current resulting from the resonance between each one of these capacitors and the leakage inductance of the transformer (L_{lk}) are zero at both the beginning and the end of the conduction time intervals (T_{on}), i.e., when the turn-on and turn-off switching transitions of the transistors are produced.

The transistors turn on after the off-time intervals (T_{gap} ; Figure 3). To achieve zero-voltage switching, the transformer has to be designed with a proper magnetizing inductance value. This value has to ensure that the current flows through this inductance at the end of both conduction intervals T_{on} , and therefore its stored energy, are large enough to perform the following actions during T_{gap} :

- Complete discharge of the parasitic capacitances C_{ds} of both the half-bridge transistors and the synchronous rectifier transistors, which will be turned on after T_{gap} ;
- Complete charge of the parasitic capacitances (C_{ds}) of both the half-bridge transistors and the synchronous rectifier transistors that have just turned off;
- Complete charge of the transformer parasitic capacitance (C_{lk_trafo}).

GaN HEMT transistors were selected to implement secondary side synchronous rectification due to their low channel resistance, higher achievable switching frequency (their rise and fall times are in the order of a few nanoseconds), and the absence of a source to drain parasitic diode, which allows the transistor conduction to be controlled in that direction. The use of this feature in the synchronous rectifier is explained in more detail in Section 3

Finally, the arrangement of the GaN HEMT of the synchronous rectifier stage was chosen to ensure a current flow from source to drain. Thereby, the gate trigger of these transistors was easier because the reference point was the output ground. As shown in Figure 2, each rectifier branch was constituted by two paralleled transistors to reduce the channel resistance in conduction mode.

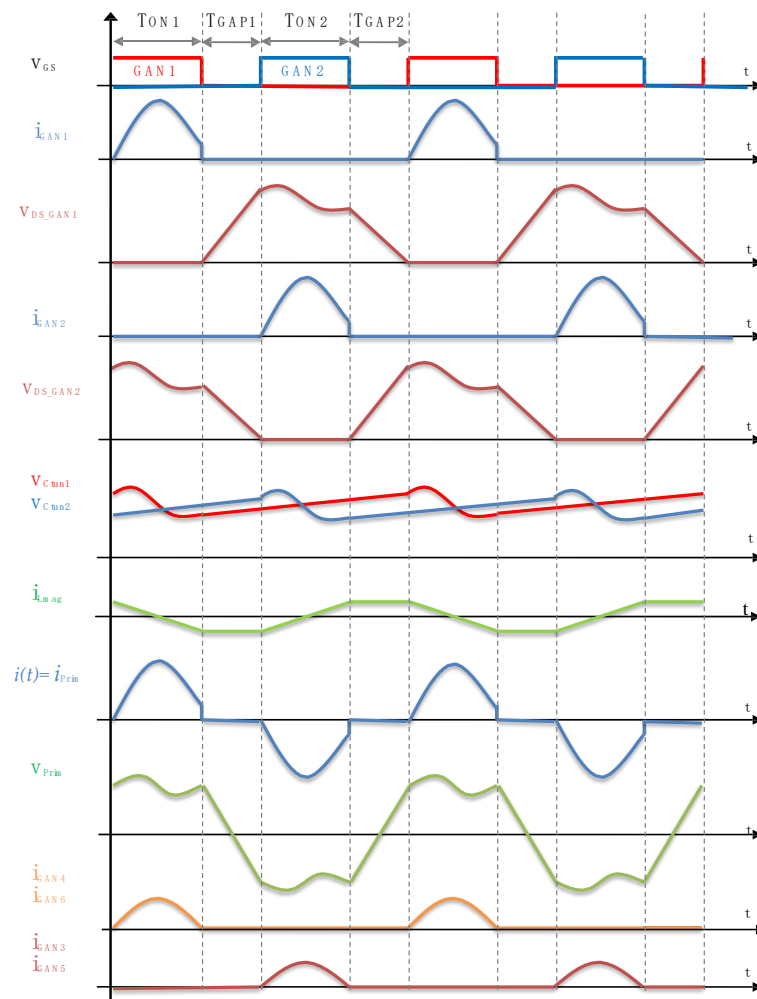


Figure 3. Theoretical time waveforms useful for the analysis of the ZVZCS resonant converter.

3.1. Circuit Description and Operation Principle

The main waveforms of the converter are shown in Figure 3, on which the explanation that follows will be based. The switching sequence of the primary-side transistors follows the order established by the operation of a classical half-bridge converter with a maximum duty cycle of 50% for each transistor. The operation of this converter will consist of a succession of four states: T_{on1} , GAP_1 , T_{on2} , and GAP_2 . Table 1 reflects the condition for each transistor that will have in each state.

Table 1. Transistors conditions for each state.

Device	Interval			
	T_{on1}	T_{GAP1}	T_{on2}	T_{GAP2}
GAN1	ON	OFF	OFF	OFF
GAN 2	OFF	OFF	ON	OFF
GAN3, GAN5	OFF	OFF	ON	OFF
GAN4, GAN6	ON	OFF	OFF	OFF

For simplicity, we distinguish only two equivalent states: the conduction of one of the transistors in primary side (GAN1 or GAN2) ($T_{on} = T_{on1} = T_{on2}$) and the non-conduction of both transistors ($T_{gap} = T_{GAP1} = T_{GAP2}$). Transistors GAN3 and GAN5 of the synchronous rectifier conduct during the on time of the GAN2 transistor, whereas transistors GAN4 and GAN6 conduct during the on time of transistor GAN1.

During T_{on1} , the transistor GAN1 is in conduction mode and the resonance between the capacitor C_{t1} and the leakage inductor of the transformer (L_{lk}) takes place. Its equivalent circuit is shown in Figure 4a. This resonance is evidenced by the sinusoidal waveform of the current flowing through the primary of the transformer ($i(t)$ in Figure 3). This resonant current is reflected to the secondary side of the transformer and flows through the GAN4 and GAN6 transistors in the source to drain direction, finally feeding the output load after being filtered by capacitor C_{out} . Both the turning on and off of transistors GAN1, GAN4, and GAN6 occurs when the current flowing through them is zero. However, a small amount of current is circulating through them at these moments due to the magnetizing inductance of the transformer, which contributes to charging/discharging the parasitic capacitances.

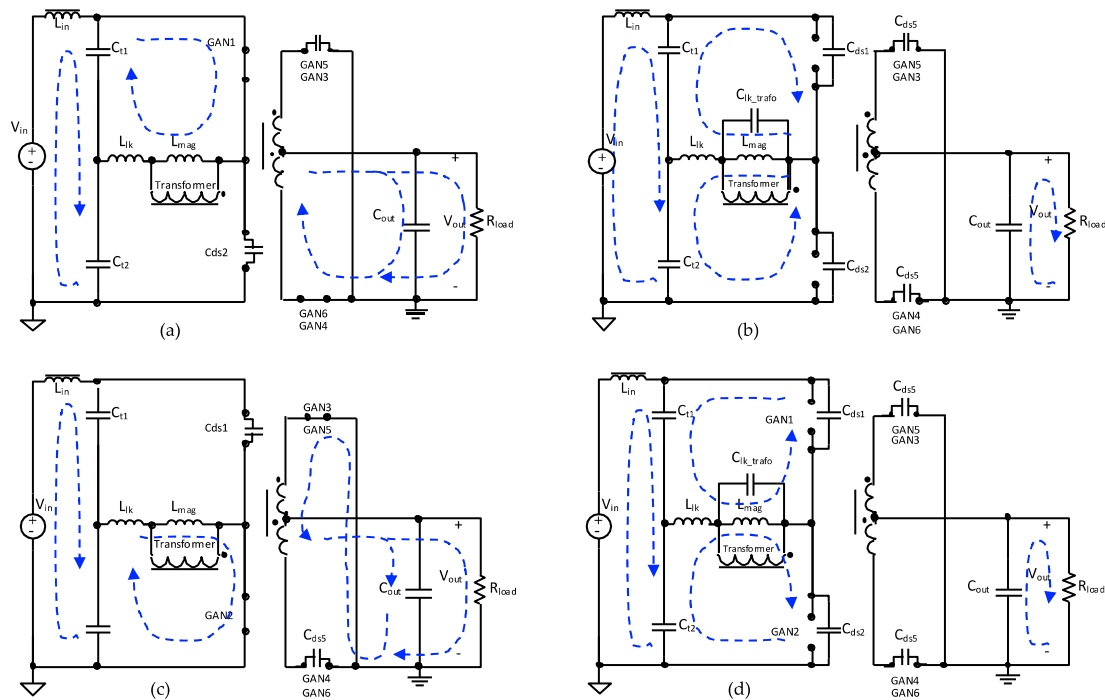


Figure 4. Sub circuit intervals during different operating states of the ZVZCS resonant converter. (a) Equivalent circuit during T_{on1} state (GAN1 ON) (b) Equivalent circuit during T_{gap1} state (GAN1 and GAN2 OFF). (c) Equivalent circuit during T_{on2} state (GAN2 ON) state. (d) Equivalent circuit during T_{gap2} state (GAN1 and GAN2 OFF).

When the T_{on1} interval finishes, the gap state (T_{gap1}) starts. During this time interval, the transformer magnetizing current charges the drain-source capacitor of GAN1 (C_{ds1}) to an approximate value of V_{in} and discharges the drain-source capacitor of GAN2 (C_{ds2}) to zero volts. Simultaneously, part of the magnetizing current is reflected to the secondary side of the transformer and charges the drain-source capacitors of the GAN3 (C_{ds3}) and GAN5 (C_{ds5}) transistors to a voltage V_{out} , and discharges the drain-source capacitors of GAN4 (C_{ds4}) and GAN6 (C_{ds6}) to zero volts. Finally, another small part of the magnetizing current charges/discharges the parasitic capacitance of the transformer (C_{lk_trafo}). Once the capacitor charge/discharge process is finished, the GAN2, GAN4, and GAN6 transistors turn on at zero voltage, and a new T_{on} interval, equivalent to the previous one, will occur, although now it will be the capacitor C_{t2} that will resonate with L_{lk} .

During the gap interval, the linear charge of both capacitors C_{t1} and C_{t2} is also produced via the input current source I_{Lin} . The charge of C_{t1} starts after its resonance interval. The charge of C_{t2} , which began after the end of its corresponding resonance interval, continues in this interval.

A deeper analysis of the different equivalent circuits was required to obtain the design equations that allow the converter design to be optimized.

3.1.1. T_{on} Interval

The equivalent circuit used for the mathematical analysis of the conduction interval of the transistors is shown in Figure 5, where V_o , C_o , and R_o are the output voltage, the output capacitor and the load values of the components present in the secondary side of the transformer reflected to the primary side, respectively.

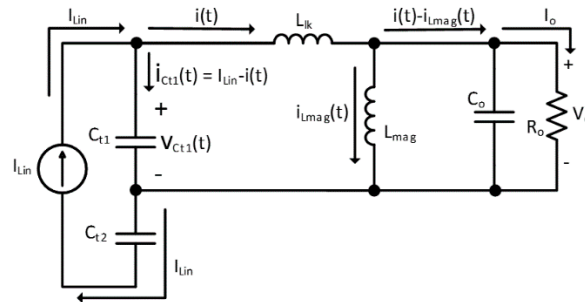


Figure 5. T_{on} equivalent circuit. V_o , C_o , and R_o are the output voltage and the values of the components present in the secondary side of the transformer reflected to the primary side, respectively.

As the value of C_o is much larger than the resonance capacitances and its series equivalent resistance (ESR) is very low, V_o was considered constant. A complete period of operation of the converter T is constituted by the addition of two T_{on} time intervals and two T_{gap} time intervals ($T = 2 \cdot T_{on} + 2 \cdot T_{gap}$).

To simplify the process for obtaining the equations that define the behaviour of the circuit in the T_{on} time interval, the magnetizing current $i_{Lmag}(t)$ was neglected because of its small value in relation to the overall current flowing through the primary of the transformer $i(t)$. This reduced magnetizing current grows linearly during the T_{on} time interval since the voltage across L_{mag} is V_o .

Calculation of $i(t)$

As a prior step to obtaining the differential equation that defines the behaviour of $i(t)$, the voltage drop across the capacitor C_{t1} can be deduced from Figure 5, where L_{lk} is the leakage inductor of the transformer:

$$v_{C_{t1}}(t) = L_{lk} \frac{di(t)}{dt} + V_o \quad (1)$$

The derivative in Equation (1) is:

$$\frac{d v_{C_{t1}}(t)}{dt} = L_{lk} \frac{d^2 i(t)}{dt^2} + \frac{dV_o}{dt} \quad (2)$$

We know that:

$$\frac{d v_{C_{t1}}(t)}{dt} = \frac{i_{C_{t1}}(t)}{C_{t1}} \quad (3)$$

Substituting Equation (3) into Equation (2), the tuning capacitor current is:

$$\frac{i_{C_{t1}}(t)}{C_{t1}} = L_{lk} \frac{d^2 i(t)}{dt^2} \quad (4)$$

According to the circuit topology in Figure 4, the tuning capacitor current verifies the following relation:

$$i_{C_{t1}}(t) = I_{Lin} - i(t) \quad (5)$$

where I_{Lin} is the DC input current of the converter for a given output power.

Substituting Equation (5) into Equation (4) and rearranging terms, we obtain the following differential equation:

$$\frac{d^2 i(t)}{dt^2} + \frac{i(t)}{L_{lk} \cdot C_{t1}} = \frac{I_{Lin}}{L_{lk} \cdot C_{t1}} \quad (6)$$

The solution to this differential equation is given by:

$$i(t) = I_{Lin} - I_{pk} \cos(\omega_{Ton} t + \varphi) \quad (7)$$

where ω_{Ton} is the resonance frequency during T_{on} , which is determined by:

$$\omega_{Ton} = \frac{1}{\sqrt{L_{lk} \cdot C_t}} \quad (8)$$

where $C_t = C_{t1} = C_{t2}$. Fixing a null value of the primary current at the beginning of the time interval, the value of the angle φ must satisfy the following expression:

$$I_{pk} = \frac{I_{Lin}}{\cos \varphi} \quad (9)$$

Substituting Equation (9) into Equation (7), $i(t)$ is obtained as:

$$i(t) = I_{Lin} - \frac{I_{Lin}}{\cos \varphi} \cos(\omega_{Ton} t + \varphi) \quad (10)$$

with a maximum value of:

$$I_{max} = I_{Lin} \left(1 + \frac{1}{\cos \varphi} \right) \quad (11)$$

The value of $\cos \varphi$ will be determined later applying the current balance in the tuning capacitors. Equation (11) will be used to select the current specification requirement of the HEMTs. The appearance of the waveform of the primary current $i(t)$ during T_{on} is shown in Figure 6.

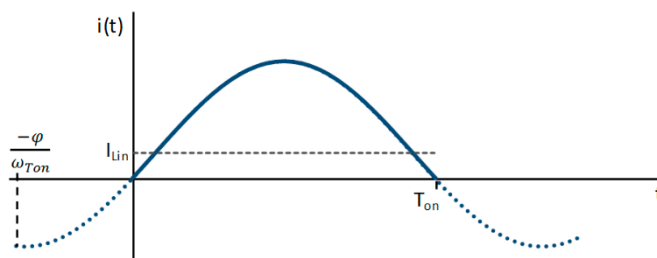


Figure 6. Primary current of the transformer $i(t)$ during T_{on} time interval.

In Equation (10) that the primary current has to be zero at the end of the T_{on} time interval:

$$\cos(\omega_{Ton} T_{on} + \varphi) = \cos(\varphi) \quad (12)$$

The following expression, which is used afterward, is obtained when the cosine of the first term of Equation (12) is developed:

$$\cos(\omega_{Ton} T_{on}) - \text{tg}(\varphi) \cdot \sin(\omega_{Ton} T_{on}) = 1 \quad (13)$$

Calculation of $v_{Ct1}(t)$

Next, the equation that determines the behaviour of $v_{Ct1}(t)$ during T_{on} as a result of the resonance between C_{t1} and L_{lk} is calculated. To do this, the derivative of $i(t)$ is found from Equation (10) and replaced in Equation (1):

$$v_{C_{t1}}(t) = L_{lk} \frac{I_{L_{in}}}{\cos \varphi} \omega_{T_{on}} \text{sen}(\omega_{T_{on}} t + \varphi) + V_o \quad (14)$$

Then, the voltages across the tuning capacitor at the beginning and at the end of the T_{on} interval are obtained from Equation (14):

$$v_{C_{t1}}(0) = L_{lk} I_{L_{in}} \omega_{T_{on}} \frac{\text{sen} \varphi}{\cos \varphi} + V_o \quad (15)$$

$$v_{C_{t1}}(T_{on}) = L_{lk} \frac{I_{L_{in}}}{\cos \varphi} \omega_{T_{on}} \text{sen}(\omega_{T_{on}} T_{on} + \varphi) + V_o \quad (16)$$

Figure 4 shows that the mean value of voltage $v_{C_{t1}}$ in the T_{on} interval must be V_o (neglecting losses), as shown in Figure 7, which describes the variation in $v_{C_{t1}}(t)$ in a complete period of operation of the converter.

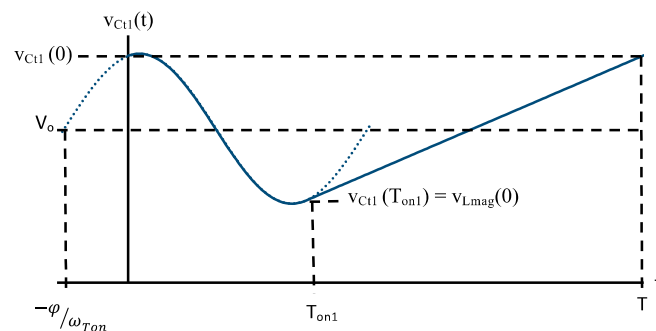


Figure 7. Evolution of the voltage across the tuning capacitor $v_{C_{t1}}(t)$ during a switching period.

3.1.2. T_{gap} Interval

In the following calculations, neither the leakage inductance nor the parasitic capacitance of the transformer is considered due to their small values compared to the magnetizing inductance of the transformer and to the parasitic capacitances of the GaN HEMT, respectively. For the step-down transformer, the parasitic capacitances of the GaN HEMT in the synchronous rectification stage can be neglected, as their values reflected to the primary side are much lower than those of C_{ds1} and C_{ds2} . Figure 8 shows the equivalent circuit for the T_{gap} time interval.

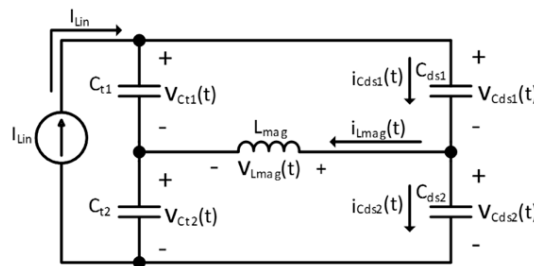


Figure 8. T_{gap} equivalent circuit.

Calculation of $v_{C_{t1}}(t)$

During the T_{gap} interval, two processes occur simultaneously. The first one is the linear charge of capacitors C_{t1} and C_{t2} with the energy supplied by the input current source, which is much larger than the magnetizing current. After completion of T_{on} , capacitor C_{t1} is charged linearly (Figures 3 and 6) at a constant current $I_{L_{in}}$ following:

$$v_{C_{t1}}(t) = v_{C_{t1}}(T_{on}) + \frac{I_{L_{in}}}{C_{t1}}(t - T_{on}) \quad (17)$$

This linear charge continues until a complete period T of the converter is completed.

$$v_{C_{t1}}(T) = v_{C_{t1}}(T_{on}) + \frac{I_{Lin}}{C_{t1}} (2T_{gap} + T_{on}) \quad (18)$$

Calculation of φ

In steady state:

$$v_{C_{t1}}(T) = v_{C_{t1}}(0) \quad (19)$$

Considering Equations (8), (15), (16), and (18), from Equation (19), we obtain:

$$\tan(\varphi) = \frac{1}{\cos \varphi} \text{sen}(\omega_{T_{on}} T_{on} + \varphi) + \omega_{T_{on}} (2T_{gap} + T_{on}). \quad (20)$$

Since the mean value of $v_{C_{t1}}(t)$ in the interval T_{on} is V_o , as shown in Figure 6, and considering the symmetry of the waveform, it follows that:

$$v_{C_{t1}}(0) - V_o = V_o - v_{C_{t1}}(T_{on}) \quad (21)$$

Therefore, from Equations (15) and (16):

$$\text{sen}(\omega_{T_{on}} T_{on} + \varphi) = -\text{sen}(\varphi) \quad (22)$$

Substituting Equation (22) into Equation (20) and operating, we obtain:

$$\varphi = \arctan \left[\frac{\omega_{T_{on}} (2T_{gap} + T_{on})}{2} \right] \quad (23)$$

With this expression, the maximum current of the GaN HEMT can be determined from Equation (11). Substituting (23) into (13), we obtain:

$$\cos(\omega_{T_{on}} T_{on}) - \frac{\omega_{T_{on}} (2T_{gap} + T_{on})}{2} \sin(\omega_{T_{on}} T_{on}) = 1 \quad (24)$$

This transcendental equation will allow $\omega_{T_{on}}$ to be obtained from the values of T_{on} and T_{gap} . The fulfilment of Equations (19) and (21) implies that the mean value over a complete period of $V_{C_{t1}}$ is V_o . Since the voltage waveform in C_{t2} is identical to the voltage across C_{t1} , even though with a $T_{on} + T_{gap}$ delay time, the mean value of $V_{C_{t2}}$ is also V_o . Finally, since the mean value of V_{Lin} in Figure 2 is 0, $V_{in} = 2V_o$ if ideal components are considered.

Calculation of $i_{L_{mag}}(t)$

Now, the time evolution of the magnetizing current must be known to ensure that its stored energy is large enough to guarantee the zero-voltage switching (ZVS) condition. The other process that occurs in the T_{gap} time interval is the resonance between the magnetizing inductance of the transformer and the parasitic capacitances of the two transistors of the half bridge, C_{ds1} and C_{ds2} . During T_{gap} , the resonant current charges the parasitic capacitance of the GaN HEMT previously in conduction from 0 V to a level slightly greater than V_{in} . This current discharge the parasitic capacitance of the GaN HEMT previously off from almost V_{in} to 0 V. At this precise time, this last transistor is switched on, achieving a zero-voltage and zero-current commutation.

The differential equation that defines the time behaviour of the current through the magnetizing inductance can be obtained by a previous analysis of the equivalent circuit in Figure 8, where:

$$v_{C_{t1}}(t) = v_{L_{mag}}(t) + v_{C_{ds1}}(t) \quad (25)$$

$$v_{C_{t2}}(t) = -v_{L_{mag}}(t) + v_{C_{ds2}}(t) \quad (26)$$

Subtracting both equations, we obtain:

$$v_{C_{t1}}(t) - v_{C_{t2}}(t) = 2v_{L_{mag}}(t) + v_{C_{ds1}}(t) - v_{C_{ds2}}(t) \quad (27)$$

As the waveform of the voltage across C_{t2} is identical to the voltage across C_{t1} , although with a delay time $T_{on} + T_{gap}$, the difference between v_{ct1} and v_{ct2} in the T_{gap} time interval, as shown in Figure 3, takes a constant value equal to:

$$v_{C_{t1}}(t) - v_{C_{t2}}(t) = \frac{I_{Lin}}{C_{t1}} \cdot (T_{on} + T_{gap}) \quad (28)$$

Taking the derivative in Equation (27):

$$0 = 2L_{mag} \frac{d^2 i_{L_{mag}}(t)}{dt^2} + \frac{d v_{C_{ds1}}(t)}{dt} - \frac{d v_{C_{ds2}}(t)}{dt} \quad (29)$$

or employing the relation between voltage and current in the parasitic capacitances:

$$0 = 2L_{mag} \frac{d^2 i_{L_{mag}}(t)}{dt^2} + \frac{i_{C_{ds1}}(t)}{C_{ds1}} - \frac{i_{C_{ds2}}(t)}{C_{ds2}} \quad (30)$$

As $C_{ds} = C_{ds1} = C_{ds2}$ and according to the relationship between currents:

$$i_{C_{ds1}}(t) - i_{C_{ds2}}(t) = i_{L_{mag}}(t) \quad (31)$$

Finally, the differential equation that describes the evolution of the magnetizing current is:

$$\frac{d^2 i_{L_{mag}}(t)}{dt^2} + \frac{i_{L_{mag}}(t)}{2L_{mag}C_{ds}} = 0 \quad (32)$$

The solution to this differential equation is given by:

$$i_{L_{mag}}(t) = I_{L_{max}} \cos(\omega_{T_{gap}} t + \sigma) \quad (33)$$

where $\omega_{T_{gap}}$ is the resonant frequency during T_{gap} :

$$\omega_{T_{gap}} = \frac{1}{\sqrt{2L_{mag}C_{ds}}} \quad (34)$$

At the beginning of the GAP state, the magnetizing inductance, L_{mag} , will be fully charged. Since the average value of its intensity is zero and it is charged during T_{on} with a constant voltage of V_o , during T_{gap} it will maintain this intensity at its maximum point. Considering the symmetry of magnetizing current waveform (Figure 9) whose value is:

$$i_{L_{mag}}(0) = i_0 = \frac{V_o}{L_{mag}} \frac{T_{on}}{2} \quad (35)$$

The value of angle σ must fulfil $i_{L_{mag}}(0) = i_0$; therefore, from Equation (33):

$$I_{L_{max}} = \frac{i_0}{\cos(\sigma)} \quad (36)$$

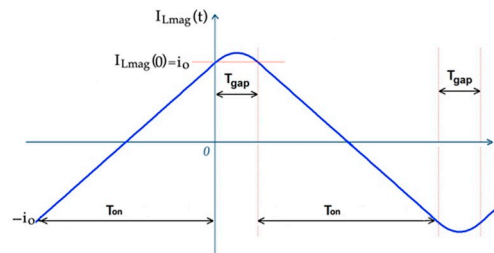


Figure 9. Evolution of $i_{L_{mag}}(t)$ during a switching period.

Substituting (36) into (33), we obtain:

$$i_{L_{mag}}(t) = \frac{i_0}{\cos(\sigma)} \cos(\omega_{T_{gap}} t + \sigma) \quad (37)$$

Calculation of σ

$V_{L_{mag}}(t)$ can be obtained from Equation (37) as:

$$v_{L_{mag}}(t) = -L_{mag} \frac{i_0}{\cos(\sigma)} \omega_{T_{gap}} \sin(\omega_{T_{gap}} t + \sigma) \quad (38)$$

Taking (38) for $t = 0$:

$$V_0 = -L_{mag} \frac{i_0}{\cos(\sigma)} \omega_{T_{gap}} \sin(\sigma) \quad (39)$$

Substituting i_0 from Equation (35) into (39), we obtain:

$$\sigma = \arctan \left[\frac{-2}{\omega_{T_{gap}} \cdot T_{on}} \right] \quad (40)$$

As a result of this study, the maximum value of the magnetizing current can be known.

3.1.3. Condition to Guarantee ZVS Condition Accomplishment

From Figure 2, as shown in the waveforms in Figure 3, the v_{ds2} voltage of GAN2 when GAN1 is conducting results from the addition of the voltages across the capacitors C_{t1} and C_{t2} . As the voltage across capacitor C_{t2} is identical to that across C_{t1} , although with a delay time $T_{on} + T_{gap}$, we obtain:

$$v_{ds2}(t) = 2V_o + L_{lk} \frac{I_{L_{in}}}{\cos \varphi} \omega_{T_{on}} [\sin(\omega_{T_{on}} t + \varphi) - \sin(\varphi)] + \frac{I_{L_{in}}}{C_{t1}} (t + T_{gap}) \quad (41)$$

From Equation (41), for $t = 0$:

$$v_{ds}(\text{charge}) = 2V_o + \frac{I_{L_{in}}}{C_{t1}} T_{gap} \quad (42)$$

and for $t = T_{on}$, considering Equation (22):

$$v_{ds}(\text{discharge}) = 2V_o - \frac{I_{L_{in}}}{C_{t1}} T_{gap} \quad (43)$$

Magnetizing current is responsible for charging/discharging the drain to source capacitances. Therefore, the contribution of the magnetizing current during T_{gap} must be large enough to charge C_{ds1} from 0 V to $v_{ds}(\text{charge})$ and discharge C_{ds2} from $v_{ds}(\text{discharge})$ to 0 V:

$$\begin{aligned}\Delta Q &= \int_0^{T_{\text{gap}}} i_{L_{\text{mag}}}(t) dt = \int_0^{T_{\text{gap}}} i_{C_{\text{ds}1}}(t) dt - \int_0^{T_{\text{gap}}} i_{C_{\text{ds}2}}(t) dt = \\ &= C_{\text{ds}1} \cdot v_{\text{ds}}(\text{charge}) + C_{\text{ds}2} \cdot v_{\text{ds}}(\text{discharge}) = C_{\text{ds}} \cdot 4V_0\end{aligned}\quad (44)$$

The condition to guarantee the zero-voltage commutation of the transistors is obtained by integration with Equation (37):

$$4V_0 = \frac{1}{C_{\text{ds}} \cdot \omega_{T_{\text{gap}}}} \frac{i_0}{\cos(\sigma)} \left(\sin(\omega_{T_{\text{gap}}} T_{\text{gap}} + \sigma) - \sin(\sigma) \right) \quad (45)$$

4. Design Procedure

Firstly, the following converter specifications must be known: input and output voltages (to determine the transformer turns ratio), output power (to determine the input current assuming a typical efficiency of 95% for these type of converters), and switching frequency. With this information, the switches to be employed can be selected and their parasitic capacitances can be determined. In a first iteration of the design procedure, the duration of the on state, T_{on} , is chosen so that $2T_{\text{on}}/T$ is in the order of 70% of the switching period. This also determines the duration of the gap state T_{gap} .

As explained above, during the gap state, the charging and discharging occur of the drain to source capacitances of the half-bridge switches from the stored energy in the magnetizing inductance at the end of the ON state. The initial value of this magnetizing current is i_0 . The iterative design procedure continues selecting an initial value of i_0 , which at least permits the charging/discharging of the C_{ds} capacitances for T_{gap} , assuming a constant current process and a final value of $2V_0$, that is:

$$i_0 = \frac{2 \cdot C_{\text{ds}}}{T_{\text{gap}}} \cdot 2V_0 \quad (46)$$

Then, from (35), the magnetizing inductance that provides i_0 at time T_{on} is:

$$L_{\text{mag}} = \frac{V_0}{2i_0} \cdot T_{\text{on}} \quad (47)$$

The value of L_{mag} can be adjusted using an air gap in the implemented transformer. Now, the resonance frequency during the gap state $\omega_{T_{\text{gap}}}$ can be known from Equation (34) and the value of σ angle, from Equation (40). The maximum value of the magnetizing current $i_{L_{\text{max}}}$ can be calculated from Equation (36).

After, a numerical solution for the exact value of the duration of the gap state to guarantee the ZVS condition can be obtained from Equation (45). Once the value of T_{gap} is obtained, as the period has a fixed value, the value of T_{on} must be recalculated. If necessary, a new iteration is performed with these new values of T_{on} and T_{gap} .

As T_{on} is already known, the value of the resonance frequency during the on state, $\omega_{T_{\text{on}}}$, can be determined using numerical calculation of Equation (24).

Next, the leakage inductance of the implemented transformer, L_{lk} , is experimentally measured. The required values of the resonant capacitances C_t are obtained from Equation (8). Then, we calculate the φ angle from Equation (23) to finally obtain the maximum value of the primary current I_{max} from Equation (11). This value of I_{max} should be much greater than i_0 . The flowchart in Figure 10 summarizes the design procedure.

Reverse Conduction Control of the Synchronous Rectifier Transistors

Reverse conduction of the GaN HEMT used as synchronous rectifier transistors, during the on states, is due to the generation of a conduction channel by applying a positive voltage V_{gs} only during these states.

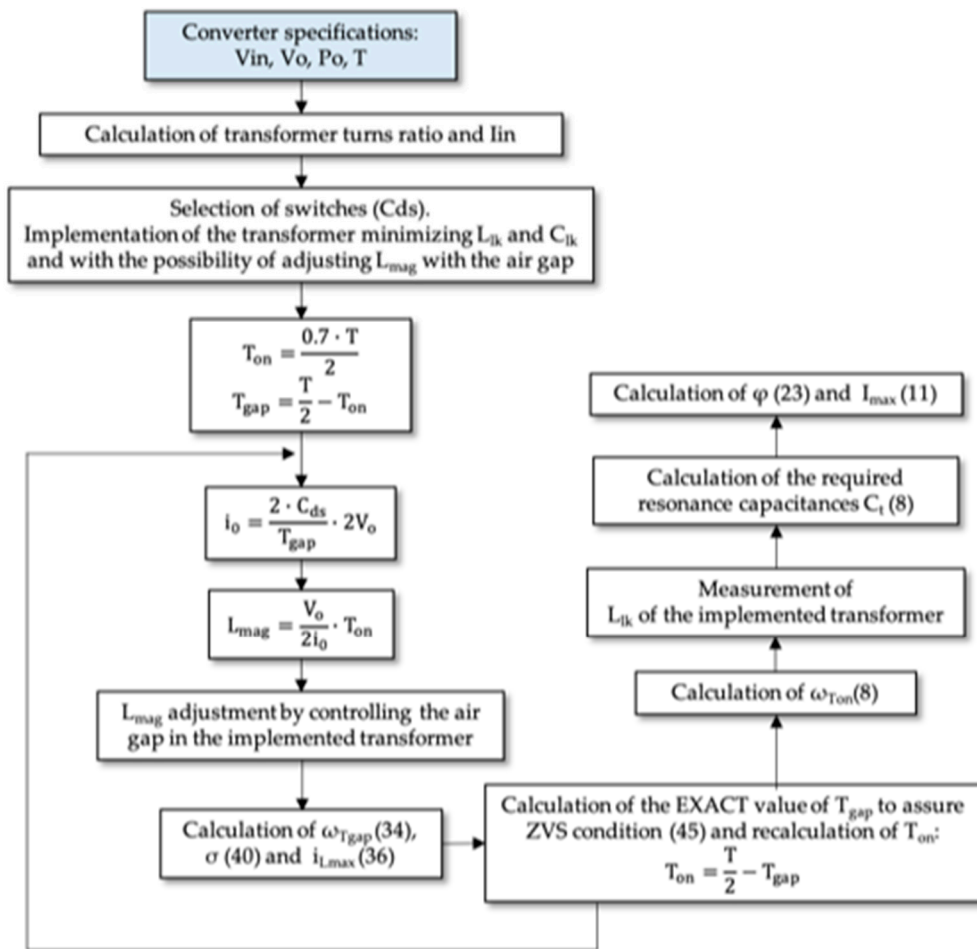


Figure 10. Design flowchart.

As previously mentioned, the transistors of the synchronous rectification stage must be in the off state during the T_{gap} time interval. A voltage $V_{gs} = 0$ V can be applied to ensure this condition. However, the GaN HEMT transistor could begin to drive in the reverse direction if the gate is directly connected to the source (Figure 11a) and the source to drain voltage ($V_{sd} = V_{gd}$) increases and reaches the threshold value for the generation of the conduction channel. This situation can occur if the secondary voltage reaches the voltage across C_{out} plus this threshold voltage. This conduction interval would provide a method for the discharge of the magnetizing inductance; therefore, the loading and unloading processes of the parasitic capacitances of the half-bridge and synchronous rectifier transistors would not be completed, as shown in Figure 12. Consequently, the V_{ds} voltage of the transistors to be connected would not be 0 V at the switching time. This would slightly increase the losses in the converter.

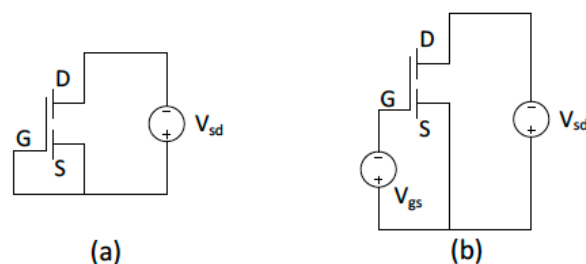


Figure 11. Two different GaN HEMT bias for the gap state of the synchronous rectifier transistors. (a) $V_{GS} = 0$ V and (b) $V_{GS} < 0$ V.

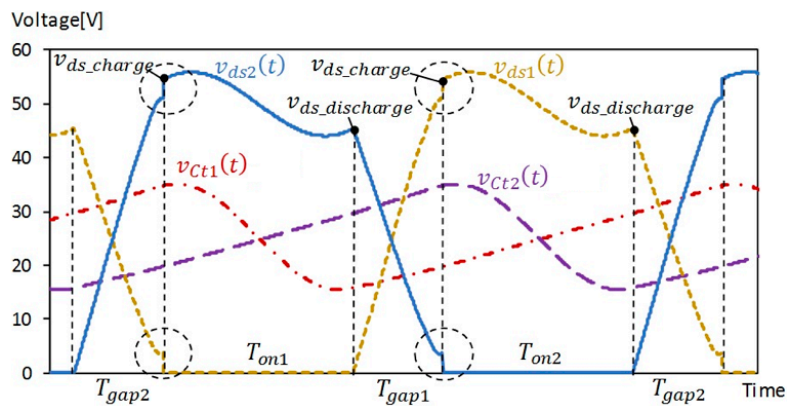


Figure 12. Effect of the undesired reverse conduction of the synchronous rectifier transistors at the end of the gap state (inside the circles).

This undesired reverse conduction can be prevented by employing a negative polarization voltage V_{gs} (Figure 11b). As $V_{gd} = V_{gs} + V_{sd}$ is fulfilled, under the same value of voltage V_{sd} , the voltage V_{gd} is prevented from reaching its threshold value for entering conduction. As the primary voltage at the end of the gap interval of GAN2 is determined by Equation (15), the required value of V_{gs} is obtained from:

$$v_{\text{prim}} = L_{lk} I_{L_{in}} \omega_{T_{on}} \tan \varphi + V_o \leq V_o + n \cdot (V_{gd(\text{threshold})} - V_{gs}), \quad (48)$$

$$\text{with } n = \frac{\text{number of primary turns}}{\text{number of secondary turns}} \quad (49)$$

Solving for V_{gs} :

$$V_{gs} \leq V_{gd(\text{threshold})} - \frac{L_{lk} I_{L_{in}} \omega_{T_{on}} \tan \varphi}{n} \quad (50)$$

Figure 12 shows the effect of the undesired reverse conduction of the synchronous rectifier transistors at the end of the gap state, defaulting the ZVS condition.

5. Experimental Design

A breadboard was implemented, working at a switching frequency of 1 MHz, input voltage of 50 V, output voltage of 6 V, and output power of 150 W. The transformer turns ratio, n (50), was four with an output current of 25 A. Following the design procedure, the on time was initially fixed to 350 ns and the gap time to 150 ns. To validate the benefits of using GaN HEMTs up to 1 MHz, we implemented another breadboard using a silicon MOSFET working at 100 kHz.

5.1. Selection of the Switches

Equation (11) provides the maximum value of the current through the half-bridge transistors. The maximum value of the current through the synchronous rectifier transistors was obtained multiplying the previous one by the transformer turns ratio and considering the two paralleled transistors.

The maximum operating voltage across the half-bridge transistors is slightly greater than the input voltage due to the resonance in the tuning capacitors. European Space Agency (ESA) requirements [20] establish that the transistor voltage in normal operation should not exceed 80% of the maximum voltage supported by the transistor. Transistors with a maximum voltage of 80 V were selected because the 60 V transistors do not meet the ESA requirements and the 100 V one is oversized.

For the selection of the synchronous rectifier transistors, we must consider that:

$$V_{\text{max_sec}} = V_{C_{out}} + V_{\text{sec_trafo}} = 6 + 6 = 12 \text{ V} \quad (51)$$

Considering again the ESA requirements, transistors with a maximum voltage of 30 V were found to be suitable for the rectification stage. Table 2 shows the requirements and the selection of the different transistors.

Table 2. Requirements and characteristics of the selected transistors.

Device	Requirements V_{\max}/I_{\max}	Static Characteristics	
		$R_{DS(ON)}$	$V_{DS\max}/I_{D\max}$
Half bridge transistors: EPC2021 [21]	>62.5 V/14 A	2.5 m Ω	80 V/90 A
Synchronous rectifier transistors EPC2023 [21]	>15 V/28 A	m Ω	30 V/90 A

5.2. Transformer Design

Once the transformer turns ratio is known, the transformer design can be initiated, prioritizing the minimization of the values of L_{lk} and C_{lk} . To do this, the transformer was implemented using a planar ferrite core type E 32/6/20-3F4 and several 100 μm thick copper sheets to complete the required four turns on the primary side and one turn on each one of the secondary outputs. In order to achieve those goals, Ferroxcube's 3F4 Magnesium-Zinc ferrite was selected, as it has a relative permeability of 1000 was chosen, as it exhibits low loss in the 1–2 MHz range. The magnetizing inductance can be adjusted by means of the air gap. Figure 13 depicts the two planar transformers built for the 100 kHz and 1 MHz prototypes.

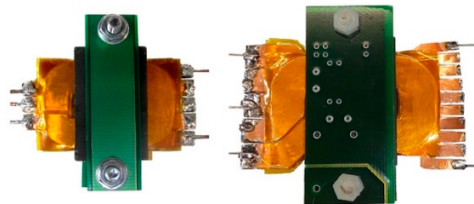


Figure 13. Transformers size comparison. (left) 1 MHz planar transformer (E 32/6/20-3F4) and (right) 100 kHz planar transformer (E38/8/25-3F3).

5.3. Calculation of C_{tuning}

As the transformer leakage inductance L_{lk} was 37 nH and the measured value of the printed circuit parasitic inductances was 52 nH, the resonant inductance was 89 nH. From Equation (8), the required tuning capacitance C_{tuning} was 100 nF. X7R ceramic capacitors were employed for its implementation.

5.4. Calculation of C_{output}

Several aspects must be considered to choose a proper output capacitance value. Firstly, the primary reflected value of the output capacitor must be much greater than the tuning capacitor C_t , following Equations (52) and (53):

$$\frac{1}{C_t} + \frac{n^2}{C_{\text{out}}} \approx \frac{1}{C_t} \quad (52)$$

$$\frac{C_{\text{out}}}{n^2} \gg C_t \quad (53)$$

The output capacitor must be selected to limit the peak-to-peak output voltage ripple to a reasonable value. The output voltage ripple is given by:

$$\Delta v_{\text{out}} = \Delta v_{C_{\text{out}}} + \Delta v_{\text{ESR}} \quad (54)$$

where $\Delta v_{C_{out}}$ is the capacitive voltage ripple:

$$\Delta v_{C_{out}} = \frac{n I_{Lin} \left(T - \frac{2\pi}{\omega_{Ton}} \right)}{C_{out}} \quad (55)$$

and Δv_{ESR} is the resistive voltage ripple due to the series equivalent resistance (ESR):

$$\Delta v_{ESR} = ESR \cdot n \cdot I_{Lin} \cdot \left(1 + \frac{1}{\cos(\varphi)} \right) \quad (56)$$

Power losses in the output capacitor depend on the root mean square value of the current across this component and its parasitic resistance:

$$P_{ESR} = ESR \cdot I_{C_{out_RMS}}^2 \quad (57)$$

with:

$$I_{C_{out_RMS}}^2 = \frac{n^2 I_{Lin}^2}{T_{on} + T_{gap}} \left[T_{on} \left(1 + \frac{1}{2 \cos^2(\varphi)} \right) + \frac{3}{\omega_{Ton}} \tan(\varphi) \right] - 4n^2 I_{Lin}^2 \quad (58)$$

An output capacitance of 220 μF was implemented by connecting ten 22 μF capacitors in parallel to reduce the parasitic resistance to an approximate value of 5 m Ω . As such, output voltage ripple was about 300 mV and the power losses in the capacitor were nearly 2.3 W in worst-case conditions.

5.5. Implemented Prototype

Figure 14 shows a picture of the prototype built in a four-layer printed circuit board. The isolation transformer was placed on the bottom face of the board.

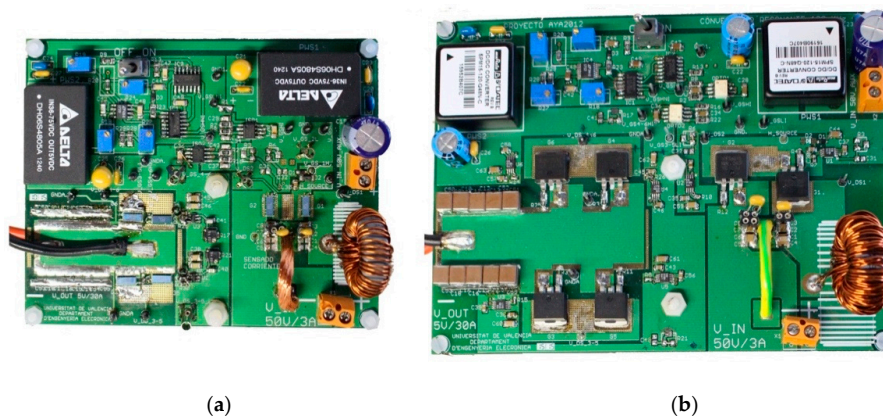


Figure 14. Implemented prototype of the IBC with (a) GaN HEMTs and (b) silicon MOSFETS.

To ensure the cut-off of the synchronous rectifier transistors during the T_{gap} time interval, a series connection of a diode and a small inductance was placed in the off path of the gate drive circuit (Figure 15). This configuration provides a negative biasing of the gate with respect to the source during T_{gap} without needing an auxiliary negative voltage source, as is shown in the oscillogram of Figure 16.

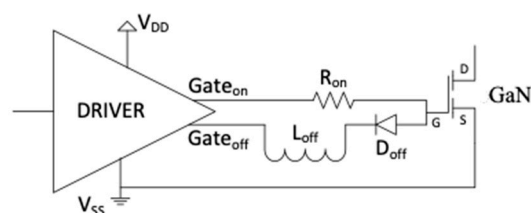


Figure 15. Drive circuit solution to provide negative voltage during the gap time.

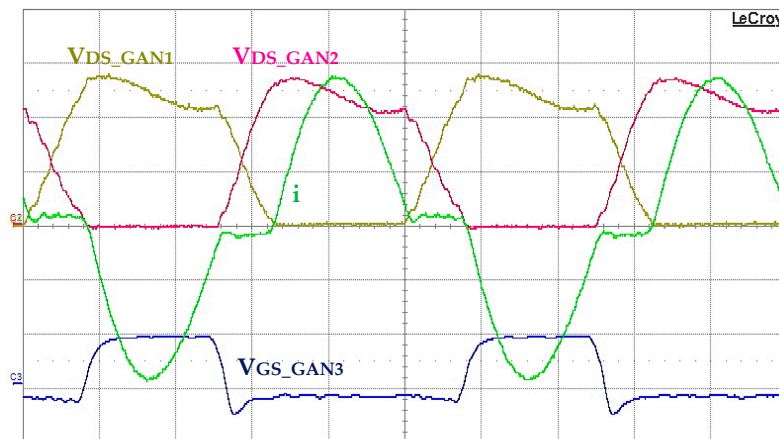


Figure 16. Experimental main waveforms of the IBC working at 1 MHz. i is the primary current (5 A/div), V_{ds_GAN1} is the drain to source of GAN1 (20 V/div), V_{ds_GAN2} is the drain to source of GAN2 (20 V/div) and V_{gs_GAN3} is the gate to source of GAN3 working as synchronous rectifier (5 V/div). Time base: 200 ns/div.

6. Experimental Results

In the previous theoretical analysis, the only parasitic capacitances considered charged/discharged during the gap state were those of the half-bridge transistors. However, other smaller parasitic capacitances are charged/discharged, whose values were previously neglected. These parasitic capacitances correspond to the transformer, to the synchronous rectifier transistors, and to the printed circuit board. Therefore, converter start-up requires fine adjustment of the transformer magnetizing inductance by slightly varying its air gap. Due to this adjustment, the switching on of the transistors was conducted at 0 V.

Figure 16 shows the 1 MHz experimental waveforms of the converter working at maximum output power (150 W). Both the drain-to-source voltage of the half-bridge transistors and the primary current were as expected for a ZVZCS resonant converter.

The measured efficiency of the converter is shown in Figure 17. The obtained results for the 1 MHz GaN HEMT converter were compared with the achieved with another prototype working at 100 kHz and implemented using silicon MOSFET transistors. The experimental efficiencies of both prototypes were very similar.

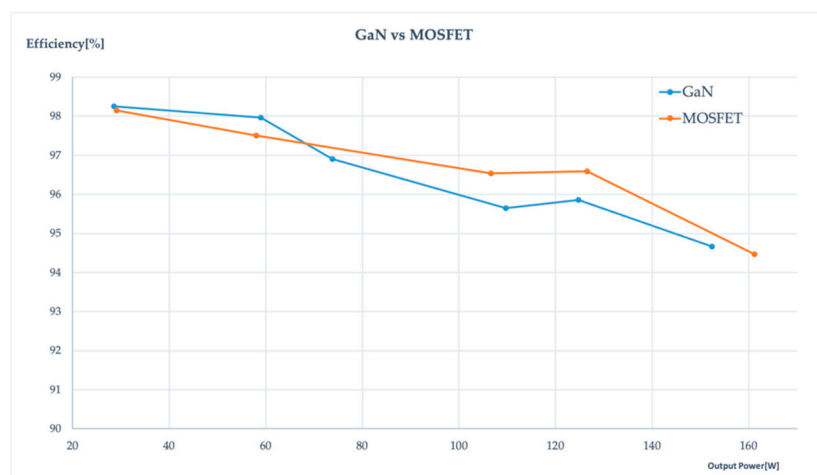


Figure 17. Evolution of the efficiency with the output power for the same topology but implemented with two different semiconductor technologies.

Finally, Table 3 compares the weight, volume, and power density between these two prototypes. Power density was improved with the GaN HEMT converter, although this characteristic was not optimized in this initial prototyping stage that represent a proof of concept.

Table 3. Volume, weight and power density of the two implemented prototypes.

Prototype	Volume (cm ³)	Weight (g)	Power (W)	W/cm ³	W/g
GaN HEMT	486.4	200	150	0.31	0.75
Silicon MOSFET	883.3	275	150	0.17	0.54

7. Conclusions

In this study, we propose the use of GaN HEMTs in a real DC/DC converter for a space power application. An intermediate bus converter based on an GaN HEMTs half-bridge ZVZCS resonant converter working at 1 MHz was designed and implemented. The experimental results and performance were compared with the same converter using silicon MOSFET transistors and working at 100 kHz. The experimental obtained confirmed the potential of GaN HEMTs to be used in power DC/DC converters for space applications, improving the power density while maintaining a similar efficiency. It should be noted that without having been able to have a magnetic material with lower losses for the megahertz range, the power density has been increased by 82%, maintaining the same efficiency as for the 100 kHz version. The efficiency is maintained, even though the frequency has increased around ten times, which is due to the excellent switching and conduction characteristics of the GaN HEMTs—among others, the small gate capacitance and the lower channel resistance in conduction should be pointed out. An optimized design procedure has been proposed to guaranty the zero-voltage switching condition, enabling an increase in the power density without a penalization of the efficiency.

In conclusion, the advantages provided by the proposed GaN HEMTs indicate that they will be able to replace the conventional silicon transistors in aerospace applications, considering their inherent radiation tolerance and small size, providing higher efficiency and smaller total size at the system level.

Author Contributions: E.M. and J.L.L. conceived the idea and designed the experiment; E.M. and J.B.E. guided the experiment and wrote the manuscript; J.L.L. and A.F. designed and built the magnetic devices; J.B.E., J.M.B., and A.G. conceived the procedure optimized design; E.S.-K. helped with data analysis and the setup design. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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