# Multi-pulse Characterization of Trapping/Detrapping Mechanisms in AlGaN/GaN High Electromobility Transistors

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## Abstract

GaN high-electro mobility transistors (HEMTs) are among the most promising candidates for use in high-power, high-frequency, and high-temperature electronics owing to their high electrical breakdown threshold and their high saturation electron velocity. The applications of these AlGaN/GaN HEMTs in power converters are limited by the surface trapping effects of drain-current collapse. Charge-trapping mechanisms affect the dynamic performance of all GaN HEMTs used in power switching applications. This study analyzes the dynamic resistance of GaN HEMTs and finds that the effects of dynamic resistance can be suppressed by controlling switching conditions and on-off cycles.

Keywords: Semiconductor device reliability, GaN HEMTs, dynamic on-resistance

## 1. Introduction

Wide-bandgap (WBG) power semiconductors have been researched intensively in recent years because of their theoretically promising advantages. WBG semiconductors can withstand high voltages per unit area. However, the wide bandgap is also related to a reduction of the channel width, which reduces the drain-source on-state device resistance ($R_{DS(ON)}$), so these semiconductors can be used to produce devices that can withstand higher voltages with lower $R_{DS(ON)}$. In addition, the higher electron saturation velocity of these materials increases the maximum switching frequency, which allows higher system frequencies with lower losses and reduces the size of the reactive components in the power converter. The other great advantage of these semiconductors is their potential for operating at higher temperatures owing to the low intrinsic carrier concentration, which could make them suitable for use in harsh environmental conditions [1-3].

Nowadays, the main two WBG semiconductors that have been used to replace Si are GaN and SiC. SiC devices have proven even more reliable than Si devices [4-5]. The reliability of GaN transistors, however, has not yet been fully clarified. GaN devices have developed more slowly because of the need for lateral structures. Lateral structures like the HEMT transistor use heterostructures to form a two-dimensional electron gas (2DEG), which yields a faster device with lower on-resistance. However, these structures are difficult to manufacture owing to the likelihood of mismatched lattices in the junction between the different materials forming the heterostructure. If the lattices are not matched, electrons can become trapped, a phenomenon known as dynamic resistance or current collapse. This trapping reduces the current that the devices can drive below the device's rated current.

Many studies in the literature have examined trapping in GaN HEMTs. In references [6, 7] the three dominant mechanisms of trapping are explained; two are caused by bias conditions, one on the drain and the other on the gate. The third relevant mechanism is hot electron trapping, which arises

in the semi-on condition during switching events. References [8, 9] consider the temperature of the material under different stresses and conditions, with various current during the test, off-state stress time, frequency, and gate voltage. Other reports have focused on hot electron trapping, which occurs during switching events [10-12].

The present study addresses the dynamic resistance of commercial GaN HEMTs, using soft and hard switching conditions to identify novel detrapping mechanisms during the off-state when subjected to voltage bias stress. Designers need to understand this mechanism because it shows that dynamic resistance can be eliminated by using techniques such as soft switching and controlled frequency conditions.

## 2. Experimental methods

We tested commercially available normally-off HEMTs made from AlGaN/GaN on Si substrate, rated at 600 V. Two different devices were selected so we could compare two different structures. We chose the Panasonic hybrid-drain-embedded gate injection transistor (HD-GIT) structure, which is supposed to prevent current collapse [13], and the second is the GaN Metal-Insulator-Semiconductor HEMT (MISHEMT) manufactured by GaN Systems Inc. Table 1 summarizes the key parameters of the devices.

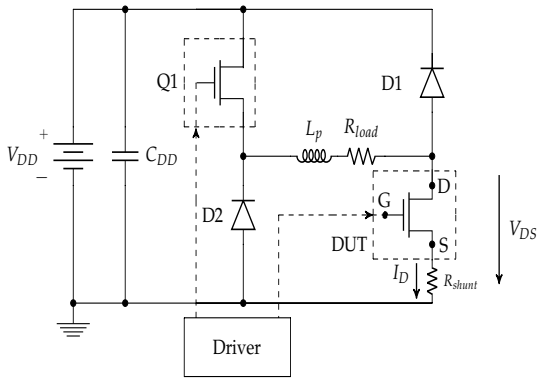
**Table 1 Parameters of the investigated GaN HEMTs.**

| | Symbol | GaN MIS-HEMT GS66508P | p-GaN HEMT PGA26E07BA |
|---|---|---|---|
| **Drain-to-source breakdown voltage** | $BV_{DSS}$ | 650 V | 600 V |
| **Continuous drain current (Tc=25ºC)** | $I_D$ | 30 A | 26 A |
| **Drain-to-source ON resistance (Tj = 25 ºC)** | $R_{DS(ON)}$ | 50 mΩ[a] | 56 mΩ[b] |
| **Input Capacitance (1 MHz, 400 V)** | $C_{iss}$ | 168 pF | 405 pF |
| **Total Gate Charge** | $Q_G$ | 5.8 nC | 5 nC |

(a) Measured at 9 A, (b) Measured at 8 A

For the measurement of dynamic resistance, we implemented a setup designed specially to fully control the time at which voltage stress is applied to the device under testing (DUT). This setup also allows us to reproduce soft switching conditions, as will be shown later. Fig. 1 shows the circuit schematic based on the same asymmetric half-bridge configuration as the one used in [14] and the hardware setup for testing. For the top transistor (Q1) a SiC MOSFET was used in to give a low output capacitance; this feature limits the amplitude of current peaks following the charge and discharge of the parasitic output capacitance of the transistor. For electrical measurements, we used a shunt resistor of 98 mΩ (SDN-414-10) to measure the current and the voltage was measured with a passive voltage probe (PP018 300 V and 500 MHz from Lecroy).

Owing to the high voltage applied to the DUT, the voltage across the device has a large dynamic range that can overload the oscilloscope input amplifier, so the on-state voltage cannot be determined accurately. To avoid this problem, a voltage clamp circuit was used together with a passive voltage probe. The commercial clp1500V15A1 voltage clamp from Springburo GmbH was used. The low range (2 V) was selected in the voltage clipper to give a fast response of 100 ns, which is affected by the passive voltage probe and the voltage clipper. Precise frequency-response compensation was applied in the passive voltage probe to compensate for the whole measurement chain of the clipper and voltage probe. To control the DUT on-time, the generic SI8271BB isolated MOSFET driver from Silicon Labs was used.

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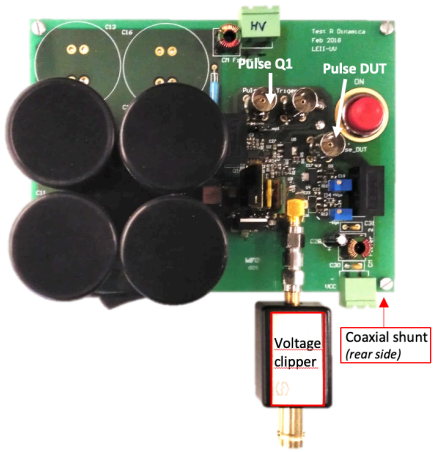



**(b)**

**Figure 1 (a) Circuit diagram for dynamic resistance measurements (b) Test set-up**

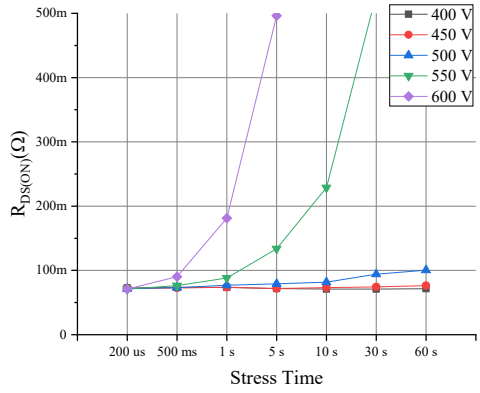
## 3. Experimental Results

To evaluate the different mechanisms that induce an increase of the dynamic resistance, various measurements were taken. First, the off-state voltage stress was evaluated with single-pulse measurements; then multiple-pulse

measurements were taken to evaluate electron trapping during switching events.

### *3.1 Single-pulse measurements*

The single-pulse measurements require varying the off-state time with a constant on-time of 10 $\mu$s with $V_{GS}$ = 4 V. The gate voltage is used to indicate any change in the dynamic resistance due to the behavior of traps that act like virtual gates [15]. When using a higher gate voltage, higher currents need to be used to see the influence of traps on dynamic resistance. Instead, we have chosen a lower gate voltage that allows us to see the effects of dynamic resistance with lower currents, which minimizes self-heating in the devices. The results for the GaN MISHEMT and p-GaN HEMT are shown in Fig. 2. The plotted value is an average of the recorded measurements between 1 $\mu$s and 9 $\mu$s, and we performed this test for $V_{DS}$ ranging from 400 V to 600 V.

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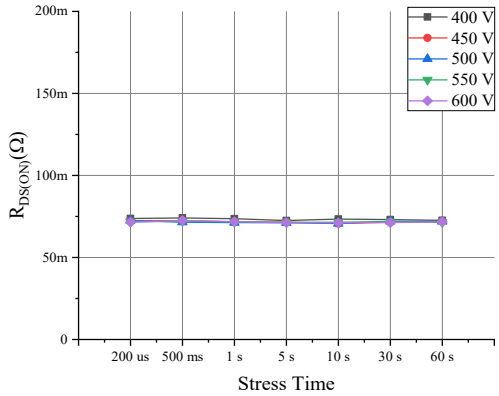


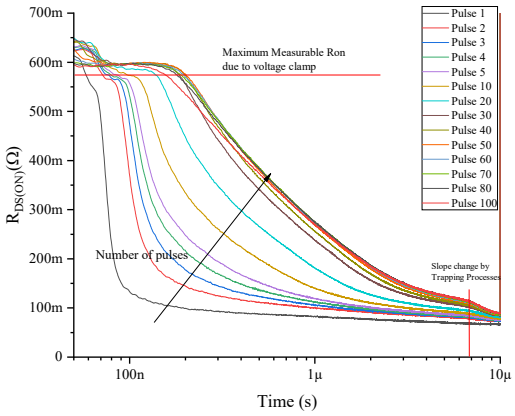

**(b)**

**Figure 2 Single-pulse measurements of dynamic resistance with varying off time for different applied $V_{DS}$ and 10 $\mu$s on-time for a) GaN MISHEMT and b) p-GaN HEMT.**

In Fig. 2a), one can observe an increase of dynamic resistance in the GaN MISHEMT device as both the voltage and stress time increase. However, the stress time starts to have more of an effect once it exceeds 500 ms. Therefore, the dynamic resistance stays nearly constant for times less than 500 ms for all the drain voltages applied, which will be irrelevant in most applications. Meanwhile, the p-GaN HEMT did not show any increase in resistance for all the times and voltages we applied. Based on these results, we can confirm that the GIT structure with a p-doped region near the drain effectively releases trapped charges. In contrast, off-state voltage stress trapping clearly affects the GaN MISHEMT devices. This trapping originates in the increased injection of electrons from the gate-drain access regions, owing to the high negative gate-drain voltage, and/or from substrate injection into the buffer due to the flow of drain-bulk vertical current [6].

### *3.2 Multiple-pulse measurements*

The results in Fig. 2 show how the drain voltage stress influences dynamic resistance. One of the structures has high dynamic resistance, but the times required to see any change in dynamic resistance are so long that this observation will not be practical for most applications. The next tests used multiple-pulse measurements, which are necessary in GaN HEMT devices because the semi-on state caused by the combination of high drain voltage ($V_{DS}$) and high drain current ($I_{DS}$) during switching events can greatly increase the dynamic resistance due to the injection of hot electrons from the channel into the buffer or gate-drain surface [6]. To evaluate this increase in dynamic resistance, a test sequence of 100 pulses with 200 $\mu$s off and 10 $\mu$s on was performed. The results are shown in Fig. 3 for GaN MISHEMT and p-GaN HEMT. Note that the results of these multiple-pulse tests and the single-pulse test cannot be compared because the mechanisms of trapping are different so the dynamic resistance behavior will be also different.

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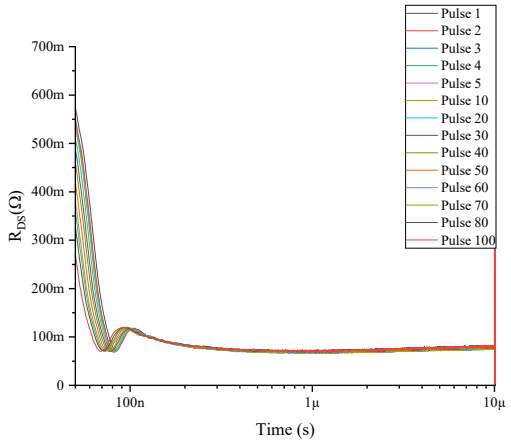



**(b)**

**Figure 3 Dynamic resistance measurements applying 100 pulses with 200 µs off and 10 µs on with $V_{DS}$ = 550 V for a) GaN MISHEMT and b) p-GaN HEMT.**

As is shown in Fig. 3a), the dynamic resistance increases with the number of pulses as it stabilizes beyond a certain number of pulses, around 30 pulses in the case of GaN MISHEMT. Two features of these results call for analysis. First is the increase in dynamic resistance, which cannot be due to the applied drain voltage stress since we have shown that the applied voltage stress is irrelevant for times lower than 500 ms in this DUT. Therefore, the increase must be related to hot electron trapping as mentioned in [11]. Second, we need to understand the stabilization of dynamic resistance. This stabilization is due to the accumulation of trapped charges that are de-trapped during the on-state. When the hot electron trapping is balanced by this de-trapping during the on-state, the device reaches a steady-state dynamic resistance. Despite the increase of resistance between pulses, the resistance is decreasing during the on-state of each pulse. This is a common behavior in GaN HEMTs. During the on-time the barrier energy level of the traps is lower, so that traps can be recombined and flow through the channel, reducing the resistance. The change in the slope of the dynamic resistance is marked with a red line in Fig. 3. The rate of this decrease during the on-state depends on the different activation energies of the traps, which mostly depends on the location of the traps [7, 16]. The constant values over 575 mΩ at the start of each pulse are false values that are introduced by the voltage clipper that clamps the voltage to 1.6 V. The current through the DUT in that case is 2.75 A, as it is forced by the 550 V applied over the fixed on-state resistance of 200 Ω.

Meanwhile, in the single-pulse measurements of p-GaN HEMTs, the dynamic resistance does not increase along with the number of pulses, as shown in Fig 3b). This behavior confirms the benefit of the GIT structure, in which the p-doped region near the drain introduces holes to that region that effectively release the trapped electrons [17]. Because dynamic resistance does not arise in multiple or single pulses in the p-GaN HEMT, the rest of the tests only evaluated in GaN MISHEMT devices.

The increase in dynamic resistance in the GaN MISHEMT is based on hot electron trapping during switching events. To test this hypothesis, we also tested the MISHEMT devices under soft switching conditions. These conditions are achieved with the gate pulses plotted in Fig. 4. With this pulse configuration, we have zero voltage switching (ZVS) in the turn-on transition and zero current switching (ZCS) in the turn-off transition.

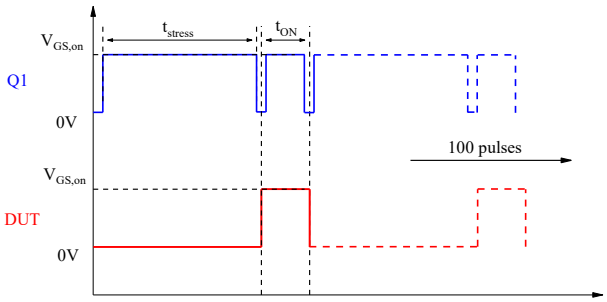



**Figure 4 Gate pulse configuration for soft switching conditions.**

The test was repeated for all the drain voltages and switching times that were tested in the hard switching tests, but now with soft switching transitions in both on and off-states. The dynamic resistance was measured using a pulse with on-state of 10 $\mu$s and off-stress time of 200 $\mu$s, taking the average value between 1 $\mu$s and 9 $\mu$s. The results are shown in Fig. 5, and demonstrate ~~the~~ that dynamic resistance does not occur with soft switching transients. Also, we find that using soft switching in only one of the switching transitions gives no increase in the dynamic resistance independently of the drain voltage applied. This demonstrates that trapped charges must accumulate in hard switching events to induce a measurable increase in the dynamic resistance. Therefore, a hard turn-off transition would need to be followed by a hard turn-on to induce a measurable increase in dynamic resistance. Otherwise, the dynamic resistance will not increase, as shown in Fig. 5. Perhaps charges trapped by hot electrons during one switching event are de-trapped during the on-state, and not enough remain to increase the dynamic resistance if one of the switching transitions is soft. Moreover, when using hard switching with drain-source voltages lower than 300 V, soft or hard switching conditions yield the same behavior.

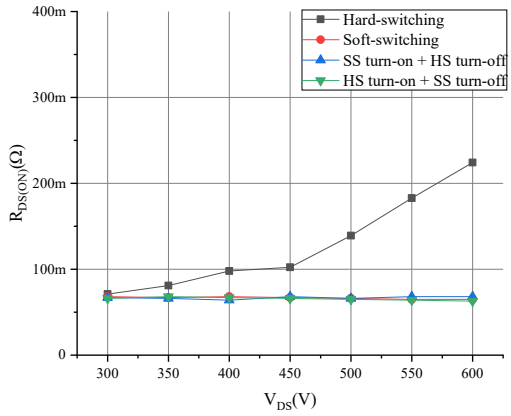



**Figure 5 Comparison of hard and soft switching measurements varying drain voltage applied in GaN MISHEMT with 100 pulses of 200 $\mu$s off-state and 10 $\mu$s on-state. Measuring resistance at pulse 100.**

When the device is in the semi-on state with high voltage and high current stress applied simultaneously, gate injection trapping occurs and the electrons in the 2DEG are accelerated by the field and injected into the AlGaN barrier defects or the buffer near the channel [6].

These measurements give evidence for two different trapping mechanisms. One is induced by the voltage stress applied during the off state and begins to have relevant effects with off-state times higher than 500 ms. The second trapping mechanism is hot electron trapping during the switching events if hard switching is used. Aiming to evaluate how the off-time affects hot electron trapping, we have performed more tests with multiple pulses varying the off-time but keeping the on-time of the DUT constant at 10 $\mu$s, recording the average value of $R_{DS(ON)}$ between 1 $\mu$s and 9 $\mu$s. The amount of charges removed during the on-time must be kept constant so we can observe the effects of the off-time. The results are shown in Fig. 6.

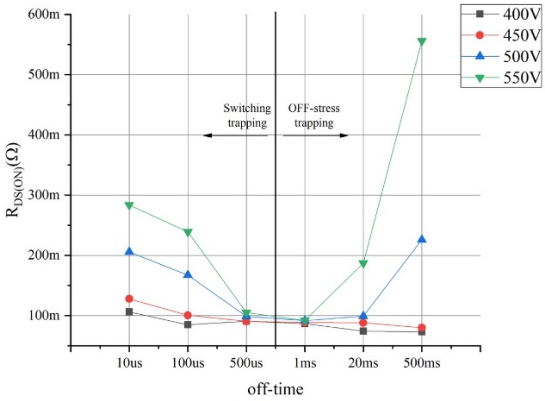
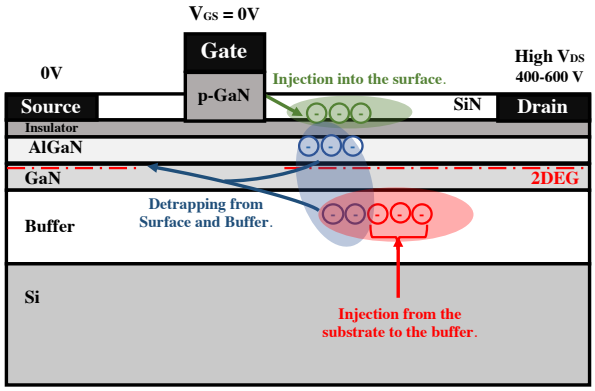



**Figure 6 Dynamic resistance measurements over 100 pulses with hard switching varying the off-state time and stress voltage with constant on-time of 10 $\mu$s.**

For the results shown in Fig. 6, the number of pulses was kept constant (100 pulses) for all test conditions, so the hot electron trapping is the same in all cases. Therefore, the resistance should be constant or even increasing during the off-times owing to the accumulation of traps caused by hot electrons and voltage stress. However, the resistance decreases between 10 $\mu$s and 1 ms, and this reduction can only be explained by de-trapping during the off-state driven by hot electrons during the switching events. In addition, for off-times greater than 1 ms, the resistance increases because with this longer off-time, trapping due to the applied voltage stress becomes relevant.

Therefore, when multiple pulses are applied, voltage-stress trapping coexists with de-trapping from the hot-electron traps. These phenomena are in opposition. The first is a reduction of dynamic resistance due to de-trapping of electrons that are injected into the AlGaN barrier or buffer near the channel during the semi-on state. The second is trapping by the injection of electrons from the gate-drain access regions or the substrate into the buffer due to the high applied drain voltage. These mechanisms are illustrated in Fig. 7a, and the opposing mechanisms explain the results in Fig. 6. When off-state stress trapping is negligible (for off-state times lower than 1 ms), de-trapping of the hot-electron traps drives the reduction in dynamic resistance. When the off-state stress is relevant (off-state times higher than 1 ms), the reduction of the dynamic resistance due to the de-trapping of switching-induced traps is negligible, so the dynamic resistance is increased by the high drain voltage stress. Therefore, the on-resistance increases as the off-time increases.

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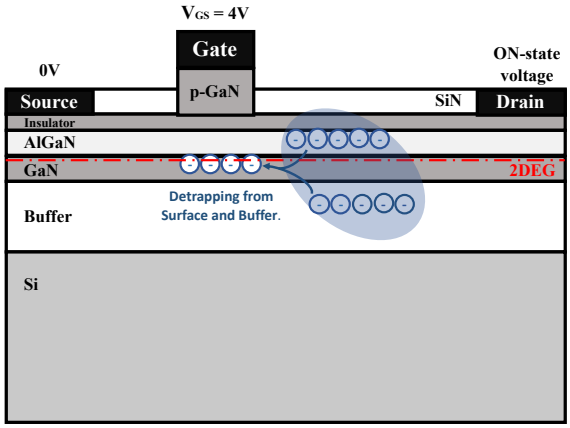


**(b)**

**Figure 7 Schematic of lateral GaN MISHEMT structure to illustrate the trapping effects a) during the off-state after semi-on state and b) during on-state after off-state and semi-on state. Trapping due to the applied off-state voltage stress (green and red) and de-trapping of hot-electron traps during switching (blue) are shown.**

In Fig. 7b, we have added a schematic cross section to illustrate the traps during the on-state. In that case, two main differences arise. First, during the on-state, no trapping of the high drain voltage occurs; if not, detrapping of these high-voltage-induced traps also occurs. Therefore, the dynamic resistance will decrease more during the on-state, but the energy barrier level will also be lower during the on-state. This situation also favors the detrapping of electrons, which will decrease the resistance even more. This tendency explains why the 10 µs on-state decreases the dynamic resistance by up to 500 mΩ (see Fig. 3a), while during the off-state, a period as long as 500 µs is needed to reduce the dynamic resistance from 300 mΩ to 100 mΩ (see Fig. 6).

## 4. Conclusion

This paper presents a study of the dynamic resistance on commercial GaN HEMTs, showing how the structure affects dynamic resistance. The p-GaN device did not show any increase in dynamic resistance while the GaN MISHEMT had dynamic resistance greatly affected by the bias conditions and number of pulses. In this device, two different trapping mechanisms were revealed. Off-state stress trapping is induced by the high drain-source voltage applied during off-state. Hot electron trapping is induced during the semi-on state generated in hard switching events. This second trapping mechanism can be eliminated by using soft switching conditions in at least one of the switching events, as demonstrated in Fig 5.

In addition, we found evidence for detrapping caused by off-state stress on the traps induced by hot electrons during switching events. This stress mitigates the increase in dynamic resistance during the off-state of the DUT, which is relevant for switching times lower than 1 ms. With higher times, the dynamic resistance increases owing to the high voltage bias applied during the off-state. The sum of trapping and de-trapping gives the minimum value of the dynamic resistance, which is useful in the design of power electronics.

## Acknowledgment

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