High-Power Battery Discharge Regulator for Space Applications

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***Abstract*—This paper presents a new solution for a battery discharge regulator for high power space applications (power-per-module $\geq$ 5 kW) using a high efficiency step-up converter. Basic requirements are: efficiency higher than 97%, mass lower than 2.5 kg, no galvanic isolation necessary and a high Mean Time Between Failures (MTBF). Taking into account all these parameters the selected topology has been two interleaved Boost converters with passive soft switching. Small signal analysis of these two interleaved Boost converters is also presented.**

***Index Terms*—space battery discharge regulator (BDR), interleaved Boost, passive soft switching**

I. Introduction

NOWADAYS, Li-ion batteries are preferred to feed space missions during eclipse, due to their much larger power and energy density. In addition they have no memory effect and have already many flight hours, which demonstrate the technology is mature. Other important advantages are high charge efficiency, which not only saves power of the solar panels, but also reduces the heat generated during the charging process, which in space is difficult to dissipate. Another important issue to take into account when flying batteries is the insurance to pay for the mission as it depends strongly on the space heritage of the flying batteries. The less time in space of a given technology the more expensive is the insurance. Also depth-of-discharge is much more limited in space missions reaching at most 50% in Low Earth Orbits (LEO) and 70% in Medium Earth Orbits (MEO) in order to lengthen the lifetime of the batteries.

Other technologies like Ni-Cd were flown in the past and after reconditioning was learned, they demonstrated a very reliable operation, but with the penalty of a very high mass (therefore an expensive launch). Before Li-ion batteries were used, also pressurized Ni-H2 technology was flown, but its higher mass compared with Li-ion has pushed it into the background. Other problems as its high self-discharge rate and lower energy density have also made it less popular than Li-ion.

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The main suppliers of Li-ion batteries for the European space missions are SAFT and SONY (licensed by ABSL). Both have already an appreciable heritage in space missions with many batteries flown (since 1999). The other manufacturer who flies Li-ion batteries in space missions is Mitsubishi Electric from Japan. Li-ion batteries provide a larger voltage per cell. They present an energy density of up to 155 Wh/kg including losses in harness, connectors and are qualified for space use. They are expected to reach soon 180 Wh/kg and will be reaching 250 Wh/kg in the future [1][2][3][4].

On the other side, satellites in Geostationary Earth Orbits (GEO) have also increased their power budget in last decade (although this trend has not evolved as fast as expected) and therefore higher bus voltages are required. Higher battery voltages, like the one found in Li-ion technology, are therefore useful for these buses. The use of Li-ion batteries will become more and more popular in GEO missions, like telecom satellites, and suitable Battery Discharge Regulators are needed featuring high power density and high efficiency.

It is clear that classical power converter usually present a higher efficiency the smaller the voltage difference of input to output. If we take into account that actual GEO space missions are ranging powers up to of 20 kW we need a high DC voltage bus, which could have a voltage between 100 V and 120 V.

This paper presents a technological solution for a Battery Discharge Regulator coping with the main requirements, mainly for space application but also useful for any other similar application.

Our specifications stated an above-battery voltage bus and therefore a step up topology was needed for the Battery Discharge Regulator.

The converter should comply with the following specifications:

Input voltage (battery voltage)	$V_i = 82$ V $\ldots 100$ V
Output voltage (bus voltage)	$V_o = 120$ V $\pm$ 0.5 %
Switching frequency	$f_s = 100$ kHz
Output power	$P_o = 5$ kW

Modularity is also required and parallel connection of the modules should be straightforward. The easiest way to comply with this requirement is to provide the converter with current regulation. Current regulated converters with common voltage loop can be immediately parallelized, short circuit protections are inherent to the control loop and current sharing is also guaranteed.

The simplest step up topology is the Boost converter but another solution is a converter with galvanic isolation. This last solution can have problems to comply with the requirements regarding mass and efficiency.

High MTBF is also necessary in space missions and therefore two basic principles have to be observed: all components have to work without heating up significantly and the simpler the better. Cooling is very difficult in space, because only conduction and radiation is available, and heating of the components must not translate into a large ΔT. One way to assure a very low ΔT is to apply strict derating rules [5]. This assures low heating of the components and long life. The simplicity means little component count, especially active components. The fewer components and the fewer active components the lower is the probability that the system fails.

With these constraints in mind we have searched for existing topologies that are as easy and reliable as possible. An ideal topology should have the smallest amount of active components and in any case it should be unable to short the input bus or output bus in case of a single failure. Soft switching must be taken into account and finally the less reactive components are used the less mass we will have.

II. Topology

The selected topology was the step-up or Boost. It is well known, has a single switch, has flight heritage and has a well-known dynamic response. It does not have galvanic isolation what saves us mass, losses and volume of a transformer [6]. It has also demonstrated a high efficiency in high power applications and plenty of soft switching circuits have been developed for it.

Although the right-half-plane zero is a stability problem, it can be controlled (and damped) and peak current control can be easily applied to it. In fact interleaving two converters pushes the right-half-plane zero towards higher frequencies, reducing its influence in the stability.

In order to improve the Boost converter, an interleaved solution was selected to allow the use of easy to find solid state components and reduce the mass of the reactive components by compensating the ripple with interleaving. Two Boost converters of half the power level (2.5 kW) and half the current level required for the whole application have been put in parallel to achieve the required power (5 kW). The advantage obtained is that we achieve a lower output ripple, which is one of the inherent drawbacks of the Boost topology. Although this means to double the component count, lowering the current levels permits a better behavior of the active components and complies with the derating rules of ESA [5].

A. Soft switching converters

The well-established PWM technique cannot be operated at high frequency and high power levels without the penalty of switching losses. To accommodate the increasing requirements for small size and lower volume with high efficiency a passive soft switching auxiliary circuit to improve the efficiency of the hard switched converter has been used. By choosing a passive circuit, simplicity and therefore reliability is kept at a maximum.

Some PWM soft-switching techniques utilize a form of partial resonance to soften commutation and reduce circulating energy. The Quasi-Square-Wave converters [7] use the filter inductor as the resonant inductor. This topology was used as a bi-directional battery charger/discharger for NASA EOS satellite [8]. Its main drawback is its high peak current at the main switch that limits its use up to 2 kW. The ZVS-PWM converter presented in [9] solves the problem of circulating current of ZVS-QRCs by adding an auxiliary switch across the resonant inductor and also operates at constant frequency. The main disadvantage is that the main switch suffers from a high voltage stress, which is proportional to the load range under which ZVS is maintained. ZVT-PWM converters were introduced in [10] and [11]. A shunt resonant network is activated to create a partial resonance. In this way, the converter can achieve soft switching for both, the transistor and rectifier diode while preserving the advantages of the PWM converter with minimum switch voltage and current stress for wide line and load range. Its drawback is the hard switching of the auxiliary switch. High currents in the converter also translate into recovery losses in the diodes. Therefore optimal use is restricted to relatively low current applications.

Although all these soft switching circuits provide soft switching for both transitions, they usually have one or more active switches, which have to be controlled. These active switches lower the MTBF of the whole system and therefore a passive soft switching scheme was preferred.

III. Passive Soft Switching

A very complete study on passive soft switching can be found in [12] and following its results we have selected a topology with soft turn-ON switching and hard turn-OFF switching to improve efficiency but keep complexity at its minimum.

Our proposed circuit has a difference from the one proposed in [12]: it has an additional diode, Ds_2, to increase the reliability of the system from the point of view of space standards (no single point failure). If one diode fails to short no short circuit of the bus voltage (V_O) can happen. Therefore diodes are normally doubled as well as capacitors and even MOSFETs. A circuit diagram of one of the two interleaved converters is shown in the following figure.

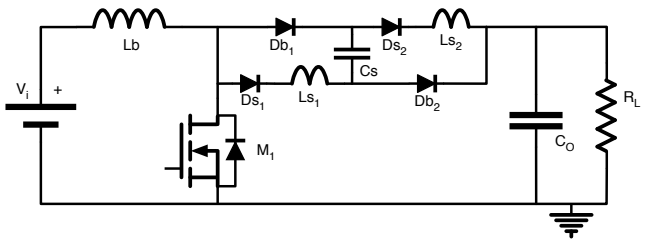

Fig. 1. Boost with passive soft-switching.

This network applied for soft turn-ON switching and with the proposed symmetrical structure has an additional benefit

that is the current sharing through both symmetrical legs of the circuit. This reduces the current stress through the diodes and makes the component selection easier.

A. Operation Principle

As we can see in Fig. 1 we have selected a soft switching cell with soft turn on only [12]. The already described modifications have also been included. The operation principle is based on a simple idea: to divert the inductor current from the switch to the diode first and then progressively change the current flow over to the leg with the diode and the inductor. Once the current is completely flowing through the main inductor and the auxiliary inductors, their connection node, where the MOSFET's drain is connected to, will be floating and therefore at turn on it is easily clamped to zero volts and the current cannot change instantaneously. Then current will build up slowly through the MOSFET beginning from zero current. The only drawback of this scheme is that the voltage to be blocked by the MOSFET is $V_O + V_{Cs}$, where Cs is chosen large enough to keep its voltage constant and of low value (aprox. 20 V in our case). Lets try to explain with a little more detail the switching process of MOSFET M_1, which is the main switch of the Boost converter.

Turn OFF

When the main switch of the Boost converter, M_1, is opened, current flowing through M_1 changes over from the switch to the path Db_1-Cs-Db_2. This transition happens therefore almost in a hard manner. Losses depend on the overlap of current through M_1 and drain-source voltage of M_1. These losses can be reduced depending on the value of the drain-source output capacitance, C_{DS1}, and the speed of the gate drive; the faster the better (although electromagnetic interference (EMI) issues have to be considered). Then the current begins to change its path progressively from Db_1-Cs-Db_2 to Ds_1-Ls_1-Cs-Ls_2-Ds_2, until the current through Db_1-Db_2 reaches zero. Current flows then only through Ds_1-Ls_1-Cs-Ls_2-Ds_2 and is equal to the current through the main inductor of the Boost converter. By adjusting the value of Ls_1 we can reach zero current through Db_1 just before we switch on M_1 and therefore avoiding its reverse recovery losses.

Turn ON

When the switch M_1 is closed, current begins to build up slowly through it and this current is taken from the current flowing through the path Ds_1-Ls_1-Cs-Ls_2-Ds_2 where it decreases. This current increase through M_1 is done under a controlled current slope imposed by Ls_1 and Ls_2. Once the current through this path reaches zero, all the current flows through the switch M_1. The design has been tuned properly to switch M_1 on when the current trough Lb is all flowing trough Ls_1 and Ls_2 to achieve a zero-current condition. Simulated waveforms of the circuit shown in Fig. 2 and Fig. 3 confirm this expected behavior.

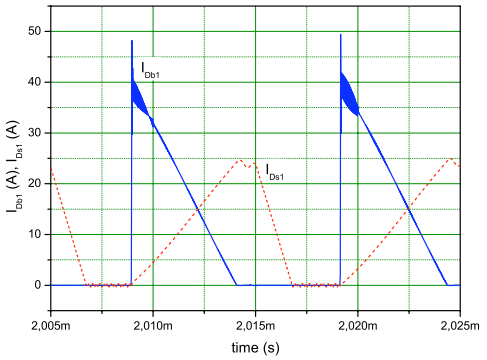

Fig. 2. Simulated converter waveforms of current, I_{Db1} and I_{Ds1}, through diodes Db_1 and Ds_1.

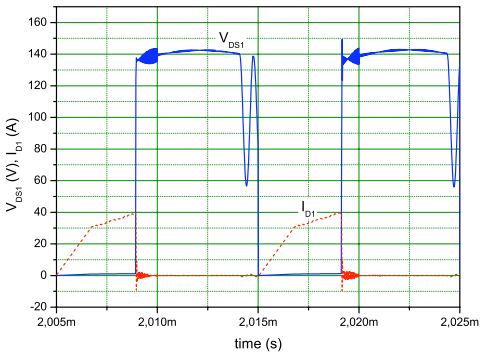

Fig. 3. Simulated converter waveforms of current through and voltage at MOSFET M_1, V_{DS1} and I_{D1}.

B. Passive Soft Switching Design

As the chosen soft switching topology is the easiest one and only used for turn on, the design is also greatly simplified. We only have to know the worst-case conditions of the turn off interval T_{OFF} during which the inductor has to change over from the Db_1 branch to the Ds_1 branch. Cs is then discharged with a negative current ramp beginning with a positive value equal to I_i that ends up at a negative value equal to $-I_i$ (we are neglecting the current ripple of Lb) and the capacitor shows then a parabolic voltage which is seen added to V_O at the MOSFET's drain (see Fig. 2). Therefore we chose the value of T_{OFF} following Eq. (1).

$$T_{OFF} \leq (1 - D_{max})T_s \tag{1}$$

The steps to follow afterwards are:

1) Fix the voltage of the capacitor Cs, taking into account that this value plus two diodes voltage drop is exactly the voltage stress of the MOSFET.
2) Calculate the value of $Ls_1 = Ls_2 = Ls$ taking into account that it is charged at the voltage of Cs.

$$Ls = T_{OFF}\frac{Cs}{I_{imax}} \tag{2}$$

A larger value of Ls will increase V_{Cs} and therefore V_{DSmax}. A smaller value of Ls will decrease it but will generate more parasitic resonances.

3) Now we have to choose a value for Cs in order to assume a fixed voltage at its terminals throughout the whole period. As current is flowing in and out of its ends in a linear way, voltage is not constant and will change in a parabolic way. If we choose a given voltage ripple V_{Cs} ripple, then

$$C_S = T_{OFF}\frac{I_i}{4V_{Cs}} \tag{3}$$

In our case T_{OFF} = 6.83 μs, I_i = 32 A, V_{Cs} = 20 V and $V_{Csripple}$ = 5 V. These values result in Ls = 4.3 μH and Cs = 11.0 μF. We chose to select a single capacitor for Cs to simplify the experimental prototype. So our final experimental value is Cs = 10 μF. The chosen value of Ls, Ls = 4 μH, is the best adjustment to the theoretical value achieved. On the other hand these values resulted correct enough and the error of 10% did not influence negatively in the behavior of the soft switching cell.

The detailed losses calculation of the converter shows (see Fig. 4) that soft switching reduces losses of transistor Q (in our case MOSFET M_1) at on switching, saving a large amount of energy, but as the number of diodes is multiplied by four, conduction losses (Dcond in Fig. 4) are increased a 26.6%. Conduction losses of the MOSFET are also halved with the soft switching circuit due to the fact that part of the current of the MOSFET is flowing through the diodes branch when switched on. Anyhow this calculation has been done using tabulated switching data of the active elements given by the manufacturer and this data is normally oversized and is obtained under certain switching conditions which, although similar, are not exactly the same than ours.

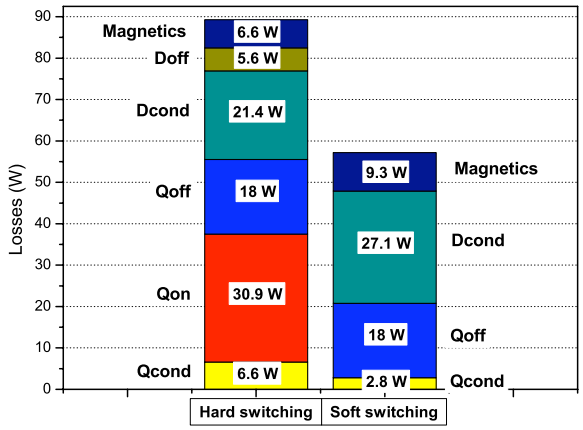

Fig. 4. Theoretical losses calculation of a 2.5 kW Boost converter with and without the proposed passive soft ON switching circuit. The losses are calculated for several items: magnetic elements (Magnetics), diodes off switching (Doff) and conducting (Dcond), MOSFET on switching (Qon), off switching (Qoff) and conducting (Qcond). Efficiency is increased theoretically by 1.3% with the proposed passive soft switching method.

The DC transfer function of the converter is also slightly modified. Its new expression includes the effect of the resonant capacitor Cs. This is an important reason to keep V_{Cs} small compared to V_O, to avoid a great difference between the theoretical duty and the real duty.

$$V_O = V_i\frac{1}{1-D} - V_{Cs} \tag{4}$$

Therefore the duty cycle also changes with this circuit. When adapting to the voltage loss at the output due to V_{Cs} it becomes,

$$D = 1 - \frac{V_i}{V_O + V_{Cs}} \tag{5}$$

Simulation and experimental results have confirmed our design.

IV. Interleaved BOOST Converters

The final structure of the converter is obtained by interleaving two of these converters (see Fig. 5). This reduces the voltage ripple at the output and if input inductors are coupled [13], good current sharing is possible. In our case current sharing is assured by peak current control. Each converter has its own peak current control loop that is governed by a single error voltage amplifier. This equalizes current in both converters.

As the supply to our converter is a battery and taken into account that the Boost topology has an input inductor, no input current ripple problem is expected. The output current ripple is reduced by the interleaving technology and the voltage ripple is very small thanks to the large bus capacitor (1 mF). This large capacitor keeps output impedance within the value required by ESA Standards [14][15].

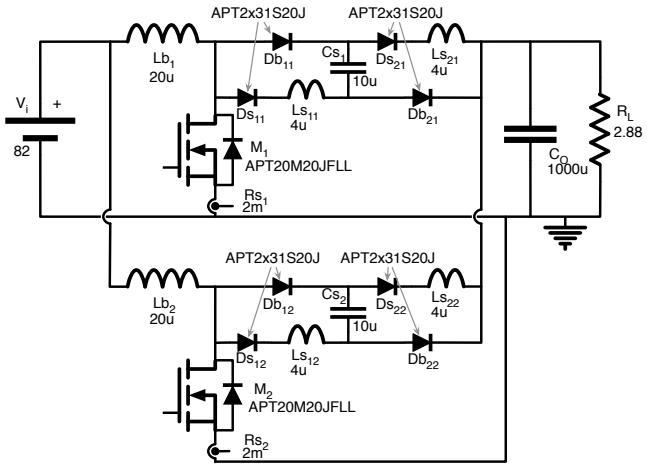

Fig. 5. Two interleaved Boost converters with passive soft ON switching circuit. Note that the current sensor?s value is the real resistance of the shunt.

Interleaving, of course, means that both converters are operated with drive signals shifted by 50% of the period. To synchronize both circuits, two shifted clock signals have been derived from a 4047 astable that sets an RS flip-flop made out of discrete NAND gates. The flip-flop is reset by the signal coming from the sensing shunt (2 mΩ) at the source of the power MOSFET.

To connect more than two converters in parallel they could be synchronized in a stair-case manner (for 4 converters each

could have 90 phase shift drive signal) and therefore reduce the generated noise by widening the spectrum, we would have to use a divider instead of the gates after the 4047 and divide by the number of converters parallelized.

One very important design issue for Boost converters is the input current ringing when the converter is started. Input inductor current oscillates with output capacitance independently of the MOSFET state (ON or OFF). The only solution to avoid a too high current (simulation gave us unacceptable values because of the low loss resistance of the whole path) through the diodes is adding an input current limiting circuit. Such circuit could be a "solid state fuse" with current limiting behavior that trips off when input current reaches a too high level during a too long time. The so-called "solid state fuse" is built with four blocks: a MOSFET, a floating power supply, a current sensor and a trip off logic. The MOSFET is normally ON and allows current to flow through it. If a programmed current limit is reached, the MOSFET enters its linear region, limiting the current. As this increases the power dissipation of the MOSFET and usually means a faulty behavior of the load, this current limitation can only be supported during a short period of time. Afterwards the MOSFET is switched off and the load is disconnected. The floating power supply is needed to feed the driving circuit of the MOSFET and the current sensor. The simplest way to build it is with a charge-pump circuit. The current sensor can be done with a current mirror and a shunt resistor. Finally the trip off logic can be made off several gates to compose a flip-flop and an RC network for timing purposes.

Under lab conditions the input current ringing is not observed if current limiting supplies are used but when the converter is connected to a battery or any other unlimited source, care must be taken to avoid this problem.

V. Small Signal Analysis

The small signal behavior of two interleaved Boost converters does not change from a single Boost converter, but values of the reactive components and load change for the whole equivalent converter depending on the interconnection of the two converters [13]. In our case, equivalent inductance becomes half its value, bus capacitance and load stays the same, as it is common to both converters. As we have a unique voltage loop controlling the inner current loop of each interleaved converter, we have used the model shown in Fig. 6.

The boxed items in Fig. 6 are repeated two times (once for each Boost converter: Boost 1 and Boost 2) and both provide current to the output capacitor (included in Gvi) and are controlled by the same control voltage, $\tilde{v}_c$. The different transfer functions, without taking into account neither parasitic elements nor the soft switching cell, are:

$$Gid_x = \frac{\tilde{i}_{Lx}}{\tilde{d}} = \frac{V_O}{Lb_x} \frac{s + \frac{2}{R_L C_O}}{s^2 + \frac{s}{R_L C_O} + \frac{(1-D)^2}{(Lb_1 || Lb_2) C_O}} \quad (6)$$

where subindex "x" stands for each Boost converter (1 or 2).

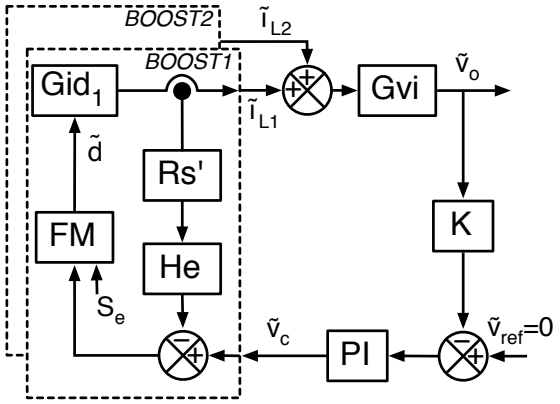

Fig. 6. Small signal model of the interleaved Boost converters with peak current control. Gid: power section transfer function; Gvi: output transfer function; FM: PWM modulator gain, where S_e is the slope of the compensation ramp; Rs': equivalent sensing resistor; He: sampling gain for peak current control; K: gain of output voltage sensor; PI: compensator of voltage loop.

$$Gvi = \frac{\tilde{v}_O}{\tilde{i}_{L1} + \tilde{i}_{L2}} = \frac{1-D}{C_O} \frac{Lb_1 || Lb_2}{R_L (1-D)^2} \frac{\frac{R_L (1-D)^2}{Lb_1 || Lb_2} - s}{s + \frac{2}{R_L C_O}} \quad (7)$$

$$He = \frac{sT_s}{e^{sT_s} - 1} \quad (8)$$

$$FM = \frac{1}{(S_n + S_e) T_s} \quad (9)$$

$$PI = \frac{A}{s}(s + \omega_z) \quad (10)$$

Eq. (6) to Eq. (10) stand for a peak current control with a classical compensation taking into account the right half plane zero. He is the sampling gain and FM the modulator gain, where S_n is the ON time slope times the equivalent sensing resistor Rs' (S_n = 0.82 V/μs in our case) and S_e is the compensation ramp (S_e = 0.2 V/μs in our case). For the control design we have chosen a bandwidth of 3 kHz. The result for the compensator is a proportional gain A = 56.7 and a zero at ω_z = 817 Hz. The resulting output impedance of the whole system was compliant with the standard norms [14][15] given by the European Space Agency (ESA).

The designed frequency response of the whole 5 kW system is shown in the following Bode diagram (Fig. 7) that agrees with the experimental results, shown later (in Fig. 11).

Fig. 8 and Fig. 9 show the control circuits of the interleaved Boost converter. Fig. 8 represents the common voltage loop control circuit, with its main error amplifier and a difference amplifier to sense the bus voltage. Fig. 9 shows the peak current control loop circuit that can be found in each Boost converter. We can see that after the current through the MOSFET, I_D, is sensed with a shunt resistor, the signal is filtered and amplified and then brought to the comparator. The other signal arriving to the comparator is the main control signal, v_c, which comes from the main error amplifier, added to the compensating ramp, S_e. The comparator generates the

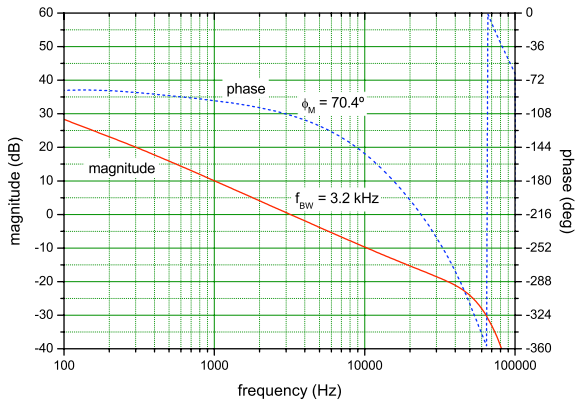

Fig. 7. Simulated open loop frequency response of the two interleaved Boost converters with common voltage loop as of block diagram of Fig. 6.

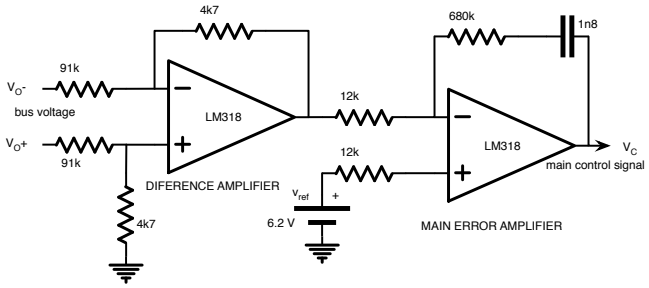

Fig. 8. Voltage loop common control stage. It senses the bus voltage and outputs the main control signal that commands the peak current level of both interleaved Boost converters.

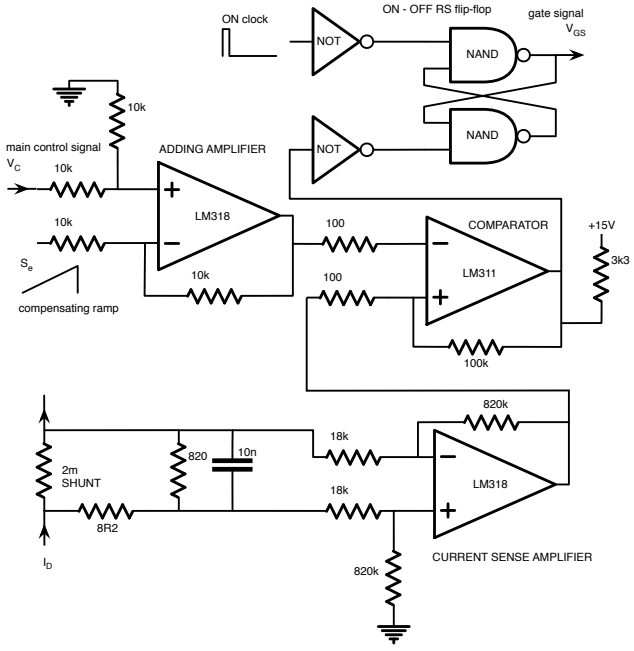

Fig. 9. Current loop control of each Boost converter. Each converter has its shunt resistor, compensating ramp and the comparator that triggers the OFF command. The ON command is set by a clock signal generated by an astable built with a 4047.

OFF signal of the MOSFET and a clock signal generates the ON signal. A discrete RS flip-flop handles these two signals and generates the PWM signal of the MOSFET. This PWM signal is fed through a driver to the gate of the MOSFET (not shown in Fig. 9).

VI. Experimental Results

Experimental results show that the specifications are being met and high efficiency is achieved. The prototype has been built based on a four layers power PCB and the transistors and diodes used are of SOT-227B package.

To avoid EMI problems OFF switching has been slowed down by increasing the value of the gate resistor but efficiency still stays very high. This is mainly due to the use of state of the art components. A better layout would allow a faster switching process and a compromise has to be reached between speed and EMI.

The V_{DS} - I_D overlap can be clearly seen during the OFF transition (Fig. 10). An additional capacitance between drain and source could also improve this behavior but increases the current through the MOSFET during turn on.

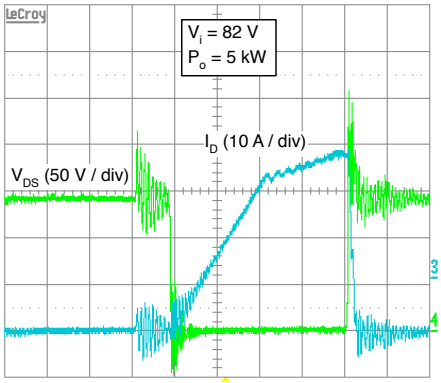

Fig. 10. V_{DS} and I_D of one of the interleaved Boost converters (V_i = 82 V, P_O = 5 kW).

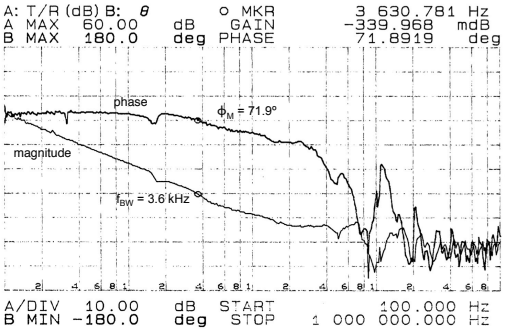

Fig. 11. Frequency response of the whole converter at V_i = 90 V, P_O = 3 kW.

The following figure shows us the efficiency of the whole converter. We see that it is always above 97% for the worst case, which corresponds to V_i = 82 V (highest current). For

comparison purposes the soft switching cell was removed and the efficiency measured again and we observe that at high power levels the efficiency improvement is about 1%. At lower power the difference is less, probably due to parasitic effects not taken into account in the theoretical calculation.

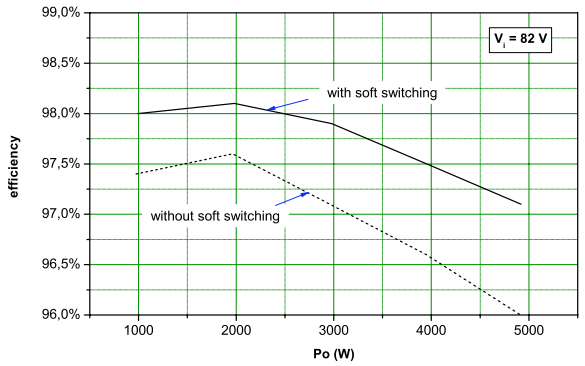

Fig. 12. Efficiency of the whole converter for the whole power with and without soft switching cell and for the lowest input voltage V_i = 82 V.

Otherwise, the measured efficiency agrees almost with the calculated results, which predicted an efficiency of 97.6% under worst-case conditions.

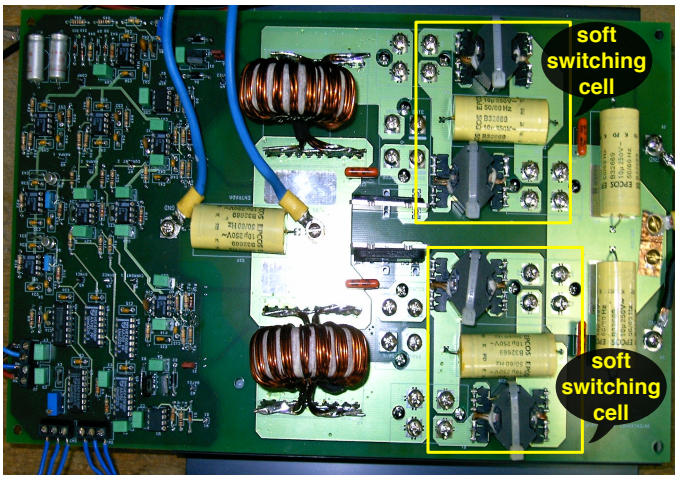

Fig. 13. Converter layout with the two symmetrical interleaved Boost units. Each of the switching cells are highlighted.

Fig. 13 shows a picture of the experimental set up. It shows the layout of the whole 5 kW converter. Symmetry has been enhanced as much as possible and all switching paths have been shorted as much as possible to reduce parasitic inductances. A four layers board should be seriously considered at this power levels if high performance is looked after. The heatsink, which is placed under the board, did not need forced air cooling during the tests although it would be necessary under continuous operation. The two cables seen at the top of the picture is the power input coming from the "solid state fuse" and feed the converter.

VII. Conclusion

The interleaved Boost converter has shown a very good performance for this application. The specified efficiency is achieved with the chosen converter. The losses depend very much on the technology used and state of the art components have been considered.

Passive soft switching applied to the interleaved Boost has shown up as very easy to implement and provides the achieved high efficiency. Passive soft switching provides also a much higher MTBF as it avoids active components. Peak current control allows easy paralleling of converters and interleaving reduces effectively the output voltage ripple.

Mass is only 950 g without taking into account the output capacitor bank and the heatsink, which is provided by the satellite platform.

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