Bidirectional High-efficiency Non-isolated Step-up Battery Regulator

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***Abstract*—This paper presents the design and results of a high-efficiency high-power (5 kW) non-isolated bidirectional DC-DC converter. High stability due to minimum phase behavior is an additional benefit of the topology. The converter is a new BOOST with output filter where input and output inductors are coupled. This converter is useful with any system that needs to charge and discharge backup batteries and can be applied in space, automotive and telecom power systems.**

***Index Terms*—Bidirectional DC/DC converter, battery regulators, space power systems**

I. Introduction

HIGH power DC buses used nowadays are normally backed up with batteries, which have to be charged and discharged depending on the bus power demand. These systems are common in telecommunication applications, space platforms and automotive electrical buses. In most part of these applications the power source is a DC voltage and therefore a DC-to-DC converter is needed.

Modularity is also required which translates into the ability of connecting modules in parallel easily. Current control solves this requirement and also provides additional benefits like inherent short circuit protection, equal current sharing and a more stable system. The use of a bidirectional unit saves mass and cost [1] [2] [3], because the same converter works as charger and discharger of the battery. One drawback is that it usually adds complexity due to the need to drive a second transistor (in our case, a "floating" drive is needed).

High efficiency is also a main goal [4]. In space, the losses not only mean heat that has to be dissipated without convection, but also higher cost during the launch due to the need of more solar panel and battery mass to overcome this power loss. Not only bidirectional solutions can increase efficiency, but also parallel power processing can be a solution [5] [6] [7].

Coupled inductors have been used in power converters as soft switching aids [8], to couple multiple converter architecture and improve current sharing [9] and to increase voltage gain [10]. The result is an improvement in power density, better control of the filter elements and higher efficiency.

In space applications power system converters also require additional measures to avoid single point failures. Space critical systems (power, attitude, etc.) usually must be single point failure free for unmanned missions and two point failure free for manned missions. A single point failure is defined as a single failure which implies the loss of the system (the power system in our application) [11].

The converter proposed does not require galvanic isolation, should comply with the following specifications and has been studied to be used in a Low Earth Orbit mission fulfilling some of the European Space Agency's (ESA) requirement:

Input voltage (battery voltage)	$V_i = 85$ V $\ldots 100$ V
Output voltage (bus voltage)	$V_o = 120$ V $\pm$ 0.5 %
Switching frequency	$f_s = 100$ kHz
Throughput power	$P_o = 5$ kW
Efficiency	$\eta > 95\%$

The converter regulates the bus voltage independently of the power flow direction. Throughput power can be in either direction, from V_i to V_o or from V_o to V_i. Input and output filtering is needed to avoid excessive ripple at the bus side and overstressing the battery with pulsating current on the other side, but this input and output filtering usually needs a close look at stability issues. This can be solved by choosing topologies which already integrate these filters [12].

To achieve a high Mean Time Between Failures (MTBF), two basic principles have to be observed: all components must have a low temperature rise and the circuit must be as simple as possible. One way to assure a high MTBF is to apply strict derating rules [13]. Therefore high efficiency is required to prevent excessive power loss and simplicity to reduce component count to its minimum.

II. The Coupled Inductor BOOST Converter

Several studies on the coupled inductor BOOST (see Fig. 1) can be found in the literature [14], [15], [16], [17], [18] and [19]. The topology is a step up converter with an additional output filter, where the input inductor and output inductor are coupled together. Transfer function is the same as for the classical BOOST converter. Bidirectionality is achieved by replacing the BOOST diode with a MOSFET and does not affect the control, as long as the control devices are capable of sensing and processing bidirectional currents.

The use of the coupled inductors assures that the converter behaves, from the control point of view, as a minimum phase system and therefore without a right half plane zero, which can create stability problems. The minimum phase condition

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is guaranteed [15] if constraint given by Eq. (9) is fulfilled or if a damping network is added [20]. In both cases the circuit can then be easily stabilized. Conductance Control [21] has been added, applied by sensing the current flowing through L_{lk}. Parallelizing is then straightforward thank to the current control loop.

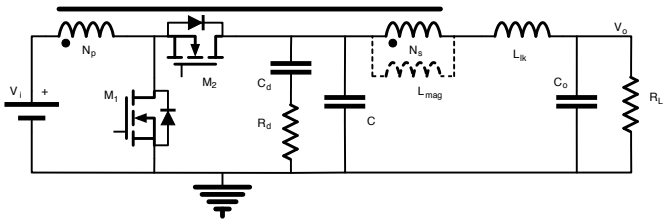

Fig. 1. Bidirectional Coupled Inductors' Boost

The great advantage of this topology compared with the two-inductor BOOST converter is that when working as a unidirectional converter its main switch is referred to ground and energy transfer is done in an inductive way instead of a capacitive way [16]. Input and output current are filtered with this topology and due to the fact that the filtering is integrated into the converter, no stability problems appear. Therefore a BOOST-like topology is available with additional output filtering and without a right half plane zero (under all circumstances if damping is added).

III. Small Signal analysis of the Coupled Inductor BOOST Converter

The small signal analysis of the Coupled Inductor BOOST Converter demonstrates the conditional stability in case no damping is added and the unconditional stability if proper damping is added [15], [17], [19]. Applying the state-space-averaging method, the topology of Fig. 1 can be linearized and its transfer functions obtained.

If we call the duty cycle D and define,

$$n = \frac{N_p}{N_s} \tag{1}$$

$$\gamma = 1 - \frac{(1-D)}{n} \tag{2}$$

$$A(s) = \frac{V_o}{1-D}\frac{(R_L C_o s + 1)}{R_L} \tag{3}$$

$$F(s) = (R_d C_d s + 1) \tag{4}$$

$$Q(s) = n^2 L_{mag} C_d s^2 \tag{5}$$

Then the output current transfer function, $P(s) = \frac{\tilde{i_L}}{\tilde{d}}$ is given by the following expression:

$$P(s) = \frac{\tilde{i_L}}{\tilde{d}} = A(s)\cdot \frac{\left((1-\gamma)n^2 L_{mag} C s^2 - \gamma\frac{n^2 L_{mag}}{R_L}s + (1-D)^2\right)F(s) + (1-\gamma)Q(s)}{\left(\left(n^2 L_{mag} C s^2 + (1-D)^2\right)F(s) + Q(s)\right)\left(L_{lk}C_o s^2 + \frac{L_{lk}}{R_L}s + 1\right) + \gamma^2\frac{n^2 L_{mag}}{R_L}s(R_L C_o s + 1)F(s)} \tag{6}$$

This expression is necessary to design the current loop. If no current loop is used and only the voltage loop is used, then the transfer function $\frac{\tilde{v_o}}{\tilde{d}}$ (see Eq. (8)) can be calculated by multiplying Eq. (6) times the expression of the output low pass filter, $LPF(s)$ (see Eq. (7)),

$$LPF(s) = \frac{R_L}{(R_L C_o s + 1)} \tag{7}$$

$$\frac{\tilde{v_o}}{\tilde{d}} = \frac{\tilde{i_L}}{\tilde{d}} \cdot LPF(s) \tag{8}$$

In case the circuit does not have the damping network branch $R_d - C_d$, the expression $P(s)$ can be simplified applying the condition of $C_d = 0$ F. Even in this case the system can become a minimum phase system.

If the Routh-Hurwitz criterion is applied to see when $\frac{\tilde{v_o}}{\tilde{d}}$ for $C_d = 0$ becomes a minimum phase system, what means that the real part of all zeros are on the left hand plane, then condition of Eq. (9) is derived [15], [17], [19].

$$\frac{N_p}{N_s} < \frac{V_i}{V_o} \tag{9}$$

With the damping network $R_d - C_d$ present, condition of Eq. (9) must not be fulfilled [15]. The design presented in this paper is based on a bidirectional coupled inductors BOOST with a damping network as shown in Fig. 1.

Using the block diagram of Fig. 2 and classical design techniques for the error amplifieres, the feedback networks can be calculated and the Bode plots obtained to confirm a stable behavior.

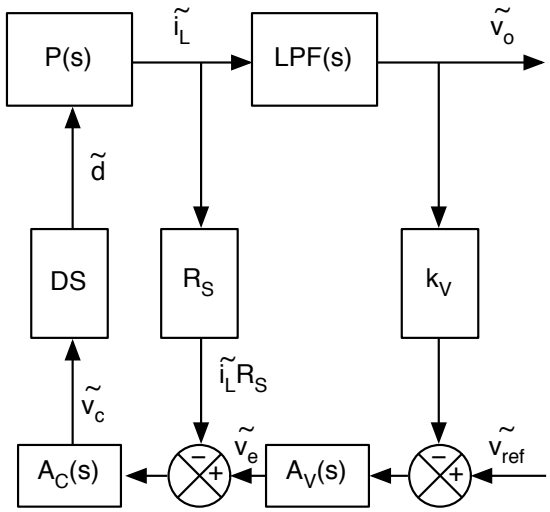

Fig. 2. Control Block diagram, where $DS = \frac{1}{V_{sawtooth}}$ is the sawtooth of the PWM modulator, R_S is the current sensing resistor, $k_V = \frac{V_o}{V_{ref}}$ is the output voltage divider sensor , $A_C(s)$ is the current error amplifier, $A_V(s)$ is the voltage error amplifier.

The expressions of the closed current loop, $A_{clc}(s)$, the overall open voltage loop, $A_{olv}(s)$, and the output impedance are,

$$A_{clc}(s) = \frac{DS\ P(s)A_C(s)R_S}{DS\ P(s)A_C(s)R_S + 1} \tag{10}$$

$$A_{olv}(s) = k_V A_V(s) \frac{A_{clc}(s)}{R_S} LPF(s) \tag{11}$$

$$Z_o(s) = \frac{LPF(s)}{k_V A_V(s) \frac{A_{clc}(s)}{R_S} LPF(s) + 1} \tag{12}$$

The bode plot of $A_{olv}(s)$ is shown in Fig. 3. It can be clearly seen that the system is completely stable and behaves as a minimum phase system. Analytical study of the converter is not affected by bidirectionality. The bidirectional behavior only translates into the need of a control circuit to handle negative currents.

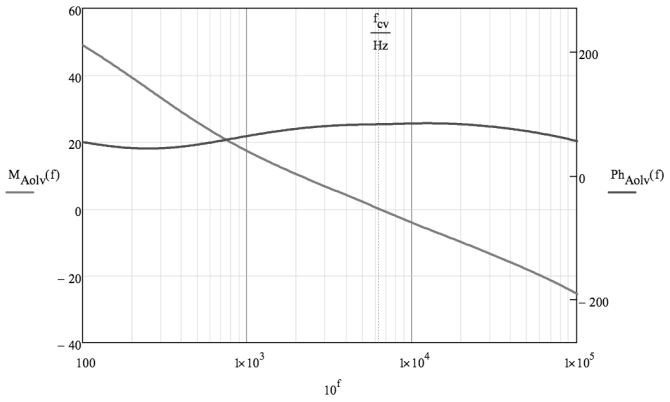

Fig. 3. Calculated open voltage loop (A_{olv}) frequency response of the converter at $V_i = 85$ V and $P_o = 5$ kW. $M(f)$ stands for magnitude in dB and $Ph(f)$ for phase in degrees.

IV. Design of the Coupled Inductor BOOST Converter

The proposed design modifies the one proposed in [14] and [15] and assumes that the relative input current ripple is equal to the relative output current ripple (Eq. (13)). Letting $\Delta I_o = \Delta I_{lk}$, and $I_o = I_{lk}$, we define β as

$$\frac{1}{\beta} = \frac{\Delta I_o}{I_o} = \frac{\Delta I_{L_{lk}}}{I_{L_{lk}}} = \frac{\Delta I_i}{I_i} \tag{13}$$

Two variables will be fixed by the designer, β, which is the ratio between the average output current and the output current ripple and the coupling factor k of the coupled inductors. Using the transformer model, the leakage inductance is L_{lk} and the magnetizing inductance is L_{mag}, and k will determine their values. As the selected coupling factor k is not close to one, as will be explained later, a large leakage inductor will result, and therefore an additional inductor must be added in the real circuit.

L_{lk} is given by

$$L_{lk} = k^2 V_o (V_o - V_i) \frac{\beta}{P_o f_s} \tag{14}$$

where P_o is the output power and f_s is the switching frequency.

The magnetizing inductance at the secondary side of the transformer, that is in parallel with the secondary winding, N_s, is given by (see Fig. 1)

$$L_{mag} = \frac{k^4}{1-k^2} V_o (V_o - V_i) \frac{\beta}{P_o f_s} \tag{15}$$

Fixing the peak-to-peak voltage ripple ΔV_C allowed at C, we can calculate C from

$$C = \frac{1}{\Delta V_C} \frac{V_o - V_i}{V_o^2} \frac{P_o}{f_s} \tag{16}$$

To not be constrained by condition given by Eq. (9), we have chosen to add the damping network $R_d - C_d$ (see Fig. 1). If one would have chosen to comply with Eq. (9), then a new set of expressions would have been developed, different from the one presented here. The damping network allows us to choose the turns ratio n of the transformer (see Eq. (17)) to fulfill the design assumption of Eq. (13), without fulfilling Eq. (9).

$$n = \frac{N_p}{N_s} = \frac{1}{k^2} \frac{V_i}{V_o} \tag{17}$$

The damping network formed by R_d and C_d, is calculated following Eq. (18) and Eq. (19). It does theoretically not imply appreciable losses, although these losses depend directly on the value of R_d, which is function of k. C_d includes a factor 10 to assure that the system is of minimum phase in any case (see [15] for more mathematical insight).

$$C_d = 10 \left(P_o^2 \frac{1-k^2}{k^2} \frac{(V_o - V_i)}{V_o^3} \frac{\beta}{P_o f_s} + \right.$$
$$\left. + 2P_o \sqrt{\frac{1-k^2}{k^2}} \sqrt{\frac{V_o - V_i}{V_o^3}} \sqrt{\frac{\beta}{P_o f_s}} \sqrt{C} \right) \tag{18}$$

The damping resistor R_d is then given by Eq. (19),

$$R_d = \frac{\sqrt{C + C_d}}{C_d} \sqrt{\frac{k^2}{1-k^2} V_o (V_o - V_i) \frac{\beta}{P_o f_s}} \tag{19}$$

As peak-to-peak voltage ripple, ΔV_C, at capacitor C is fixed by design, we can suppose that R_d is heated by the rms value of ΔV_C and if we assume that it has a triangular shape, then the power loss at R_d is,

$$P_{R_d} = \frac{\Delta V_C^2}{12 R_d} \tag{20}$$

Following Eq. (20) the power dissipation of R_d can be kept small (for $k = \frac{1}{\sqrt{2}}$, $P_{R_d} = 2.5$ W at $P_o = 5$ kW).

Once the current ripple factor β and the coupling factor k are fixed, all the other elements will be designed using the forementioned equations for the worst case ($V_{i\ min}$ and $P_{o\ max}$). The variation of k affects the size of the magnetic elements, the turns ratio and the damping network. The larger is k the larger will be the magnetic elements, L_{lk} and L_{mag}, and the damping resistor R_d, but the smaller will be the damping capacitor, C_d, and the disipated power of R_d (see Fig. 4 and Fig. 5). The current ripple does not depend on k because it has been fixed by β. The coupling effect does only

affect the stability of the converter and not the DC transfer function of the converter. Although it may seem that, with a small k, the magnetic elements could be reduced as far as one desires, for a given ripple, the power from Eq. (20) increases dramatically as well as C_d also increases its value unacceptably. A compromise will have to be found.

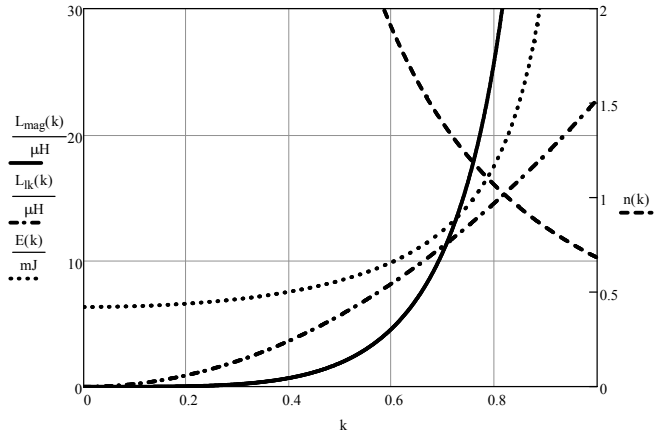

Fig. 4. Variation of L_{mag}, L_{lk}, n, and E, the energy stored in the magnetic elements, with respect to k. The energy is a way to estimate the volume and mass of the magnetic elements. It is clearly seen that for low values of k, the magnetic elements are smaller but the turn ratio increases. For $k = 0$ the magnetic elements become zero, but not its energy because of an infinite turns ratio n. This is clearly a limit and a non feasible solution.

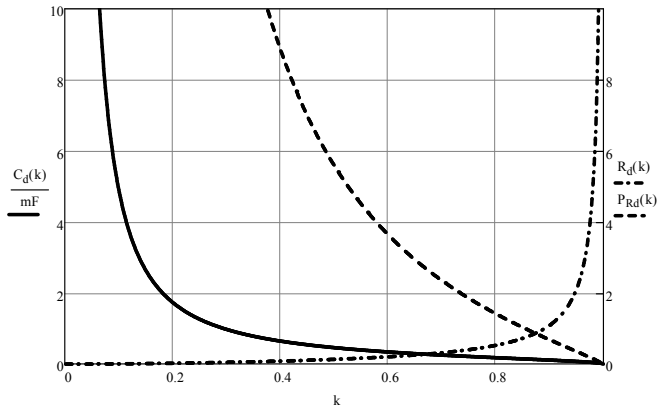

Fig. 5. Variation of C_d, R_d (in ohms) and P_{R_d} (in watts) with respect to k. It is clearly seen that for lower values of k, C_d and P_{R_d} increase dramatically. Therefore a value between $k = 0.5 \ldots 0.8$ seems a reasonable choice.

$$\frac{V_o}{V_i} = \frac{1}{1-D} \tag{21}$$

In steady state, the inverse relation of Eq. (21) applies always for input and output current (due to power balance) aswell as for input and output current ripple due to design constrained fixed by Eq. (13).

Damping does not penalize efficiency (only 0.05%) and provides us with smaller inductors by avoiding the forementioned condition (Eq. (9)). By using the presented design equations a perfect and stable behavior can be expected under all load and input voltage range.

Output capacitor C_o is designed taking into account speed of response (higher speed means smaller C_o) and output impedance (lower impedance means larger C_o). For a given crossover frequency, ω_c, and a maximum output voltage overshoot of 1% of V_o for a 50% output current step, the output capacitor is given by Eq. (22).

$$C_o = \frac{1}{\omega_c Z_o} = \frac{1}{\omega_c \left(\frac{\Delta V_o}{\Delta I_o}\right)} = \\ = \frac{1}{\omega_c \left(\frac{1\% V_o}{50\% I_{o\ max}}\right)} = \frac{1}{\omega_c \left(0.02 \frac{V_o^2}{P_{o\ max}}\right)} \tag{22}$$

V. Circuit Description

A prototype ($P_o = 5$ kW) has been designed ($\beta = 2.5,\ k = \frac{1}{\sqrt{2}},\ \Delta V_c = 3$ V, $\omega_c = 35$ kHz) and built to check the real circuit. High quality components have been used and a discrete control circuit has been built to have a higher flexibility. A four layer PCB with additional copper deposition (to cope with the high circulating currents) has been designed.

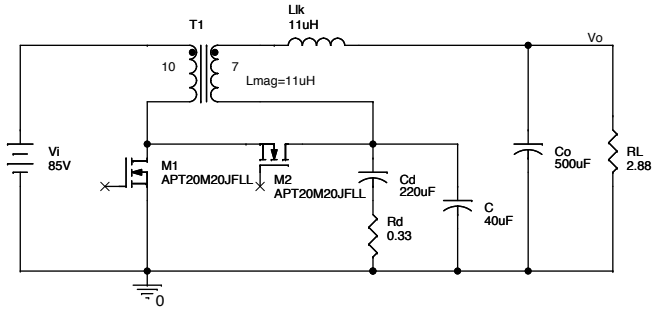

Fig. 6. Circuit diagram of the 5 kW prototype. The turns ratio of the transformer is $\frac{N_p}{N_s} = \frac{10}{7}$ and the magnetizing inductance seen from the secondary was designed as $L_{mag} = 11\ \mu$H.

Fig. 6 shows the power circuit of the prototype with the real values used. Body diodes of the MOSFET are not shown although present in the real circuit. M1 is driven with a PWM signal that has a duty cycle D and M2 with the complementary signal $(1 - D)$.

VI. Experimental Results

The experimental results have shown that the system is stable and specifications have been met. Nevertheless, losses in the damping resistor R_d were larger than expected mainly due to switching noise which increased the root-mean-square voltage across it. The damping network was acting as a noise filter circuit, but it was not designed for this purpose. This did not affect efficiency noticeably (10 W over 5 kW) but only power rating selection of resistor R_d (from 2.5 W to 10 W).

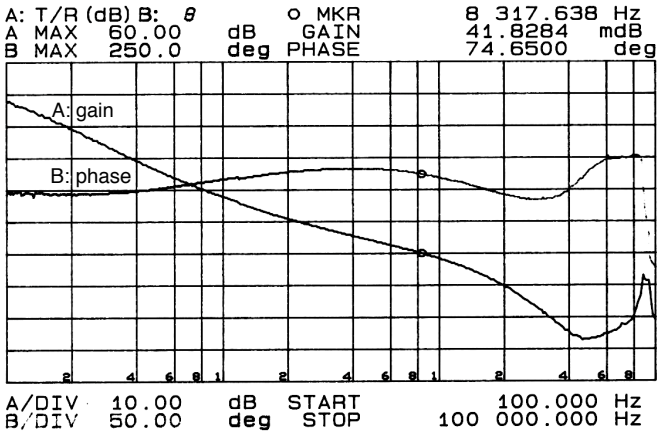

Fig. 7. Measured open loop (o/l) frequency response (A_{olv}) of the whole converter at $P_o = 5$ kW and $V_i = 85$ V. Experimental bandwidth reaches 8.3 kHz and phase margin is more than 74°, although the design was made for 6.3 kHz and a phase margin of 82°.

A. Frequency response

First we will present the experimental frequency response for the overall loop, $A_{olv}(s)$, (current loop closed and voltage loop open).

The overall frequency response of Fig. 7 shows that the system looks like a first order system. Cross over frequency is higher in the real prototype (due to variations in the values of the components) than the one designed with the model (Fig. 3). When varying power level and input voltage, crossover frequency changed from 7.6 kHz to 8.3 kHz and the phase margin changed from 87° to 74°. The system is stable over all the output power and input voltage range.

Maximum bandwidth reached is $f_{BW} = 8.3$ kHz with a phase margin of 74°.

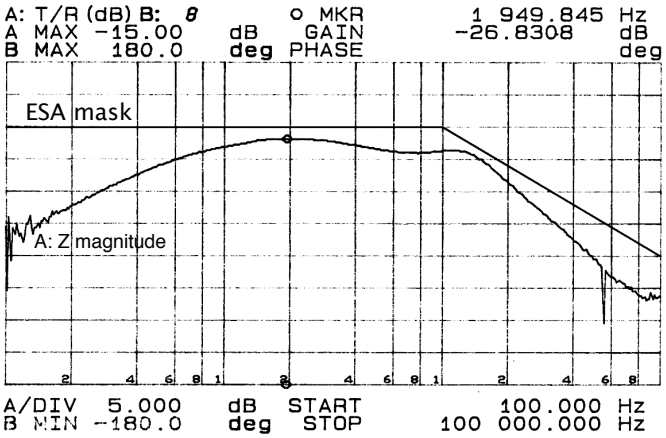

Fig. 8. Measured output impedance of the converter at $P_o = 2$ kW and $V_i = 100$ V. The maximum is at 1.9 kHz and reaches 46 mΩ staying always within the required mask of ESA.

Output impedance has also been measured to see if the requirement of ESA are fulfilled [11]. This requirement defines a mask which assures that under a 50% output current modulation the voltage overshoot is smaller than 1%. Using a special setup based on a power MOSFET working in its active region we have modulated the output current of the converter and measured the output voltage. Fig. 8 shows the calculated impedance curve and the measured curve. The mask has been also added and it can be seen that output impedance is within the limits established by ESA.

The maximum output impedance is 46 mΩ. This assures that under a 50% load change the output voltage overshoot is always below 1% of V_o (= 1.2 V) as demonstrated in Eq. (23).

$$\Delta V_o = 50\% \frac{P_{o\ max}}{V_o} Z_o = \\ = 50\% \cdot \frac{5\text{ kW}}{120\text{ V}} \cdot 46\text{ m}\Omega = 0.958\text{ V} \quad (23)$$

To assure that the impedance is correctly measured we have also made a load step of 3 kW (from 2 kW up to 5 kW) and have measured the output voltage ripple.

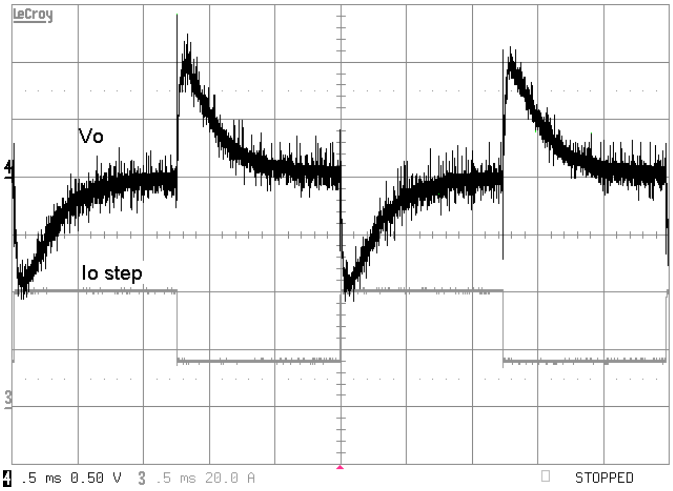

Fig. 9. Measured output voltage, V_o, ripple when applying an output current, I_o, step of 24 A (58% of $I_o max$) at 400 Hz and at $V_i = 85$ V. Ch3: I_0 (20A/div), Ch4: ΔV_0 (0.5V/div).

Load step confirms the good first order behavior of the converter and mean value of the voltage peak from Fig. 9 is $\Delta V_o \approx 1.0\ V$. Please note that the load step used at this stage is slightly larger than 50% and reaches 58%.

B. Bidirectional operation

In Fig. 10 we see waveforms of the converter in reverse operation. The current through both MOSFET is negative. We tested the converter at a reverse power of up to 2.5 kW.

MOSFET were switched in a hard way and some ringing appeared in the waveforms that did not degrade the overall behavior of the converter. Increase of noise or instabilities were not observed. No snubber circuits were put in place to reduce ringing. The ringing can be clearly seen in Fig. 10 and it appeared in both operation modes, direct and reverse.

C. Efficiency

Efficiency has been measured in direct and reverse operation. The presented efficiency shown in Fig. 11 has been

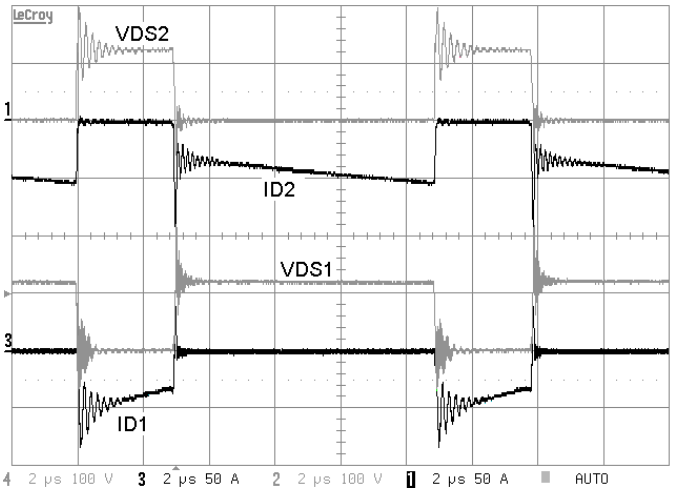

Fig. 10. Waveforms in reverse operation for both MOSFET, M_1 and M_2, are shown. Drain current, ID and drain-source voltage VDS, with the index corresponding to each MOSFET, are measured at $V_i = 85$ V and $P_o = -2.5$ kW; Ch1: I_{D2} (50A/div), Ch2: V_{DS2} (100V/div), Ch3: I_{D1} (50A/div), Ch4: V_{DS1} (100V/div). Zero level of Ch2 is the same as of Ch1 and zero level of Ch4 is the same as of Ch3.

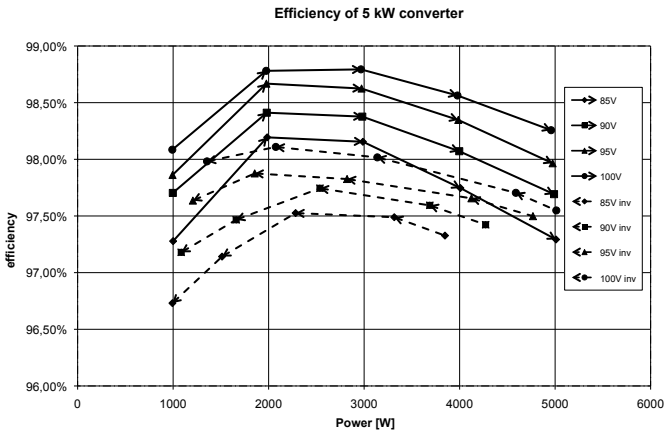

Fig. 11. Efficiency of the 5 kW hard switching prototype in direct and reverse mode. In reverse mode efficiency is about 0.7% lower then in direct mode. Continuous line represents the direct mode efficiency and dashed lines the reverse mode effciciency.

obtained including the losses of the control circuit. In direct and reverse operation, specifications have been met and efficiency is almost always higher than 97%. It is clear that at very low power levels ($P_o < 1$ kW) efficiency will be lower than specified. It is interesting to notice a slight loss of efficiency (about 0.7%) at reverse mode. This is due to the fact that a kind of synchronous rectification effect takes place. Duty cycle is always below $D = 0.317$ with our values for V_o and V_i and therefore switch M2 is always conducting more time than M1. The selected MOSFET (APT20M20JFLL) conducts about 60 A at maximum power, its on resistance is 20 mΩ and its body diode voltage drop is 1 V at 60 A. In direct operation mode, the channel voltage drop is larger than the body diode forward voltage drop for the same current level and as a result the current is shared between the body diode and the channel of the MOSFET. At the end, for the same current level, the device will suffer a lower overall voltage drop and therefore less power consumption. In reverse mode the body diode is reverse biased and the whole current will flow through the MOSFET's channel increasing its conduction losses.

VII. Conclusion

A 5 kW topology has been proposed and tested that provides optimum results as bidirectional step up DC-to-DC converter. The converter is a coupled inductor BOOST. When coupling input inductor and output filter inductor and adding a damping network, a minimum phase system results. Small signal analysis demonstrates the stability of the presented converter. Frequency response of the converter has been calculated and measured and the model has proved to be very accurate. An optimized design procedure has been proposed. All operating points of the converter in direct or reverse operation were completely stable and output voltage was always regulated. Bidirectionality has successfully been demonstrated and efficiency above 96.5% at power levels above 1 kW has been achieved. At system level this topology saves volume, mass and cost not only due to its bidirectionality but also because no additional input or output filtering is needed.

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